



# **Tiger Lake Platform Intel® Converged Security and Management Engine (Intel® CSME) 15.0 and Intel® Sensor Solution Corporate Firmware**

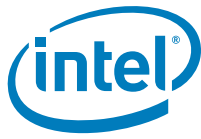
**Compliance and Testing Guide**

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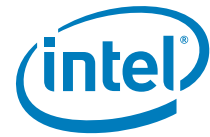
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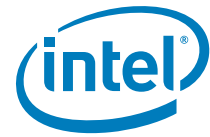
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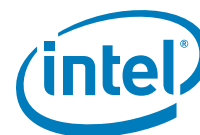


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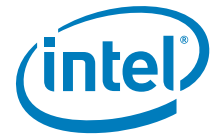




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## Revision History

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613677	0.5	<ul style="list-style-type: none"><li>• <b>Initial release</b></li></ul>	July 2019
	0.6	<ul style="list-style-type: none"><li>• <b>Removed Intel® SGX Compliance Chapter</b></li><li>• <b>Intel® Trace Hub Compliance</b><ul style="list-style-type: none"><li>— Removed test ITH_003 "BIOS - DCI Enable Post EOM".</li></ul></li><li>• <b>Intel® CSME BIOS Compliance</b><ul style="list-style-type: none"><li>— Updated terminology for the manufacturing/re-manufacturing environment.</li></ul></li><li>• <b>Intel® CSME Manufacturing or Re-Manufacturing Environment Compliance—Corporate</b><ul style="list-style-type: none"><li>— Updated terminology for the manufacturing/re-manufacturing environment.</li></ul></li><li>• <b>Common Services</b><ul style="list-style-type: none"><li>— Updated the procedure of test CS_006 for Intel® CSME Control Mode Operation after Host Profile Synchronization.</li></ul></li><li>• <b>Intel® Active Management Technology Tests</b><ul style="list-style-type: none"><li>— Updated tests to align with the support of LAN connectivity when Intel® AMT is provisioned.</li><li>— Removed non-required steps in test AMT_055.</li></ul></li><li>• <b>Intel® CSME Power Management for Corporate Designs</b><ul style="list-style-type: none"><li>— Updated XML needed for test ME_PM_27.</li><li>— Updated Table 10-2.</li></ul></li><li>• <b>Intel® CSME Power Management for Corporate Designs—Stress Testing</b><ul style="list-style-type: none"><li>— Added additional step in stress flow compliance guide test cases to check if there is any flash log in system.</li></ul></li><li>• <b>Intel® ICC Compliance</b><ul style="list-style-type: none"><li>— removed Intel® CCT usage and updated with Intel® ICC SDK usage.</li></ul></li><li>• <b>Intel® Trusted Device Setup</b><ul style="list-style-type: none"><li>— Rewrote chapter.</li></ul></li></ul>	November 2019



Document Number	Revision Number	Description	Revision Date
613677	0.7	<ul style="list-style-type: none"> <li>• <b>Added a new chapter: Intel® CSME Resiliency Compliance</b></li> <li>• <b>Removed Intel® Authenticate Chapter.</b></li> <li>• <b>Intel® CSME BIOS Compliance</b> <ul style="list-style-type: none"> <li>— Updated the pass/fail criteria of test BIOS_08.</li> </ul> </li> <li>• <b>Intel® CSME Power Management for Corporate Designs</b> <ul style="list-style-type: none"> <li>— Added a check for RSA readiness as a test step in tests ME_PM_46.1.</li> <li>— PG- LAN connectivity update.</li> </ul> </li> <li>• <b>Intel® CSME Power Management for Corporate Designs - Stress</b> <ul style="list-style-type: none"> <li>— Updated the procedure to check the flash log.</li> <li>— Updated tests PM_ST_1,2,3,4,7,12,16,17,18,19</li> </ul> </li> <li>• <b>Intel® Active Management Technology Tests</b> <ul style="list-style-type: none"> <li>— Added an overview for Intel® AMT support over different LAN solutions. See Section 10.1</li> <li>— Added LAN type options. See Section 10.2</li> <li>— Added setup of Intel® AMT over integrated LAN or WLAN. See Section 10.3.1.1</li> <li>— Added setup of Intel® AMT over integrated LAN or WLAN. See Section 10.3.1.2</li> <li>— Added WSMAN Commands Definition. See Section 10.3.2</li> <li>— Added a setup environment test for Intel® AMT basic connectivity with discrete LAN or WLAN. See Section 10.3.3.2</li> <li>— Added tests AMT_090-to-096 for Intel® AMT support over Foxville.</li> </ul> </li> <li>• <b>Intel® ICC Compliance</b> <ul style="list-style-type: none"> <li>— Removed over clocking support.</li> </ul> </li> <li>• <b>Platform Controller Hub (PCH) SoftStrap Configuration</b> <ul style="list-style-type: none"> <li>— Added additional offset changes for A1 stepping PCH.</li> <li>— Corrected offset for USB3 / PCIe Combo Port 3</li> </ul> </li> <li>• <b>Intel® Trusted Device Setup</b> <ul style="list-style-type: none"> <li>— Updated tests TDS_05-to-09.</li> <li>— Moved the E2E sealing flow to backup.</li> </ul> </li> <li>• <b>Nifty Rock Compliance</b> <ul style="list-style-type: none"> <li>— Updated procedure and pass criteria of test NR_02</li> <li>— Updated the tool name in tests NR_04-to-06.</li> <li>— Updated the procedure of test NR_07.</li> </ul> </li> <li>• <b>Appendix B—Intel® CSME Firmware Corporate Power Management in WoWLAN Coexistence Mode</b> <ul style="list-style-type: none"> <li>— Removed test cases deprecated since SKL.</li> </ul> </li> <li>• <b>Appendix C—Power Management (PM) Stress Test Corporate in WoWLAN Coexistence Mode</b> <ul style="list-style-type: none"> <li>— SPI log check procedure has been added to the test cases</li> </ul> </li> </ul>	January 2020
	0.8	<ul style="list-style-type: none"> <li>• <b>Added Chapter 25, "Platform SKU Emulation Check"</b></li> <li>• <b>Chapter 11, "Intel® CSME Power Management for Corporate Designs"</b> <ul style="list-style-type: none"> <li>— Decreased PG check time from 3 minutes to 1 minute</li> </ul> </li> <li>• <b>Chapter 10, "Intel® Active Management Technology (Intel® AMT) Tests"</b> <ul style="list-style-type: none"> <li>— Removed Test AMT_012</li> <li>— Removed notes in AMT_10x regarding active bus</li> <li>— Updated TBT Dock setup and system diagram</li> <li>— Updated Test AMT_108</li> </ul> </li> <li>• <b>Chapter 22, "Platform Controller Hub (PCH) Soft Strap Configuration"</b> <ul style="list-style-type: none"> <li>— Added USB3 and SATA combo port tests for static disable</li> <li>— Updated TPM frequency encoding to 48MHz value</li> </ul> </li> <li>• <b>Chapter 23, "Intel® System Security Report (Nifty Rock) Compliance"</b> <ul style="list-style-type: none"> <li>— Updated tests TC_NR02 and TC_NR07</li> </ul> </li> <li>• <b>Chapter 24, "Intel® Trusted Device Setup"</b> <ul style="list-style-type: none"> <li>— Removed redundant test steps</li> <li>— Reconstructed Tests procedure</li> <li>— Added unseal command by end of each step</li> </ul> </li> </ul>	April 2020



# 1 Introduction

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## 1.1 Purpose and Scope

The *Intel® Converged Security and Management Engine (Intel® CSME) and Intel® Sensor Solution Corporate Compliance Guide* for Tiger Lake Platforms is designed to provide Original Equipment Manufacturers (OEMs) and Original Design Manufacturers (ODMs) with the compliance requirements for the 2016–2017 platform implementation and the methodology and tools to verify compliance for different Intel® Manageability firmware, core components, and technologies.

This document contains the compliance requirements that reduces the number of issues in the implementation of consumer technologies. It also provides the test environment setup information, the procedure for each test, and the expected results for the purpose of validating compliancy. Requirements contained in this document target the system BIOS, Intel® CSME and other aspects of overall platform implementation.

**Note:** This document supports the following **network form factors**:

- LAN
- LAN + WLAN
- WLAN only

**Note:** This document supports Desktop, AIO, Workstation, Mobile, and Ultrabook™ **form factors** only.

**Note:** This document supports the following Operating Systems:

- Windows\* 10

## 1.2 Features

The corporate Intel® CSME firmware binary is developed to meet the demands of Intel Mobile and Ultrabook™ platforms and Microsoft\* Windows 8.1/10 InstantGo (IG) requirements. Power consumption in idle state, coupled with enhanced security features are the key deliverable for this product.

The corporate Intel® CSME firmware binary implements a power-gating feature that can reduce the Intel® CSME idle power consumption within the PCH to near-zero milliwatt. Intel® CSME enters power-gated mode, when the firmware becomes idle and the platform is in either S0 or S0ix states. This power-gated state of the Intel® CSME is represented as CM0-PG. Intel® CSME firmware exits CM0-PG state, when Intel® CSME activity is requested, or host activity requires firmware execution, such as when power transition events occur.



## 1.3 Intel® CSME Firmware General Notes

### 1.3.1 WoWLAN or WOL—Driver Feature

Intel® PETS tests that need to “Wake on LAN” may use either “Wake on LAN” (WoL) or “Wake on Wireless LAN” (WoWLAN). On platforms, which are “WLAN only” (platform that has no LAN), customers should use the WoWLAN. Refer to the WLAN driver release notes to verify that the WoWLAN feature is supported and enabled in the WLAN driver used, as the availability of the WoWLAN feature in the WLAN driver is not fully guaranteed, when this document is published.

**Caution:** In case the WoWLAN feature is not available in the WLAN driver used, do not run WoL related test.

### 1.3.2 Windows\* 8.1/10 Fast Startup (Partial Hibernate)

The “Windows\* 8.1/10 Fast Startup” feature should be disabled during Intel® PETS runs, as when enabled, platform will not go into S5 state. If this feature is enabled, S5-related test fails.

### 1.3.3 Environment Networking Recommendations

In order to reduce environment impact on tests, the following steps are proposed.

#### 1.3.3.1 General

1. Disable or shutdown non-essential applications or services on the Management Console (MC), which are not needed for testing. Applications, which periodically interact with the network to scan, it may inadvertently influence the test results.
2. Turn off the Microsoft\* Windows\* ‘Auto Discovery’ feature on the System Under Test (SUT), if enabled.
3. Turn off the Microsoft\* Windows\* ‘Network Discovery’ feature on the MC, if enabled. Refer the following links for more information on this feature:
  - a. Microsoft\* Windows\* 7/8.1/10: <http://windows.microsoft.com/en-us/windows/enable-disable-network-discovery#1TC=windows-7>.

#### 1.3.3.2 Wireless

1. Isolate the Wireless AP, so that only the SUT and MC are connected to avoid outside interference with the test.
2. Configure the Wireless AP to a frequency and channel not used by other Access Points in the area to avoid wireless crosstalk and frequency spectrum overcrowding.

**Example:** If the surrounding APs are set to operate on 2.4 GHz frequency channel 13, change testing AP to use the 5 GHz frequency channel 44, which is not used by other local APs.





## 1.4 Terminology

The keywords "MUST", "MUST NOT", "REQUIRED", "SHALL", "SHALL NOT", "SHOULD", "SHOULD NOT", "RECOMMENDED", "MAY", "MANDATORY", and "OPTIONAL" in this document are to be interpreted as described in RFC 2119.

## 1.5 Acronyms, Terminology, and Definitions

### 1.5.1 General Platform

Acronym/Term	Definition
CS	Connected Standby
FPF	Field Programmable Fuses
DHCP	Dynamic Host Configuration Protocol
DMA	Direct Memory Access
DN	Domain Name
DNS	Domain Name System
EC	Embedded Controller. Equivalent to Keyboard Controller (KBC)
EHBC	Embedded Host Based Configuration
USB-R	Integrated Device Electronics-Redirect
Intel® MEI	Intel® Management Engine Interface
Intel® TXT	Intel® Trusted Execution Technology
ISV	Independent Software Vendor
MAC	Media Access Control
MC	Management Console
PET	Platform Event Trap
PID	Provisioning ID
PPS	Provisioning Pass Phrase
PSK	Pre-Shared Key
SOAP	Simple Object Access Protocol
SOL	Serial Over LAN
SPI	Serial Peripheral Interface
SUT	System Under Test



## 1.5.2 Intel® Active Management Technology (Intel® AMT)

Acronym/Term	Definition
Agent	Software that runs on a client PC operating system
Alert	An alert occurs, when the firmware notifies the remote console that an event has occurred in the system Examples of events are a fan failure or a virus attack
ASF	Alert Standard Format
Asset Management	Intel® AMT stores hardware and software asset information in flash memory that can be read anytime; even when the PC is turned off
Closed configuration network	A closed configuration network is a special network that is used for configuration purposes only. It has no connection to the enterprise/business network
Configuration server	A software application that runs at the user configuration station. This application is responsible for connecting to the Intel® AMT firmware and automatically configuring it with pre-defined parameters
End User	The person, who uses the computer system. In a corporate setting, the end user may not have an administrator privileges on the machine
Host interface	A communication channel between the Intel firmware and applications running on the host. For Intel® AMT 1.0, this is implemented as KCS interface. In Intel® AMT 2.0 and onwards, it is implemented as Intel® MEI interface
Host or Host Processor	The processor that is running the operating system. This is different than the management processor running the Intel® AMT firmware
Host Service/Application	An application that is running on the host Processor
Intel® Management Engine Interface (Intel® MEI) driver	Intel® MEI driver—Intel® AMT host driver that runs on the host and interfaces between ISV Agent and the Intel® AMT Hardware. Intel® MEI 1 - Used for BIOS and OS interface. Intel® MEI 2 - Optional, may be used for SMI. BIOS can either enable/disable second Intel® MEI and conceal it from the host software
IT User	Information Technology user. Typically very technical and uses console to ensure multiple PCs on a network function
Intel® Converged Security and Management Engine (Intel® CSME) firmware	The Intel® CSME firmware running on the embedded processor. Cannot use "FW" generically in this PDG, as there is Fan firmware too
OS not functional	The Host OS is considered not functional in any one of the following cases: <ul style="list-style-type: none"><li>• System is in Sx power state</li><li>• System is in S0 power state and</li><li>• OS is hung</li><li>• After PCI reset</li><li>• OS watch dog expires</li><li>• OS is not present</li><li>• OS has crashed (BSOD Blue Screen of Death)</li></ul>
PET	Platform Event Trap is the ASF protocol



### 1.5.3 System States and Power Management

Acronym/Term	Definition
S0	A system state, where power is applied to all Hardware devices and system is running normally (refer to latest industry ACPI specification)
S0-S0ix	Core Well Powered; Intel® CSME Well Powered; (Intel® CSME core not consuming power) DRAM available
S3	A system state, where the host Processor is not running and power is still connected to the memory subsystem (refer to latest industry ACPI specification). Also known as standby, where the OS state is saved to memory and resumed from memory when mouse, keyboard or other activity occurs that is configured as a wake event
S4	A system state, where both the host Processor and memory are inactive (refer to latest industry ACPI specification). Also known as hibernate, where the OS state is saved to the hard disk
S5	A system state where all power to the host system is off and the power cord is still connected (refer to latest industry ACPI specification).
Sx	Any power state that is not S0
OS hibernate	When the OS saves state information to the hard disk
Standby	When the OS state is saved to memory and resumed from the memory, when mouse, keyboard or other activity occurs that is configured as a wake event.
Shut Down	A state where the system power is off and the power cord is still connected
CM0	An Intel® CSME firmware power state where all Hardware power planes are activated and the host power state is S0.
CM3	An Intel® CSME firmware power state, when the host is in Sx. The Processor DRAM Controller is turned off and DRAM power stays in off/self refresh mode. There is no UMA usage in M3 state. Less than 1MB of SRAM used for code and data. Code is executed off of flash takes ~1 ms
CM0-PG	Core Well Powered; Intel® CSME Well Powered; (Intel® CSME core not consuming power) DRAM available
CM3-PG	An Intel® CSME firmware power state, where no power is applied to the Management Engine subsystem. (Intel® CSME firmware is shut down)
Deep S4/S5	To minimize power consumption, while in S4/S5, the PCH supports a lower power version of these power states known as Deep S4/S5. In these Deep S4 and Deep S5 states, the Suspend wells are powered off, while the new Deep S4/S5 Well (DSW) remains powered. A limited set of wake events are supported by the logic located in the DSW
Global reset	A full platform reset that includes the Intel® CSME sub system and host sub system
PG	Power Gating
Intel® CSME Wake On LAN (WOL)	A feature, where the Intel® CSME sub system is powered off but will automatically resume operation, if it receives a packet from the network through the wired LAN connection



## 1.5.4 Wireless and Mobile Acronyms, Terminology, and Definitions

Acronym/Term	Definition
AP	Access Point - A device that provides a bridge between the wired LAN and the wireless LAN
BSS	Basic Service Set - A basic configuration of a wireless LAN network comprising an Access Point. All communications to and from the wireless nodes flow through the Access Point
CCK	Complementary Code Keying
CCX	Cisco Certified Extensions
DCF	Distributed Coordination Function
EAP	Extended Authentication Protocol
ESS	Extended Service Set
IEEE	Institute of Electrical and Electronics Engineers
MAC	Media Access Control hardware
MIB	Management Information Base
Network Detection feature	Network Detection is a feature designed for mobile platforms. This feature consists of an externally-exposed button on the mobile chassis that can be pressed, when the laptop lid is closed to activate a visual LED indicating to the user the presence of available wireless networks that are in range
OFDM	Orthogonal Frequency Division Multiplexing
PCF	Point Coordination Function
RSSI	Receive Signal Strength Indicator
Supplicant	An 802.1x entity that is being authenticated by the Authenticator
WEP	Wired Equivalent Privacy
Wi-Fi	Wireless Fidelity
WLAN	Wireless LAN
WoWLAN	Wake on WLAN

## 1.6 Reference Documents

Document	Document Number/Location
Intel® PCH Family SPI Flash Programming Guide	Latest Intel® CSME 15.9 Firmware Kit in VIP
Intel® Virtualization Technology for Directed I/O Architecture Specification	<a href="http://www.intel.com/technology/virtualization/index">http://www.intel.com/technology/virtualization/index</a>
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B (For Intel Virtualization, VT-x Specifications)	<a href="http://www.intel.com/products/processor/manuals/index">http://www.intel.com/products/processor/manuals/index</a>
Reference material and white papers on Intel® VT	<a href="http://www.intel.com/technology/virtualization">http://www.intel.com/technology/virtualization</a>
Intel® Virtualization Software Community	<a href="http://www.intel.com/software/virtualization">http://www.intel.com/software/virtualization</a>
Intel® TXT-enabled Xen*	<a href="http://xenbits.xensource.com/xen-unstable.hg">http://xenbits.xensource.com/xen-unstable.hg</a> and <a href="http://xen.org/download/index.html">http://xen.org/download/index.html</a>
Intel® TXT – Trusted Boot Checkout Kit	VIP Kit number - 52849
EFI shell (DUET – FAT32)	<a href="http://developer.intel.com/technology/efi/agreesource">http://developer.intel.com/technology/efi/agreesource</a>



Document	Document Number/Location
Intel® Trusted Execution Technology (Intel® TXT) - Trusted Platform Module (TPM) Nonvolatile (NV) Storage Interface Usage Application Note	# 420735
Intel® TXT Measured Launched Environment Developer's Guide	<a href="http://www.intel.com/technology/security">http://www.intel.com/technology/security</a>
Intel® APS Setup and Configuration Guide for OEMs	Available in the Intel® CSME Compliance Kit
Intel® Platform Enablement Test Suite User Guide	Located in Intel® ME Compliance and Debug Kit
Intel® APS Setup and Configuration Guide for OEMs	Located in Intel® ME Compliance and Debug Kit
Intel® Automated Power and System State Test Device (Intel® APS) User's Guide for OEMs	Located in Intel® ME Compliance and Debug Kit
Intel® AMT Tools User Guide	Located in Intel® ME Compliance and Debug Kit

## 1.7 External References

Document	Location
IEEE 802.11a Specification	<a href="http://standards.ieee.org/wireless">http://standards.ieee.org/wireless</a>
IEEE 802.11b Specification	<a href="http://standards.ieee.org/wireless">http://standards.ieee.org/wireless</a>
IEEE 802.11g Specification	<a href="http://standards.ieee.org/wireless">http://standards.ieee.org/wireless</a>
IEEE 802.11d Specification	<a href="http://standards.ieee.org/wireless">http://standards.ieee.org/wireless</a>
IEEE 802.11e Specification	<a href="http://standards.ieee.org/wireless">http://standards.ieee.org/wireless</a>
IEEE 802.11h Specification	<a href="http://standards.ieee.org/wireless">http://standards.ieee.org/wireless</a>
IEEE 802.11i Specification	<a href="http://standards.ieee.org/wireless">http://standards.ieee.org/wireless</a>
WPA Specification documentation	<a href="http://www.weca.net/OpenSection/protected_access.asp">http://www.weca.net/OpenSection/protected_access.asp</a>
ASF 2.0 Revision	<a href="http://www.dmtf.org/standards/asf/">http://www.dmtf.org/standards/asf/</a>
ACPI Specification	<a href="http://www.acpi.info/spec20c">http://www.acpi.info/spec20c</a>

## 1.8 Intel® Platform Enablement Test Suite (Intel® PETS) Testing Guidelines

Intel recommends customers to run Intel® PETS test, whenever there are any changes in:

- BIOS
- Intel® CSME firmware
- EC firmware
- Board/Silicon stepping changes

The following tests should be executed in the specified order:

1. Run Intel® PETS Setup Environment Test.
2. Run Integrated Clock Control test Package.
3. Run SPI test package.
4. Run BIOS test package.
5. Run Power Test packages.
6. Run Feature tests (Intel® AMT, WLAN, and so forth) depending on the SKU.



**Note:** To enable WOL, go to *Control Panel > System > Hardware > Device Manager > (select network adaptor) > Properties > Advanced*. Change **Enable PME** to **enabled**.

## 1.9 Intel® Boot Guard - Discrete Intel® TPM and Intel® Platform Trust Technology (Intel® PTT)

Table below shows the configuration information for the Intel® Boot Guard - Discrete TPM and Intel® Platform Trust Technology (Intel® PTT) with respect to how they work with different operating systems and firmware (Consumer/Corporate) combinations.

Refer to [Chapter 19, "Intel® Device Protection Technology with Intel® Boot Guard"](#) and [Chapter 17, "Intel® Platform Trust Technology \(Intel® PTT\) Compliancy"](#) chapter for actual compliancy tests.

Definitions:

- Supported - Intel validates this combination.
- Not Supported - Intel will not validate this combination.
- N/A - Not a valid combination from a validation standpoint.

**Table 1-1. Intel® Boot Guard - Discrete Intel® TPM and Intel® PTT**

Platform 2019 <sup>(1)</sup>	Intel® Active Client Management (Intel® ACM)	Intel® CSME Firmware	Intel® PTT	TPM 1.2	TPM 2.0
TGL Based (1-Chip and 2-chip)	Intel® ACM 3.x	Consumer	Yes	Yes	Yes
		Corporate Intel® vPro®	Yes <sup>(2)</sup>	Yes	Yes

**Notes:**

1. Refer to platform dashboard for PoR configurations.
2. Refer to Intel® PTT documentations for vPro® compatibility.

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## 2 Intel® Trace Hub (Intel® TH)

The Intel® Trace Hub Compliancy section serves as a checklist for the environment setup of Intel® Trace Hub and the SUT.

### Tools for testing:

- System Trace tool from Intel® System Debugger (part of Intel® System Studio NDA product) installed on the host computer, where the tests are run. The latest version of Intel® System Studio NDA can be downloaded from <https://registrationcenter.intel.com/en/forms/?productid=2336&SupportCode=ENA&pass=yes>. For setup and usage refer to the Get started html , System Trace User Guide and DCI user guide located at "C:\IntelSWTools\system\_studio\_2019\_nda\_xxxx\documentation\_2019\en\debugger\system\_studio\_2019\_nda\system\_debugger\system\_trace".
- Intel® SVT Closed Chassis Adapter.
- Enable DCI by setting Direct Connect Interface (DCI) Enabled under the debug tab of Intel® FIT to 'Yes'. Click Build Image and generate the full SPI image. Refer to the Bringup Guide for more details on image creation.

### 2.1 Test Coverage Summary

#### Form Factor:

D = Desktop, M = Mobile, A = All in one, W = Workstation

Test ID	Test Case Title	PETS/ Manual	Form Factor
ITH_001	Intel® CSME FW - DCI Enable (MEEN)	Manual	D M A W
ITH_002	BIOS - DCI Enable (HEEN)	Manual	D M A W
ITH_004	Capture ITH BIOS/ME Tracing Via CCA	Manual	D M A W



## 2.2 Intel® CSME FW - DCI Enable (MEEN)

<b>Test ID</b>	<b>ITH_001</b>
<b>Test Case Title</b>	Intel® CSME FW - DCI enable
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	When Intel® CSME is in manufacturing mode, DCI interface can be enabled through Intel® CSME FW (MEEN).
<b>Objective</b>	To enable DCI through Intel® CSME
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Install Intel® System Debugger, which supports the platform on a console.</li><li>2. Flash the <u>full DCI enabled</u> image on to the platform</li><li>3. Perform RTC clear to make MEEN take effective</li><li>4. Boot to BIOS and ensure that Host DCI Enable (HEEN) is set to Disabled</li><li>5. Connect the target end of the CCA to a USB3 port on the target and connect the host end of the CCA to a host with Intel® System Studio NDA software installed.</li><li>6. Open Intel® System Debugger. Use a fresh workspace and open a new Intel system trace project to configure the trace project for SUT. Refer to System Trace user Guide for more details.</li><li>7. Click <b>Connect</b> and ensure that DCI is connected without errors.</li></ol>
<b>Test Pass/Fail Criteria</b>	<p>Test passes, if user is able to connect to the target over DCI and are able to see the following message in the console:</p> <p>18:54:45 [INFO] [npk_config_api] Successfully created target connection. 18:54:45 [INFO] [npk_config_api] Querying NPK hardware...</p> <ol style="list-style-type: none"><li>1. NPK PCI access (0x0,0x1f,0x7): false</li><li>2. NPK CSR access: true</li><li>3. NPK hardware ready: true</li></ol> <p>18:54:45 [INFO] [npk_config_api] Detected Intel(R) Trace Hub hardware</p>

## 2.3 BIOS - DCI Enable (HEEN)

<b>Test ID</b>	<b>ITH_002</b>
<b>Test Case Title</b>	BIOS—CI Enable
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Check that DCI interface can be enabled through BIOS (HEEN)





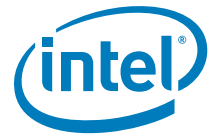
Test ID	ITH_002
Objective	To enable DCI through BIOS
Procedure	<ol style="list-style-type: none"> <li>1. Install Intel® System Debugger, which supports the platform on a console.</li> <li>2. Flash the <u>full DCI disabled</u> image on to the platform.</li> <li>3. Boot to BIOS and ensure that Host DCI Enable (HEEN) is set to Enabled, Refer to Skylake Platform PCH BIOS Enabling Recommendations for DCI and ITH Technical White Paper (# <a href="#">558380</a>) for BIOS implementation details.</li> <li>4. Connect the target end of the CCA to a USB3 port on the target and connect the host end of the CCA to a host with Intel® System Studio NDA software installed.</li> <li>5. Open Intel® System Debugger. Use a fresh workspace and open a new Intel system trace project to configure the trace project for SUT. Refer to System Trace user Guide for more details.</li> <li>6. Click <b>Connect</b> and ensure that DCI is connected without errors</li> </ol>
Test Pass/Fail Criteria	<p>Test passes, if user is able to connect to the target over DCI and are able to see the following message in the console:</p> <p>18:54:45 [INFO] [npk_config_api] Successfully created target connection.</p> <p>18:54:45 [INFO] [npk_config_api]</p> <p>Querying NPK hardware...</p> <ol style="list-style-type: none"> <li>1. NPK PCI access (0x0,0x1f,0x7): false</li> <li>2. NPK CSR access: true</li> <li>3. NPK hardware ready: true</li> </ol> <p>18:54:45 [INFO] [npk_config_api] Detected Intel(R) Trace Hub hardware</p>



## 2.4 Capturing ITH BIOS/ME Tracing Via CCA

<b>Test ID</b>	<b>ITH_004</b>
<b>Test Case Title</b>	Capture ITH BIOS/ME tracing via CCA
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	Collect Intel® CSME and BIOS logs using the STT tool
<b>Objective</b>	Collect Intel® Trace Hub logs using CCA
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Flash image that has DCI and Intel® CSME trace enabled.</li><li>2. Connect the target end of the CCA to a USB3 port on the target and connect the host end of the CCA to a host with Intel® System Studio NDA software installed.</li><li>3. Open Intel® System Debugger. Use a fresh workspace and open a new Intel system trace project to configure the trace project for SUT. Refer to System Trace user Guide for more details.</li><li>4. Check CSME and BIOS for the trace source.</li></ol> <p><b>Note:</b> Selecting BIOS is optional, if the BIOS does not support trace messages over Intel® Trace Hub</p> <ol style="list-style-type: none"><li>5. Click the green button to connect to the target on the Target Connection tab.</li><li>6. Click the play button to start the trace in the Trace Capture tab.</li><li>7. Restart the target with the restart option from Windows* menu.</li><li>8. Check, if user is able to collect BIOS and Intel® CSME logs in the STT and the messages are time correlated.</li><li>9. Shut down target by selecting shutdown option from Windows* menu.</li><li>10. Power on the target to boot from S5 to S0 state.</li><li>11. Check, if user is able to collect BIOS and Intel® CSME logs in the STT and the messages are time correlated.</li><li>12. Put the target to standby mode (S3)</li><li>13. Resume the target to boot from standby by pressing the Power Button</li><li>14. Check, if user is able to collect BIOS and Intel® CSME logs in the STT and the messages are time correlated.</li><li>15. Execute a cold reset by writing 0xE to CF9 register (mm CF9 0xE -io).</li><li>16. Check, if user is able to collect BIOS and Intel® CSME logs in the STT and the messages are time correlated.</li><li>17. Execute a warm reset by writing 0x6 to CF9 register (mm CF9 0x6 -io).</li><li>18. Check, if user is able to collect BIOS and Intel® CSME logs in the STT and the messages are time correlated.</li></ol>
<b>Test Pass/Fail Criteria</b>	The test passes, if user is able to collect BIOS and Intel® CSME logs in the STT and the messages are time correlated.





## 3 Signing and Manifesting Compliance

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This chapter includes tests to verify that OEMs are able to sign and manifest OEM components part of the SPI images. This involves creating OEM KM and placing the appropriate Public Key hashes.

### 3.1 Test Environment Setup

Signing and Manifesting documentation can be found in CSME FW kit that contains all the necessary details pertaining to OEM component signing.

### 3.2 Tools for Testing

Manifest Extension Utility (MEU): Tool used to manifest OEM Components.

OpenSSL: Freeware, can be found in Open source community. This tool integrates with MEU for signing the manifested components.

Intel® Flash Image Tool (Intel® FIT): Tool used to stitch FW image can be found in Intel® CSME FW kit.

Intel® Flash Programming Tool (Intel® FPT): Tool used to burn images on SPI platforms and set EOM state.

### 3.3 Signing and Manifesting Coverage Summary

Platform, Operating System Support, How? Column describes the test methodology.

OS Support: W = Microsoft\* Windows, WI = Microsoft\* Windows\* InstantGo\*, AOS = Android\* OS

How?: A = Fully Automated using Intel® PETS, I = Interactive using Intel® PETS and M = Manual.

Test ID	Test Case Title	PETS Package Name	OS Support	Platform	Form Factor	How?
SIGN_01	OEM KM not enabled	N/A	W WI	TGL	All	M
SIGN_02	OEM KM enabled	N/A	W WI	TGL	All	M



## 3.4 Non-Signed Image Creation

Test ID	SIGN_01
Test Case Title	OEM KM not enabled
Objective	This test verifies that OEMs are able to create a non-signed IFWI image (i.e. not enabling OEM KM), and successfully bring up the platform.
Test Pass Criteria	Platform boots to OS and ISH/iUnit/aDSP (Audio) are enabled and operational, if used. Example on ISH: This could be achieved by confirming the following test passes: ISS_FW_02 (refer to <a href="#">Section 21.4</a> )
Mandatory/ Optional	Optional
Description	<p>OEM will not sign OEM-provided binaries in the IFWI image nor input OEM KM binary.</p> <p><b>Note:</b> The OEM KM is optional. OEMs do not wish to use the OEM KM may keep out the OEM KM binary. By excluding or including OEM KM binary, the given platform is <b>permanently</b> set to require/not-require OEM KM per the configuration set in FIT. This choice is only <b>permanently committed</b> to FPF HW at the time the platform undergoes closemnf/end-of-manufacturing process. This cannot be reversed after closemnf/EOM. This is done by an FPF value called OEM_KM_Presence. This FPF value can be viewed by MEInfo.</p>
Windows* Procedure	<p><b>Note:</b> For below procedure, if user is not building image from scratch but decomposing already built image, refer to System Tools User Guide found in CSME FW kits (Decomposing an Existing Flash Image). Once image is decomposed, follow the below procedure in FIT.</p> <p><u>Manual Procedure.</u></p> <ol style="list-style-type: none"><li>Using CSME FW Bring Up guide (found in CSME FW kit), create and SPI image with ISH, iUnit and aDSP Intel signed binaries.<ol style="list-style-type: none"><li>Do not create OEM KM binary and do not include in Intel® FIT: <u>In Intel® FIT, under Platform Protection tab/xml, do not include the following:</u><ul style="list-style-type: none"><li>OEM Key Manifest Binary</li></ul></li></ol></li><li>Burn SPI image on the platform.</li><li>Verify that the platform boots to the OS and confirm ISH/iUnit/aDSP are enabled and operational.</li></ol>



## 3.5 Signed Image Creation

Test ID	SIGN_02
Test Case Title	OEM KM enabled
Objective	This test verifies that OEMs are able to sign and manifest OEM components that are authenticated by OEM KM
Test Pass Criteria	Platform boots to OS and the enabled OEM components (ISH/iUnit/Audio) are verified and operational For example on ISH, this could be achieved by confirming the following test passes: ISS_FW_02 (refer <a href="#">Section 21.4</a> )
Mandatory/Optional	Optional
Description	<p>OEM signs all OEM binaries, such as ISH, iUnit, aDSP (Audio FW) and create SPI image with OEM KM containing all the necessary keys that authenticate these components.</p> <p><b>Note:</b> The OEM KM is optional. OEMs do not wish to use the OEM KM may keep out the OEM KM binary. By excluding or including OEM KM binary, the given platform is <b>permanently</b> set to require/not-require OEM KM per the configuration set in FIT. This choice is only <b>permanently committed</b> to FPF HW at the time the platform undergoes closemfn/end-of-manufacturing process. This cannot be reversed after closemfn/EOM. This is done by an FPF value called OEM_KM_Presence. This FPF value can be viewed by MEInfo.</p>
Windows* Procedure	<p><u>Manual procedure.</u></p> <ol style="list-style-type: none"> <li>Create pairs of keys for signing OEM-provided binaries, using OpenSSL. Details of procedure are in the Chapter 5 of the TGL Signing and Manifesting Guide.</li> <li>Create OEM KM with the appropriate OEM components per the platform design, refer Chapter 7 of the Signing and Manifesting Guide.             <ol style="list-style-type: none"> <li>Enter the public key hashes of all the keys into the OEM Key Manifest's respective fields. If multiple key hashes are entered, separate nodes need to be created in the OEM Key Manifest xml, one for each different hash.</li> </ol> </li> <li>Use MEU to manifest and sign the OEM Key Manifest. Details of procedure are in the Chapter 7 of the TGL Signing and Manifesting Guide.</li> <li>Use MEU to sign (or resign if necessary) each OEM binary, whose hash is entered into the OEM Key Manifest.</li> <li>In FIT, enter the following:             <ol style="list-style-type: none"> <li>The public key hash of the OEM Key Manifest key</li> <li>The OEM Key Manifest binary</li> </ol> </li> <li>Use FIT to build an SPI image including the OEM Key Manifest. Details of procedure are in the Chapter 8 of the TGL Signing and Manifesting Guide.</li> <li>Burn the IFWI image to the platform.</li> <li>Verify that the platform boots to the OS and confirm ISH/iUnit/aDSP are enabled and operational.</li> </ol>





## 4 Intel® CSME BIOS Compliance

This chapter serves as a checklist for the environment setup for the host BIOS and Intel® Management Engine interface testing and validation.

### Test Environment:

The system under test is to be configured with the Intel® CSME **not** in manufacturing or re-manufacturing environment (fpt -closemfn) and Deep S4/S5 disabled.

### Tools for Testing:

- **Intel® Platform Enablement Test Suite**—Latest version of the tool from the Intel® CSME Compliance kit release. Refer to the *Intel® Platform Enablement Test Suite User Guide* available in the Intel® CSME Compliance kit for exact instructions on how to load and setup the Intel® Platform Enablement Test Suite software.
- Compliance\_MeBios.xml—Package should be loaded to Intel® Platform Enablement Test Suite (Intel® PETS) in order to complete this section.
- Intel® System Trace Tool (Intel® STT)

### 4.1 BIOS Compliance Test Coverage Summary

#### Form Factor:

D = Desktop, M = Mobile, W = Workstation, A = All in one

#### Network:

LAN = Systems with LAN interface and test is performed using LAN interface

WLAN = Systems with WLAN interface and test is performed using the WLAN interface

WLAN\* = Systems with WLAN interface and test is performed using the WLAN interface, only if the WLAN card supports Host Wake on WLAN.

Test ID	Test Case Title	PETS/Manual	Form Factor	Network
BIOS_01	End of POST	PETS/Manual	D M W A	LAN+WLAN; WLAN only
BIOS_02	CF9GR locking/unlocking - non Manufacturing/ re-manufacturing environment	PETS/Manual	D M W A	LAN+WLAN; WLAN only
BIOS_03	DRAM INIT Done	PETS/Manual	D M W A	LAN+WLAN; WLAN only
BIOS_05	PCI SID and SVID programming (Not available in wireless only due to firmware implementation)	PETS/Manual	D M W A	LAN+WLAN; WLAN only
BIOS_06	Intel® MEBX Binary UI	PETS/Manual	D M W A	LAN+WLAN; WLAN only
BIOS_07	Intel® CSME Software Temporary Disable	PETS/Manual	D M W A	LAN+WLAN; WLAN only
BIOS_08	Intel® CSME BIOS Extension Password reset security mechanism	PETS/Manual	D M W A	LAN+WLAN; WLAN only

#### Notes:

1. All tests in this section apply to LAN/WLAN platforms.



2. BIOS\_04: Belongs to "Intel® CSME Manufacturing or Re-manufacturing Environment Compliance—Corporate" chapter.

## 4.2 End of Power-On Self-Test (POST)

Test ID	BIOS_01
Test Case Title	End of POST
Mandatory/Optional	Mandatory
Description	When the system completes POST, BIOS is required to send an "END_OF_POST" message to the Intel® CSME by means of the Intel® MEI, when the system is transitioning from S4/S5 to S0.
Objective	<p>Verify that the BIOS sends the END_OF_POST message, when the platform is transitioning from S4/S5 and before the BIOS boot process is done and the OS starts.</p> <p>If the system is in the Intel® CSME flash protection mode, END_OF_POST message is optional.</p> <p><b>Note:</b> Host Firmware Status Register (HFSTS) address space at PCH B0:D22:F0(HFSTS1) register offset 40h [bit 4] can determine, if the Intel® CSME is in the Flash Protection Mode. For shipping machine, HFSTS address space at PCH B0:D22:F0(HFSTS1) register offset 40h [bit 4] has to be '0'.</p>
Procedure	<ol style="list-style-type: none"> <li>1. Boot the system under test to OS.</li> <li>2. Intel® Platform Enablement Test Suite performs the following: <ol style="list-style-type: none"> <li>a. For each of the following system transitions: <ol style="list-style-type: none"> <li>i. G3 -&gt; S0 (CM-Off-&gt;CM0)</li> <li>ii. S5 -&gt; S0 (CM3-&gt;CM0)</li> <li>iii. S4 -&gt; S0 (CM3-&gt;CM0)</li> </ol> </li> <li>b. Boot to OS and verify, if END_OF_POST message is sent by BIOS or not.</li> <li>c. Read the PCI address space at PCH B0:D22:F0(HFSTS1) register offset 40h [bit 4]. <ul style="list-style-type: none"> <li>— If [bit 4] is equal to '0', it means, this is not in the Intel® CSME flash protection mode.</li> <li>— If [bit 4] is equal to '1', it means it is in the Intel® CSME flash protection mode.</li> </ul> </li> </ol> </li> </ol>
Test Pass/Fail Criteria	<p>Test passes, if the BIOS Mode displays a status of POST Boot, when the system is not in the Intel® CSME flash protection mode.</p> <p>If the system is in the Intel® CSME flash protection mode, the test fails with a status of system configuration error.</p>



## 4.3 CF9GR Locking/Unlocking

Test ID	BIOS_02
Test Case Title	CF9GR(CF9h Global Reset) locking/unlocking—non Manufacturing/ re-manufacturing environment
Mandatory/Optional	Mandatory
Description	When the system is not in the manufacturing/re-manufacturing environment, BIOS must ensure that CF9GR is cleared (PWRMBASE register offset 1048h [20] = '0') and locked (by means of setting PWRMBASE register offset 1048h [bit 31] of the same register to '1'), in order to prevent the host from issuing global resets and resetting Intel® CSME before handing control to the OS.
Objective	For security reasons, the BIOS must ensure that CF9GR is cleared and locked before handing control to the OS in the shipping machine (Intel® CSME not in flash protection mode). <b>Note:</b> The recommended allocation of PWRMBASE is 0xFE000000 in PCH BIOS Specification.
Procedure	<ol style="list-style-type: none"><li>1. Manually read the PCI address space to verify the Intel® CSME Flash Protection Mode bit at PCH B0:D22:F0 register offset 40h [bit 4] is equal to '0'.</li><li>2. Manually read the memory-mapped address at PWRMBASE register offset 1048h [bit 20] to verify the bit is set to '0'.</li><li>3. Manually read the memory-mapped address at PWRMBASE register offset 1048h [bit 31] = '0' to verify the bit is set to '1'.</li></ol>
Test Pass/Fail Criteria	Test passes, if the PWRMBASE register offset 1048h [bit 20] = '0' and bit 31 of the same register is '1' when the system is not in the Intel® CSME Flash Protection Mode.

## 4.4 DRAM INIT Done

Test ID	BIOS_03
Test Case Title	DRAM INIT Done
Mandatory/Optional	Mandatory
Description	The BIOS is required to send the DRAM INIT Done message, which belongs to MKHI_OSBUP_COMMON_GROUP. This message is sent by the BIOS prior to the End of Post (EOP) on the boot, where host wants to indicate to Intel® CSME firmware that DRAM initialization is complete and CSME UMA is ready to use.
Objective	Verify that the BIOS sends the DRAM INIT Done message and the Intel® CSME transitions to CM0 with UMA.
Procedure	<ol style="list-style-type: none"><li>1. For each of the following system transitions:<ul style="list-style-type: none"><li>— G3 -&gt; S0 (CM-Off-&gt;CM0)</li><li>— S5 -&gt; S0 (CM3-&gt;CM0)</li><li>— S4 -&gt; S0 (CM3-&gt;CM0)</li></ul></li></ol> Boot to OS and read the PCI address space B0:D22:F0 to verify the Intel® CSME HFSTS1 at offset 40h [bits 8:6]. If [bits 8:6] are equal to '001', it means Intel® CSME has transitioned to CM0 with UMA. If [bits 8:6] are equal to '000', it means the Intel® CSME is not using UMA and is not in a valid state.
Test Pass/Fail Criteria	Test passes, if the Intel® CSME transitions to CM0 with UMA for the system transitions listed above <sup>(1)</sup> .

**Notes:**

1. Check for "CM0 with UMA" state once CSME exits from "CM0-PG" state.





## 4.5 PCI SID and SVID Programming

Test ID	BIOS_05
Test Case Title	PCI SID and SVID programming
Mandatory/Optional	Mandatory
Description	Verify that valid values are specified for the SID and SVID for PCI devices
Objective	Verify that the BIOS programs the Subsystem ID (SID) and Subsystem Vendor ID (SVID) of the Intel® MEI and KT devices to be compliant with the PCI Specification requirement that SID and SVID must be non-zero and Read-Only. Intel® MEI device is in PCI B0:D22:F0 and Intel® CSME SOL(KT) device is in PCI B0:D22:F3.
Procedure	<ol style="list-style-type: none"> <li>1. Configure the Intel® CSME platform.</li> <li>2. Enable the Intel® AMT and Intel® CSME SOL functionalities through the Intel® MEBX.</li> <li>3. Intel® Platform Enablement Test Suite analyzes and verify the Intel® MEI/ SOL SID and SVID fields are not zero.</li> </ol>
Test Pass/Fail Criteria	Test passes with the tool reports non-zero values for the SID and SVID fields.

## 4.6 Intel® Management Engine BIOS Extension (Intel® MEBX) Binary UI

Test ID	BIOS_06
Test Case Title	Intel® MEBX Binary UI
Mandatory/Optional	Mandatory
Description	OEM must provide a method to allow the user to invoke the Intel® MEBX UI, when requested. OEMs are now using non-verbose or silent mode for Intel® MEBX invocation to reduce BIOS POST time, and the traditional method of CTRL+P is replaced by many OEMs in favor of their own hot-key.
Objective	This test is to verify that the BIOS provides a mechanism for the Intel® MEBX UI to be invoked.
Procedure	In an Intel® CSME enabled system, following the OEM instructions to verify the Intel® MEBX UI can be entered on the system transitions.
Test Pass/Fail Criteria	<p>Test passes, if the Intel® MEBX UI can be invoked in the following system transitions:</p> <ol style="list-style-type: none"> <li>1. First System Boot - After flashing the system or performing a clear CMOS</li> <li>2. G3 -&gt; S0 (CM-Off-&gt;CM0)</li> <li>3. S5 -&gt; S0 (CM3-&gt;CM0)</li> <li>4. S4 -&gt; S0 (CM3-&gt;CM0)</li> </ol> <p>Test fails, if the Intel® MEBX UI can be invoked in the S3 -&gt; S0 system transition.</p>



## 4.7 Intel® CSME Temporary Disable

Test ID	BIOS_07
Test Case Title	Intel® CSME Software Temporary Disable
Mandatory/Optional	Optional
Description	BIOS should not send any Intel® MEI messages, when the Intel® CSME firmware is in software temporary disable mode.
Objective	If the SUT supports the ability to put the Intel® CSME in the software temporary disable mode, enable this feature using the option (typically a BIOS Setup option). The system BIOS must boot without any halt or long delays.
Procedure	<ol style="list-style-type: none"><li>1. Boot the machine.</li><li>2. Enable the Intel® CSME software temporary disable mode using the SUT provided method. A subsequent reboot occurs.</li><li>3. The Intel® CSME enters the software temporary disable mode.</li><li>4. The BIOS should not send any Intel® MEI message except for the DRAM INIT Done message and set the Intel® CSME enable message. BIOS should not prompt the Intel® MEBX hotkey entrance. No Intel® MEBX is allowed, when the system runs in software temporary disable mode.</li><li>5. The system can boot to OS successfully.</li><li>6. Restore the Intel® CSME to normal mode by disabling the Intel® CSME software temporary disable mode by using the SUT provided method. A subsequent reboot occurs.</li><li>7. The Intel® CSME enters the normal mode.</li><li>8. The system can boot to OS successfully.</li></ol>
Test Pass/Fail Criteria	Test passes, if the BIOS can boot to OS successfully without noticeable delays (5 second delays for Intel® MEI message timeout) and no error messages are printed to the SUT console, when the Intel® CSME is in software temporary disable mode.

## 4.8 Intel® MEBX Password Reset Security Mechanism

Test ID	BIOS_08
Test Case Title	Intel® CSME BIOS Extension Password reset security mechanism
Mandatory/Optional	Optional
Description	The initiation of the Intel® CSME BIOS Extension password reset process must be protected with one of the following: <ul style="list-style-type: none"><li>• Hardware mechanism that is, user must open the computer chassis and change the Hardware settings</li><li>• A CMOS clear</li><li>• A BIOS setup option</li></ul>
Objective	Verify that the platform has a mechanism to un-provision without a strong password. for example Open the computer chassis to do a CMOS clear or a BIOS setup option.
Procedure	This would depend on the platform implementation
Test Pass/Fail Criteria	Test passes, if there is a mechanism in such as using the NVRAM to un-provision the system and also restore back to factory default password (which has been set at closemnp process) without a strong password. <b>Notes:</b> <ol style="list-style-type: none"><li>1. Due to the Password encryption with unique hash calculation on different platform, Default password hash differs irrespective to the password key value in different platforms.</li><li>2. Change in the hashed password subjects to password update with in the platform.</li></ol>

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## 5 Intel® CSME Manufacturing or Re-Manufacturing Environment Compliancy - Corporate

The Intel® CSME Manufacturing/ Re-Manufacturing Environment compliancy chapter serves as a checklist for the environment setup of the host BIOS and Intel® CSME interface testing and validation, when the Intel® CSME is in Flash Protection Mode.

The tests in this section verifies that certain BIOS operations are *not* performed, when the Intel® CSME is in Manufacturing/ Re-manufacturing Environment.

### Test Environment for Intel® CSME BIOS Compliancy section:

The system under test is to be configured with the Intel® CSME in manufacturing/re-manufacturing environment and Deep S4/S5 disabled.

### Tools for Testing:

- **Intel® Platform Enablement Test Suite** - Latest version of the tool from the Intel® CSME Compliancy kit release. Refer to the *Intel® Platform Enablement Test Suite User Guide* available in the Intel Compliancy kit for exact instructions on how to load and setup the Intel® Platform Enablement Test Suite software.
- `Compliance_MeBios_ManufacturingMode.xml` - Package should be loaded to Intel Platform Enablement Test Suite in order to complete this section.

### 5.1 Intel® CSME Manufacturing Mode Compliancy Test Coverage Summary

#### Form Factor:

D = Desktop, M = Mobile, W = Workstation, A = All in one

#### Network:

LAN = Systems with LAN interface and test is performed using LAN interface

WLAN = Systems with WLAN interface and test is performed using the WLAN interface

WLAN\*\* = Systems with WLAN interface and test is performed using the WLAN interface, only if the WLAN card supports Host Wake on WLAN.

Test ID	Test Case Title	PETS/Manual	Form Factor	Network
BIOS_04	CF9GR locking/unlocking - Manufacturing/ Re-manufacturing Environment	PETS	D M W A	LAN+WLAN; WLAN only



## 5.2 CF9GR Locking/Unlocking

Test ID	BIOS_04
Test Case Title	CF9GR locking/unlocking - Manufacturing/ Re-manufacturing Environment
Mandatory/Optional	Mandatory
Description	When the system is in the Intel® CSME Manufacturing/ Re-Manufacturing Environment, BIOS must set the CF9GR register (Memory-mapped address at PWRMBASE register offset 1048h [bit 20]) to '0' to allow host only resets before handing control to the OS. For the Intel® FPT tool to perform a global reset with parameter/GRESET, the BIOS must keep the CF9GR setting unlocked (by setting PWRMBASE register offset 1048h [bit 31] of the same register to '0').
Objective	For security reasons, the BIOS must ensure that CF9GR is cleared and locked before handing control to the OS in the shipping machine. But for the usage of Intel® FPT tool with /GRESET parameter in the manufacturing/re-manufacturing environment, the BIOS must ensure that CF9GR reset mode can be changed by the Intel® FPT tool. <b>Note:</b> The recommended allocation of PWRMBASE is 0xFE000000 in PCH BIOS Specification.
Procedure	<ol style="list-style-type: none"><li>1. Boot the system under test to OS.</li><li>2. Intel Platform Enablement Test Suite performs the following:<ol style="list-style-type: none"><li>a. Manually read the PCI address space at PCH B0:D22:F0 register offset 40h [bit 4] to verify the Intel® CSME Flash Protection Mode bit is equal to '1'.</li><li>b. Manually read the memory-mapped address at PWRMBASE register offset 1048h [bit 20] to verify the bit is set to '0'.</li><li>c. Manually read the memory-mapped address at PWRMBASE register offset 1048h [bit 31] to verify the bit is set to '0'.</li></ol></li></ol>
Test Pass/Fail Criteria	Test passes, if the PWRMBASE register offset 1048h [bit 20] = '0' and [bit 31] of the same register is '0', when the system is in the Intel® CSME Flash Protection Mode.

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## 6 Common Services

This chapter covers Intel® AMT and Intel® ME related features and technologies. Among those are the following features, which require BIOS and/or system integration:

- Intel® AMT Wireless Network
- Intel® ME Firmware Update and Partial Firmware Update
- USB Key Based Configuration
- Remote and Host Based Configuration

### 6.1 Test System Configuration

Each test in this chapter contains a table describing the system configuration to which the test is applicable. Below is an example environment for a given test:

Form Factor	System Power Model	Intel® AMT Network Interface
<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input checked="" type="checkbox"/> Not Used

**Form Factor:** Describes the kind of system for which the test is applicable. These tests cover feature availability for associated platform. For Workstation form factors, the term 'Intel® AMT Server' may be also used for systems, which support Intel® AMT and run a server operating system.

**System Power Model:** Describes under which System Power Model the test is applicable under. A system with 'Standard' configuration follows traditional OS power model in sending the system to Sleep results in S3 resting system state. Systems that support Modern Standby or Microsoft\* Windows\* InstantGo\* moves to S0 Low Power Idle state upon being sent to Sleep. This is usually defined by feature support relative to the operating system in conjunction with BIOS and system device support, but may also be due to the nature of the operating system itself relative to the goals of the test.

**Intel® AMT Network Interface:** Describes the Intel® AMT networking interface used by the test, if any. 'LAN' and 'WLAN' indicate that the test is explicitly using the respective LAN and/or wireless LAN (WLAN) interface. 'Either Used' indicates that an Intel® AMT network interface is used during the test, but the test itself is not specifically define, which specific interface is to be used. 'Not Used' indicates that the test procedure does not rely on the Intel® AMT network interface; even though Intel® Platform Enablement Test Suite (Intel® PETS) or other test methodology may require general networking access to the SUT. Not all Workstation and Intel® AMT Server designs may have Intel® AMT wireless LAN interface support.

### 6.2 Test Coverage Summary

The following describes columns in the test coverage summary below. The **Test ID** is the reference identifier for the test in this document and any related tools, which reference this document. The **Title** is the name of the test. The Requirement (**Req.**) column describes the requirement for test execution. The **Form Factor**, **OS** (Operating System), and **Net** (Intel® AMT Network Interface) indicate the applicable test system configuration (refer to [Section 6.1](#) for details). **How?** column describes the test methodology.

**Req.:** M = Mandatory, C = Conditional<sup>1</sup>, and O = Optional



<sup>1</sup> Considered the same as Mandatory but with exemptions. Refer test for details.

**Form Factor:** D = Desktop, M = Mobile, and W = Workstation

**Power Model:** S = Standard, and M/I = Modern Standby or Microsoft\* Windows InstantGo\* (refer above for details)

**Net:** L = LAN, W = WLAN, E = Either Used, and N = Not Used

**How?:** A = Fully automated using Intel® PETS, I = Interactive using Intel® PETS automation, and M = Manual

**Table 6-1. Intel® AMT Test Coverage Summary**

Test ID	Title	Req.	Form Factor D M W	Power Model S M/I	Net	How?
<b>Intel® AMT Wireless Network</b>						
CS_001	Host Control Mode Operation	C	☑ ☑ ☑	☑ ☑	W	I
CS_002	Host Control Mode Operation with Intel® AMT Wireless Network Support Disabled	C	☑ ☑ ☑	☑ ☑	W	A
CS_003	Intel® ME Control Mode Operation with Host OS	C	☑ ☑ ☑	☑ ☑	W	A
CS_004	Intel® ME Control Mode Operation with BIOS	C	☑ ☑ ☑	☑ ☑	W	I
CS_005	Intel® ME Control Mode Operation with Access Point Profile Switching	C	☑ ☑ ☑	☑ ☑	W	I
CS_006	Intel® ME Control Mode Operation after Host Profile Synchronization	C	☑ ☑ ☑	☑ ☑	W	I
CS_007	Intel® ME Control and Host Control Mode Toggle	C	☑ ☑ ☑	☑ ☑	W	A
CS_008	Software Radio Frequency Kill (RF-Kill)	C	☑ ☑ ☑	☑ ☑	W	I
CS_009	Hardware Radio Frequency Kill (RF-Kill)	C	☑ ☑ ☑	☑ ☑	W	I
CS_010	Software and Hardware Radio Frequency Kill (RF-Kill)	C	☑ ☑ ☑	☑ ☑	W	I
<b>Intel® ME Firmware Update and Partial Firmware Update</b>						
CS_020	Intel® ME Firmware Update	C	☑ ☑ ☑	☑ ☑	N	I
CS_021	Intel® ME Firmware Partition Update for Secure Output Locale	M	☑ ☑ ☑	☑ ☑	N	I
CS_022	Intel® ME Firmware Partition Update for WLAN µCode	C	☑ ☑ ☑	☑ ☑	W	I
<b>USB Key Based Configuration</b>						
CS_030	USB Key File Version 2.1 with Consumable Record	M	☑ ☑ ☑	☑ ☑	E	I
CS_031	USB Key File Version 2.1 with Non-Consumable Record	M	☑ ☑ ☑	☑ ☑	E	I
CS_032	USB Key File Version 3 with Consumable Record	M	☑ ☑ ☑	☑ ☑	E	I
CS_033	USB Key File Version 4 with Consumable Record	M	☑ ☑ ☑	☑ ☑	E	I
CS_034	USB Key with Multiple Consumable Records	M	☑ ☑ ☑	☑ ☑	E	I
CS_035	USB Key File Configuration Process Cancellation	M	☑ ☑ ☑	☑ ☑	E	I
CS_036	USB Key Drive Compliance	M	☑ ☑ ☑	☑ ☑	E	I
CS_037	USB Key File Configuration Disabled at Factory Default	M	☑ ☑ ☑	☑ ☑	E	I
<b>Remote and Host Based Configuration</b>						
CS_040	Remote Configuration Support	C	☑ ☑ ☑	☑ ☑	E	A

**Table 6-1. Intel® AMT Test Coverage Summary**

Test ID	Title	Req.	Form Factor D M W	Power Model S M/I	Net	How?
CS_041	Host Based Configuration Support	M	☑ ☑ ☑	☑ ☑	E	A
CS_042	Embedded Host Based Configuration Support	O	☑ ☑ ☑	☑ ☑	E	A

## 6.2.1 Test Environment Setup

When completing tests within this chapter, especially those, which send the system to a specific S-state (S3, S4, S5, DeepSx, etc.), it is important to ensure that the network wake events are properly configured for each applicable device (LAN and/or WLAN).

If not properly configured, the system may wake from a given S-state unexpectedly during test execution as a result of various network traffic within the test environment, and cause the test to result in a *false failure*.

The following Host OS LAN/WLAN driver settings allow the network device to process specific network frames **without** waking the system where supported.

- Address Resolution Protocol (ARP) offload should be **enabled**
- Neighbor Solicitation (NS) offload should be **enabled**

The following Host OS LAN/WLAN driver settings allow the network device to wake the system, where supported, when specific network frames are received.

- Wake on Magic Packet should be **disabled**.
- Wake on Pattern Match should be **disabled**.
- Wake on Magic Packet from power off state should be **disabled**.

### **Note:**

The wording used for the Host OS driver settings above may vary, and in some cases may not be available depending on driver support or system configuration.

Beyond the guidance in this section, refer individual test setup information for details on specifically to enable relevant wake functionality in the network device, as applicable to the test. In all other cases, the above settings should be applied by default.

## 6.3 Intel® AMT Wireless Network

The section serves as a checklist for the environment setup and testing of Intel® AMT Wireless Network feature support.

### 6.3.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Windows\* supported by Intel® PETS, and the SUT should have a version of Windows\* supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one HDD.

### 6.3.2 Special Terminology

**Host Control:** The Host WLAN driver has ownership over the WLAN NIC and ensures proper network support for both the Host OS and, if enabled, Intel® AMT.



**Intel® ME Control:** The Host WLAN driver disabled, or missing, or otherwise unavailable. In this mode, the Intel® ME takes ownership over the WLAN NIC to ensure OOB manageability, when Intel® AMT Wireless Network support is enabled.

**Web UI:** The web-based interface on a system with Intel® AMT provisioned. While secure HTTP is available, the Web UI is also commonly accessible by means of HTTP as follows:

- Remotely: `http://<host_name>:16992/` or `http://<host_ip_address>:16992/`
- Locally: `http://127.0.0.1:16992/` or `http://localhost:16992/` after the Local Manageability Service (LMS) has started.

**Note:** To force the LMS to start on the SUT, run the Intel® Management and Security Status (Intel® MSS), otherwise, wait 3 to 4 minutes after boot for the service to start automatically.

### 6.3.3 Intel® AMT Wireless Interface Setup

The Web UI may be used to enable the Intel® AMT wireless network interface via the *Wireless Settings* page. Under *Wireless Management* choose one of the following Link Policies:

**Link Policy 2:** Enabled in S0

**Link Policy 3:** Enabled in S0, Sx/AC

**Link Policy 1** means Intel® AMT wireless network interface is **disabled**.

After setting the Link Policy, a wireless profile must be registered into Intel® AMT in order to enable WLAN connectivity, when the system is in S3, S4, or S5 (or in S0, when the Host WLAN driver is not available). This can also be done via the *Wireless Settings* page. Under *Profile Management*, click *New* to create a new wireless profile with associated security settings and pass phrase. For details, refer the *Intel® AMT OEM Web User Interface Guide* included in the firmware kit.

In order to complete wireless connectivity support for Intel® AMT, the appropriate Host WLAN driver supporting manageability must also be installed on the Host OS.

**Warning:** Unless specifically designated by the test configuration setup itself, the wireless LAN network security configuration settings used for testing wireless Intel® AMT must match in **both** the Intel® AMT and the Host OS driver configurations. This includes both:

- **Network Authentication** method (WPA-PSK known as *Wi-Fi Protected Access Pre-Shared Key*, or RSN-PSK known as *Robust Security Network Pre-Shared Key*)
- **Encryption** method (TKIP known as *Temporal Key Integrity Protocol*, or CCMP known as *Counter CBC-MAC Protocol* or AES)

Problems may occur in testing, if both the Network Authentication and Encryption methods do not align. When testing on Microsoft\* Windows environments, the Host OS may default to the highest Encryption level supported by the Access Point, when connecting to it for the first time. If the Access Point supports multiple Encryption (TKIP and CCMP) protocols at the same time, there is the risk that the Host OS selects CCMP (AES) automatically, while the test operator selects TKIP. This is considered a wireless security configuration mismatch and should be fixed before starting testing.





With the Intel® AMT Link Policy is set to 2 or 3 (wireless manageability support enabled), the Host WLAN driver installed, and the Host OS connected to a wireless access point, the Web UI shows the assigned Intel® AMT wireless network IP address on the *System Status* screen, when the system is in S0.

With the Intel® AMT Link Policy is set to 1 (wireless manageability support disabled), the Web UI shows no wireless network IP address on the *System Status* screen. To clear any Intel® AMT wireless configuration previously entered, the Access Point profiles registered on the *Wireless Settings* page should be deleted. It is only possible to delete an Access Point profile, if it is not in use by Intel® AMT.

**Note:** To thoroughly clear and reset the Intel® AMT wireless network configuration, use either the Intel® Management Engine BIOS Extension (Intel® MEBX) full unprovision menu, the CMOS clear mechanism, or the BIOS unconfigure without password mechanism. Refer the *Intel® Management Engine BIOS Extension User's Guide* or *Intel® ME BIOS Specification* documents for details.

When the system is in Sx, or the Host WLAN driver is not functional, the wireless profile registered to Intel® AMT, via the Web UI is used for enabling wireless manageability support.

### 6.3.3.1 Common Issues and Troubleshooting

The following is a list of common issues that can occur during wireless Intel® AMT testing and associated recommendations on how to check test environment and system configuration. Before checking S3-related issues, review the *Intel® AMT and Wake On Wireless LAN Coexistence* feature overview.

1. Cannot connect to the Web UI locally from the SUT.
  - a. Verify that the Local Manageability Service (LMS) is installed and running on the SUT. If necessary, restart the service to verify that connectivity can be restored.
  - b. Verify access using an alternate Web browser on the SUT.
2. There is no *Wireless Settings* menu in the Web UI, the data shown on the *Wireless Settings* page is incorrect, or the controls on the *Wireless Settings* page are not behaving as expected.
  - a. Verify that a wireless LAN card supporting Intel® vPro™ Technology is installed in the system.
  - b. Verify that the *WLAN Power Well* configuration is correctly set in the SPI image. Refer the firmware *Bring Up Guide* included with the firmware kit for details.
  - c. Verify that the correct wireless LAN uCode is installed in the firmware. Refer the *Intel® ME System Tools User Guide* for details on how to verify that there is no wireless LAN uCode mismatch and how to manually update the wireless LAN uCode.
  - d. Verify that the Controller Link (C-Link) hardware interface is properly connected to the WLAN NIC and that it is functional. Refer the *Platform Controller Hub External Design Specification* for details.
3. The *System Status* screen on the Web UI shows that there is no IP address for the wireless interface when the system is in S0, S0ix (Microsoft\* InstantGo\* mode), or S3 with Wake On Wireless LAN Coexistence **enabled**.

It may take a few seconds for the Host WLAN driver to synchronize IP and MAC address information with the Intel® ME firmware. As such, a few refreshes of the Web UI may be needed after the system completes transition to the destination S-state.

- a. Verify that the correct Intel® Wireless LAN Host OS driver is installed and that it supports Intel® vPro™ Technology with Intel® AMT.



- b. Verify that the Host OS is connected to an Access Point, which supports either WPA-PSK or RSN-PSK network authentication, and either TKIP or CCMP (AES) encryption.
  - c. Verify that the wireless Link Policy is **not** set to Link Policy 1 (disabled) in the Web UI.
4. The *System Status* screen on the Web UI shows that there is no IP address for the wireless interface, when the system is in S4, S5, or S3 with Wake On Wireless LAN Coexistence **disabled**.
  - a. Verify that the wireless Link Policy is not set to Link Policy 1 (disabled) in the Web UI.
  - b. Verify that the an Access Point which supports either WPA-PSK or RSN-PSK network authentication, and either TKIP or CCMP (AES) encryption is registered with Intel® AMT. This can be done through the Web UI.
5. Cannot connect to the Web UI remotely or KVM/Storage/SoL redirection does not function, while the system is in S0, S0ix (Microsoft\* InstantGo\* mode), or S3 with Wake On Wireless LAN Coexistence **enabled**.
  - a. Verify that the Intel® AMT has received an IP address from the Host OS driver while in S0. This can be done through the Web UI.
  - b. If the system is booted to an OS, which does not have an Intel® Wireless LAN Host OS driver that supports Intel® vPro™ Technology with Intel® AMT installed, wait 2 minutes. If the Intel® Wireless LAN driver does not take ownership of the WLAN NIC within 2 minutes after power-on, the Intel® ME attempts to take ownership and try to connect to the Access Points registered within Intel® AMT (via the Web UI).
6. Cannot connect to the Web UI remotely or KVM/Storage/SoL redirection does not function, while the system is in S5, S4, or S3 (regardless of Wake On Wireless LAN Coexistence configuration).
  - a. Verify that the correct wireless LAN uCode is installed in the firmware. Refer the *Intel® ME System Tools User Guide* for details on how to verify that there is no wireless LAN uCode mismatch and how to manually update the wireless LAN uCode.
  - b. Verify that the WLAN NIC is powered by the EC/BIOS, when SLP\_WLAN# is de-asserted high. Refer the *Platform Controller Hub External Design Specification* for details.
  - c. Verify that the RF-Kill (W\_DISABLE#) signal to the WLAN NIC is not asserted low by the EC/BIOS.
  - d. If the SUT is running Microsoft\* Windows 10, verify that the random hardware addresses (MAC address) Wi-Fi setting is **disabled**. Intel® AMT wireless feature coexistence is not available for this Host OS feature. For more information about this Host OS feature, refer to the Windows\* 10 Wi-Fi settings and documentation provided by Microsoft\*.
7. The KVM/Storage/SoL redirection is lost during system reboot or during transition from Sx to S0.
  - a. Verify that the Host OS wireless and Intel® AMT wireless network security configurations match.



## 6.3.4 Host Control Mode Operation

<b>ID</b>	<b>CS_001</b>				
<b>Title</b>	Host Control Mode Operation				
<b>Requirement</b>	Mandatory - Exempt for systems without Intel® AMT WLAN support				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS with test operator interaction				
<b>Description</b>	Intel® AMT connects over wireless LAN in S0, when the Host WLAN driver has control over the WLAN NIC.				
<b>Objective</b>	Verify that the Intel® AMT connection over wireless LAN in S0 occurs, when the Host WLAN driver is operational and connected to an Access Point.				
<b>Setup</b>	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should <b>not</b> be configured or operational.</p> <p>If the SUT is already configured, either unprovision/re-provision the SUT to clear the wireless network configuration, or disable and completely clear the wireless network configuration via the Web UI (refer <a href="#">Section 6.3.3</a> for details).</p>				
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Verify that the Host WLAN driver is enabled.</li> <li>2. Configure the Host OS to connect to an Access Point, which supports either Wi-Fi Protected Access Pre-Shared Key (WPA-PSK) or Robust Security Network Pre-Shared Key (RSN-PSK) authentication, and either Temporal Key Integrity Protocol (TKIP) or Counter CBC-MAC Protocol (CCMP) encryption.</li> <li>3. Verify the Host OS receives an IP address on the Access Point.</li> <li>4. Ping the SUT from the management console via the wireless network interface. This may require disabling firewall, anti-virus, or other software, and/or performing other configuration on the Host OS of the SUT to enable ping receipt and response.</li> <li>5. Open the Web UI from the SUT locally (refer <a href="#">Section 6.3.2</a> for details) and confirm Intel® AMT wireless <b>does not have</b> a network IP address on the <i>System Status</i> page.</li> <li>6. Follow the instructions in <a href="#">Section 6.3.3</a> for enabling wireless network connectivity via Link Policy 2 or 3 setting in the Web UI.</li> <li>7. Open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li> </ol>				
<b>Pass Criteria</b>	The test passes, if Intel® AMT responds over the wireless network, when the Host WLAN driver controls the WLAN NIC in Host Control mode.				
<b>References</b>	For details on Intel® AMT Web UI access or Wireless Setting configuration, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .				

## 6.3.5 Host Control Mode Operation without Intel® AMT Wireless Network Enabled

<b>ID</b>	<b>CS_002</b>				
<b>Title</b>	Host Control Mode Operation with Intel® AMT Wireless Network Support Disabled				
<b>Requirement</b>	Mandatory - Exempt for systems without Intel® AMT WLAN support				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS				



ID	CS_002
Description	Intel® AMT will not connect over wireless LAN in S0, when the Link Policy is set to 1 (Disabled).
Objective	Verify that there is no Intel® AMT connection over wireless LAN in S0, when the Host WLAN driver is operational and connected to an Access Point, but the Intel® AMT wireless network interface is disabled.
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer to <a href="#">Section 6.3.3</a> for details).
Procedure	<ol style="list-style-type: none"><li>1. Open the Web UI from the SUT locally (refer <a href="#">Section 6.3.2</a> for details) and confirm Intel® AMT wireless has a network IP address on the <i>System Status</i> page.</li><li>2. Follow the instructions in <a href="#">Section 6.3.3</a> to disable wireless network connectivity via Link Policy 1 (Disabled) setting in the Web UI.</li><li>3. Confirm Intel® AMT wireless <b>does not have</b> a network IP address on the <i>System Status</i> page in the Web UI.</li><li>4. Attempt to open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details). This test step should fail.</li><li>5. Ping the SUT from the management console via the wireless network interface. This may require disabling firewall, anti-virus, or other software, and/or performing other configuration on the Host OS of the SUT to enable ping receipt and response.</li></ol>
Pass Criteria	The test passes, if Intel® AMT access is no longer available over the wireless network, when the Host WLAN driver controls the WLAN NIC in Host Control mode with Intel® AMT wireless network support disabled. In this configuration, the Host OS must still receive wireless network support via the Host WLAN driver.
References	For details on Intel® AMT Web UI access or Wireless Setting configuration, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .



### 6.3.6 Intel® ME Control Mode Operation with Host OS

<b>ID</b>	<b>CS_003</b>				
<b>Title</b>	Intel® ME Control Mode Operation with Host OS				
<b>Requirement</b>	Mandatory - Exempt for systems without Intel® AMT WLAN support				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS				
<b>Description</b>	Intel® AMT connects over wireless LAN in S0, when the Host WLAN driver is disabled or not installed.				
<b>Objective</b>	Verify that the Intel® AMT connection over wireless LAN in S0 occurs, when the Host WLAN driver is disabled or not installed.				
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer to <a href="#">Section 6.3.3</a> for details).				
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Wait for <b>2 minutes</b> before starting the test after the Host OS loads to allow entry into Host Control mode.</li> <li>2. Open the Web UI from the SUT locally (refer <a href="#">Section 6.3.2</a> for details) and confirm Intel® AMT wireless has a network IP address on the <i>System Status</i> page.</li> <li>3. Open the Host OS device manager on the SUT and disable the Host WLAN driver.</li> <li>4. Wait for <b>1 minute</b> as the SUT moves into Intel® ME Control mode.</li> <li>5. Open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li> <li>6. In the Host OS device manager on the SUT, re-enable the Host WLAN driver.</li> </ol>				
<b>Pass Criteria</b>	The test passes, if Intel® AMT responds over the wireless network when the Host WLAN driver is disabled (or not installed).				
<b>References</b>	For details on Intel® AMT Web UI access or Wireless Setting configuration, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .				

### 6.3.7 Intel® ME Control Mode Operation with BIOS

<b>ID</b>	<b>CS_004</b>				
<b>Title</b>	Intel® ME Control Mode Operation with BIOS				
<b>Requirement</b>	Mandatory - exempt for systems without Intel® AMT WLAN support				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS with test operator interaction				
<b>Description</b>	Intel® AMT will connect over wireless LAN in S0, when there is no Host OS.				
<b>Objective</b>	Verify that the Intel® AMT connection over wireless LAN in S0 occurs, when there is no Host OS and WLAN device driver loaded 2 minutes after boot.				
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer to <a href="#">Section 6.3.3</a> for details).				



<b>ID</b>	<b>CS_004</b>
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Turn on the SUT to S0, and enter the BIOS menu.</li><li>2. Wait <b>at least 2 minutes</b>.</li><li>3. Open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li><li>4. Gracefully restart the system back to Host OS.</li></ol>
<b>Pass Criteria</b>	The test passes, if Intel® AMT responds over the wireless network when the BIOS is loaded after 2 minutes.
<b>References</b>	For details on Intel® AMT Web UI access or Wireless Setting configuration, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .

### 6.3.8 Intel® ME Control Mode Operation with Access Point Profile Switching

<b>ID</b>	<b>CS_005</b>			
<b>Title</b>	Intel® ME Control Mode Operation with Access Point Profile Switching			
<b>Requirement</b>	Mandatory - exempt for systems without Intel® AMT WLAN support			
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	Intel® AMT connects over wireless LAN in S0, when the Host WLAN driver is disabled or not installed. If there is a second Access Point profile registered with Intel® AMT, it shall be used when connectivity to the primary Access Point is lost.			
<b>Objective</b>	Verify that the Intel® AMT connection over wireless LAN in S0 occurs, when the wireless connectivity to the primary Access Point is lost in Intel® ME Control mode.			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer to <a href="#">Section 6.3.3</a> for details) with atleast one Access Point profile registered.			



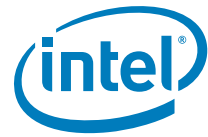
ID	CS_005
Procedure	<ol style="list-style-type: none"> <li>1. Wait <b>2 minutes</b> before starting the test after the Host OS loads to allow entry into Host Control mode.</li> <li>2. Open the Web UI from the SUT locally (refer <a href="#">Section 6.3.2</a> for details) and confirm Intel® AMT wireless has a network IP address on the <i>System Status</i> page. Ensure to note the wireless IP address assigned by the current Access Point.</li> <li>3. If necessary, follow the instructions in <a href="#">Section 6.3.3</a> to add a second Access Point profile. There should be atleast two Access Point profiles, each with the following different configuration: <ul style="list-style-type: none"> <li>• One with WPA-PSK authentication and TKIP encryption.</li> <li>• One with RSN-PSK authentication and CCMP encryption.</li> </ul> </li> <li>4. Turn <b>off</b> the radios of the Access Points that the SUT is <b>not</b> connected to.</li> <li>5. Open the Host OS device manager on the SUT and disable the Host WLAN driver.</li> <li>6. Wait <b>1 minute</b> as the SUT moves into Intel® ME Control mode.</li> <li>7. Open the Web UI from the SUT locally (refer <a href="#">Section 6.3.2</a> for details) and verify the SUT is connected to the first (and only available) Access Point by attempting to delete its profile via the Web UI. This should fail, if Intel® AMT is connected to the associated Access Point.</li> <li>8. Open the Web UI on the SUT from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li> <li>9. Turn <b>on</b> the radio of the second Access Point registered with Intel® AMT.</li> <li>10. Wait <b>1 minute</b>.</li> <li>11. Turn <b>off</b> the radio of the Access Point that the SUT is <b>currently</b> connected to. The Intel® AMT wireless network interface should shift to the second Access Point, which was enabled in step 9.</li> <li>12. Wait <b>1 minute</b>.</li> <li>13. Open the Web UI from the SUT locally (refer <a href="#">Section 6.3.2</a> for details) and confirm Intel® AMT wireless has a network IP address on the <i>System Status</i> page. Ensure to note the new wireless IP address assigned by the second Access Point <b>may be</b> different than the one assigned by the first Access Point.</li> <li>14. Open the Web UI on the SUT from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li> <li>15. In the Host OS device manager on the SUT, re-enable the Host WLAN driver.</li> <li>16. Restore the radio states of the Access Points as they were before testing started.</li> </ol>
Pass Criteria	The test passes, if Intel® AMT responds over the wireless network after the Access Point profile switch has occurred.
References	For details on Intel® AMT Web UI access or Wireless Setting configuration, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .



## 6.3.9 Intel® ME Control Mode Operation after Host Profile Synchronization

ID	CS_006																			
Title	Intel® ME Control Mode Operation after Host Profile Synchronization																			
Requirement	Mandatory - Exempt for systems without Intel® AMT WLAN support																			
System	<table><tr><th colspan="2">Form Factor</th><th>System Power Model</th><th colspan="2">Intel® AMT Network Interface</th></tr><tr><td><input checked="" type="checkbox"/> Desktop</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input type="checkbox"/> LAN</td><td><input type="checkbox"/> Either Used</td></tr><tr><td><input checked="" type="checkbox"/> Mobile</td><td></td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input checked="" type="checkbox"/> WLAN</td><td><input type="checkbox"/> Not Used</td></tr></table>					Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Not Used
Form Factor		System Power Model	Intel® AMT Network Interface																	
<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input type="checkbox"/> Either Used																
<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Not Used																
Method	Automated by Intel® PETS with test operator interaction																			
Description	Intel® AMT connects over wireless LAN in Sx, when the Access Point profile is synchronized from the Host OS via Intel® PROSet software.																			
Objective	Verify that the Intel® AMT connection over wireless LAN in Sx occurs, when after the Host WLAN driver is operational and connected to an Access Point, and the Access Point profile is synchronized via Intel® PROSet software.																			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should <b>not</b> be provisioned. Intel® AMT wireless should <b>not</b> be configured or operational.</p> <p>If the SUT is already configured, unprovision the SUT to clear the wireless network configuration completely; this <b>also</b> includes clearing any synchronized Access Point profiles from the Host OS, which may have been configured via the Intel® PROSet software in any prior test run.</p>																			
Procedure	<ol style="list-style-type: none"><li>If Intel® AMT has already been provisioned:<ol style="list-style-type: none"><li>Restart the SUT.</li><li>Enter Intel® MEBX and perform a full unprovision, and then</li><li>Boot the SUT to S0/MeOn with Host OS running.</li></ol></li><li>Restart the SUT, and boot into Intel® MEBX:<ol style="list-style-type: none"><li>Provision Intel® AMT.</li><li>Set the active power package to Power Package 2 (Intel® ME on in S0, Intel® ME wake in S3, S4-S5).</li><li>Boot back to the Host OS, and then</li></ol></li><li>Run the Intel® MSS to allow fast access to the Web UI locally.</li><li>Verify that the Host WLAN driver is enabled.</li><li>Enable Profile sync by executing the WSMAN command on the SUT local host interface.</li><li>Configure the Host OS to connect to an Access Point, which supports either Wi-Fi Protected Access Pre-Shared Key (WPA-PSK) or Robust Security Network Pre-Shared Key (RSN-PSK) authentication, and either Temporal Key Integrity Protocol (TKIP) or Counter CBC-MAC Protocol (CCMP) encryption.</li><li>Open the Web UI from the SUT locally (refer Section 6.3.2 for details) and<ol style="list-style-type: none"><li>Open the Wireless Settings page, and under Wireless Management select 'Enabled in S0, Sx/AC' (Link Policy 3),and click Submit, and then</li><li>Wait <b>1 minute</b> for the changes to apply, then confirm Intel® AMT wireless has a network IP address on the System Status page.</li></ol></li><li>Shutdown the SUT to S5/MeOn via the Host OS.</li><li>Open the Web UI on the SUT remotely from the management console via the wireless interface (refer to <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li><li>Unprovinoin the system.</li></ol>																			
Pass Criteria	The test passes, if Intel® AMT responds over the wireless network, when the Intel® ME controls the WLAN NIC in Intel® ME Control mode.																			
References	For details on Intel® AMT Web UI access or Wireless Setting configuration, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> . For details on provisioning Intel® AMT via Intel® MEBX, refer to the <i>Intel® Management Engine BIOS Extension User's Guide</i> .																			





### 6.3.10 Intel® ME Control and Host Control Mode Toggle

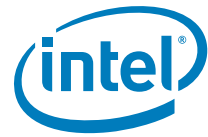
<b>ID</b>	<b>CS_007</b>				
<b>Title</b>	Intel® ME Control and Host Control Mode Toggle				
<b>Requirement</b>	Mandatory - Exempt for systems without Intel® AMT WLAN support				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS				
<b>Description</b>	Intel® AMT connects over wireless LAN in S0, when the Host WLAN driver is disabled or not installed.				
<b>Objective</b>	Verify that the Intel® AMT connection over wireless LAN in S0, when moving from Intel® ME Control mode to Host Control mode and back.				
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer <a href="#">Section 6.3.3</a> for details).				
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Wait <b>2 minutes</b> before starting the test after the Host OS loads to allow entry into Host Control mode.</li> <li>2. Open the Web UI from the SUT locally (refer <a href="#">Section 6.3.2</a> for details) and confirm Intel® AMT wireless has a network IP address on the <i>System Status</i> page.</li> <li>3. Open the Host OS device manager on the SUT and disable the Host WLAN driver.</li> <li>4. Wait <b>1 minute</b> as the SUT moves into <b>Intel® ME Control</b> mode.</li> <li>5. Open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and locate the Intel® AMT wireless network IPv4 address on the <i>System Status</i> page. The IPv4 address assigned to Intel® AMT, while in Intel® ME Control mode.</li> <li>6. In the Host OS device manager on the SUT, re-enable the Host WLAN driver.</li> <li>7. Wait <b>1 minute</b> as the SUT moves into <b>Host Control</b> mode.</li> <li>8. Again, open the Web UI on the SUT remotely from the management console via the wireless interface and confirm the Intel® AMT wireless network IPv4 address on the <i>System Status</i> page is the same in Host Control mode as it was in Intel® ME control mode. In the case of IPv6, the addresses may be different and should not be used for comparison.</li> <li>9. In the Host OS device manager on the SUT, disable the Host WLAN driver again.</li> <li>10. Wait <b>1 minute</b> as the SUT moves back into <b>Intel® ME Control</b> mode.</li> <li>11. Finally, open the Web UI on the SUT remotely from the management console via the wireless interface and locate the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li> <li>12. In the Host OS device manager on the SUT, re-enable the Host WLAN driver one final time.</li> </ol>				
<b>Pass Criteria</b>	The test passes, if Intel® AMT responds over the wireless network in both Intel® ME Control mode and Host Control mode.				
<b>References</b>	For details on Intel® AMT Web UI access or Wireless Setting configuration, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .				

### 6.3.11 Software Radio Frequency Kill (RF-Kill)

<b>ID</b>	<b>CS_008</b>				
<b>Title</b>	Software Radio Frequency Kill (RF-Kill)				
<b>Requirement</b>	Mandatory - Exempt for systems without Intel® AMT WLAN support or software RF-Kill				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used



ID	CS_008
Method	Automated by Intel® PETS with test operator interaction
Description	Intel® AMT will not connect over wireless LAN in S0, when software RF-Kill is active, regardless of Host Control or Intel® ME Control mode SUT operation.
Objective	Verify that the Intel® AMT does not connect over wireless LAN in S0 in either Host Control or Intel® ME Control mode, when software RF-kill is active.
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer <a href="#">Section 6.3.3</a> for details).
Procedure	<ol style="list-style-type: none"><li>1. Wait <b>2 minutes</b> before starting the test after the Host OS loads to allow entry into Host Control mode.</li><li>2. Open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li><li>3. Disable wireless connectivity on the SUT by applying software RF-Kill.</li><li>4. Reload the Web UI from the SUT on the management console and confirm that Intel® AMT wireless network connectivity is not available.</li><li>5. Open the Host OS device manager on the SUT and disable the Host WLAN driver.</li><li>6. Wait <b>1 minute</b> as the SUT moves into Intel® ME Control mode.</li><li>7. Reload the Web UI from the SUT on the management console and confirm that Intel® AMT wireless network connectivity is not available.</li><li>8. In the Host OS device manager on the SUT, re-enable the Host WLAN driver.</li><li>9. Enable wireless connectivity on the SUT by canceling software RF-Kill.</li></ol>
Pass Criteria	The test passes, if Intel® AMT does not respond over the wireless network, when the SUT is in either Host Control or Intel® ME Control mode with software RF-kill applied
References	For details on Intel® AMT Web UI access, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .



### 6.3.12 Hardware Radio Frequency Kill (RF-Kill)

ID	CS_009														
Title	Hardware Radio Frequency Kill (RF-Kill)														
Requirement	Mandatory - Exempt for systems without Intel® AMT WLAN support or hardware RF-Kill														
System	<table><tr><th colspan="2">Form Factor</th><th>System Power Model</th><th colspan="2">Intel® AMT Network Interface</th></tr><tr><td><input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN</td><td><input type="checkbox"/> Either Used <input type="checkbox"/> Not Used</td></tr></table>					Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Form Factor		System Power Model	Intel® AMT Network Interface												
<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used											
Method	Automated by Intel® PETS with test operator interaction														
Description	Intel® AMT will not connect over wireless LAN in S0, when hardware RF-Kill is active, regardless of Host Control or Intel® ME Control mode SUT operation.														
Objective	Verify that the Intel® AMT does not connect over wireless LAN in S0 in either Host Control or Intel® ME Control mode, when hardware RF-kill is active.														
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer <a href="#">Section 6.3.3</a> for details).														
Procedure	<ol style="list-style-type: none"><li>1. Wait <b>2 minutes</b> before starting the test after the Host OS loads to allow entry into Host Control mode.</li><li>2. Open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li><li>3. Disable wireless connectivity on the SUT by applying hardware RF-Kill.</li><li>4. Reload the Web UI from the SUT on the management console and confirm that Intel® AMT wireless network connectivity is not available.</li><li>5. Open the Host OS device manager on the SUT and disable the Host WLAN driver.</li><li>6. Wait <b>1 minute</b> as the SUT moves into Intel® ME Control mode.</li><li>7. Reload the Web UI from the SUT on the management console and confirm that Intel® AMT wireless network connectivity is not available.</li><li>8. In the Host OS device manager on the SUT, re-enable the Host WLAN driver.</li><li>9. Enable wireless connectivity on the SUT by cancelling hardware RF-Kill.</li></ol>														
Pass Criteria	The test passes, if Intel® AMT does not respond over the wireless network, when the SUT is in either Host Control or Intel® ME Control mode with hardware RF-kill applied.														
References	For details on Intel® AMT Web UI access, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .														

### 6.3.13 Software and Hardware Radio Frequency Kill (RF-Kill)

ID	CS_010				
Title	Software and Hardware Radio Frequency Kill (RF-Kill)				
Requirement	Mandatory - Exempt for systems without Intel® AMT WLAN support, or both SW and HW RF-Kill				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS with test operator interaction				
Description	Intel® AMT will not connect over wireless LAN in S0, when software and hardware RF-Kill are active, regardless of Host Control or Intel® ME Control mode SUT operation.				
Objective	Verify that the Intel® AMT does not connect over wireless LAN in S0 in either Host Control or Intel® ME Control mode, when software and hardware RF-kill are active.				



ID	CS_010
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Intel® AMT wireless should be configured and operational (refer <a href="#">Section 6.3.3</a> for details).
Procedure	<ol style="list-style-type: none"><li>1. Wait <b>2 minutes</b> before starting the test after the Host OS loads to allow entry into Host Control mode.</li><li>2. Open the Web UI on the SUT remotely from the management console via the wireless interface (refer <a href="#">Section 6.3.2</a> for details) and confirm the Intel® AMT wireless network IP address on the <i>System Status</i> page.</li><li>3. Disable wireless connectivity on the SUT by applying <b>both</b> software and hardware RF-Kill.</li><li>4. Open the Host OS device manager on the SUT and disable the Host WLAN driver.</li><li>5. Wait <b>1 minute</b> as the SUT moves into Intel® ME Control mode.</li><li>6. Reload the Web UI from the SUT on the management console and confirm that Intel® AMT wireless network connectivity is not available.</li><li>7. Cancel the hardware RF-Kill setting, leaving software RF-kill still applied.</li><li>8. Reload the Web UI from the SUT on the management console and confirm that Intel® AMT wireless network connectivity remains unavailable.</li><li>9. In the Host OS device manager on the SUT, re-enable the Host WLAN driver.</li><li>10. Enable wireless connectivity on the SUT by canceling software RF-Kill.</li></ol>
Pass Criteria	The test passes, if Intel® AMT does not respond over the wireless network with both software and hardware RF-kill applied.
References	For details on Intel® AMT Web UI access, refer to the <i>Intel® AMT OEM Web User Interface Guide</i> .

## 6.4 Intel® ME Firmware Update and Partial Firmware Update

The section serves as a checklist for the environment setup and testing of Intel® ME firmware update and partial (partition) firmware update feature support.

### 6.4.1 Tools for Testing

A formatted USB Key, the Intel® FWUpdLcl and Intel® MEInfo tools from the Intel® ME firmware kit.



## 6.4.2 Intel® ME Firmware Update

ID	CS_020																			
Title	Intel® ME Firmware Update																			
Requirement	Mandatory - Exempt when upgrade/downgrade support is not yet available in firmware																			
System	<table><tr><td colspan="2">Form Factor</td><td>System Power Model</td><td colspan="2">Intel® AMT Network Interface</td></tr><tr><td><input checked="" type="checkbox"/> Desktop</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input type="checkbox"/> LAN</td><td><input type="checkbox"/> Either Used</td></tr><tr><td><input checked="" type="checkbox"/> Mobile</td><td></td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input type="checkbox"/> WLAN</td><td><input checked="" type="checkbox"/> Not Used</td></tr></table>					Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Not Used
Form Factor		System Power Model	Intel® AMT Network Interface																	
<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input type="checkbox"/> Either Used																
<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Not Used																
Method	Automated by Intel® PETS with test operator interaction																			
Description	Firmware Update settings, as set by the Intel® FIT tool, allow update to the firmware.																			
Objective	Verify that the Intel® ME firmware can be updated.																			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running.																			
Procedure	<div>1. Enter a formatted USB Key into the management console.</div> <div>2. Browse to an update firmware image on the management console. This may be the latest firmware released by Intel, or an earlier version of the firmware than the firmware currently loaded on the SUT.</div> <div>3. Place the selected update firmware image on the USB Key.</div> <div>4. Move the USB Key to the SUT.</div> <div>5. Run the Intel® FWUpdLcl tool on the SUT with the -save option, to save the current firmware image to the USB Key.</div> <div>6. Extract the current version of the Intel® ME firmware, using the Intel® MEInfo tool.</div> <div>7. Run the Intel® FWUpdLcl tool on the SUT to update the firmware to the image on the USB Key.</div> <div>8. Restart the SUT.</div> <div>9. Verify the SUT has booted to the Host OS.</div> <div>10. Extract the new version of the Intel® ME firmware using Intel® MEInfo and ensure that it has changed from the original firmware version.</div> <div>11. Verify that the new firmware version is correct.</div> <div>12. Run the Intel® FWUpdLcl tool on the SUT to restore the firmware to the original image extracted earlier from the SUT.</div> <div>13. Restart the SUT.</div> <div>14. Verify the SUT has booted to the Host OS.</div> <div>15. Extract the new version of the Intel® ME firmware using Intel® MEInfo, and ensure that it has been restored to the original firmware version.</div>																			
Pass Criteria	<div>The test passes, if the firmware update is successful, and the original firmware can be restored for each of the following conditions:</div> <div><div><div>Update to newer version of firmware than what is installed on the SUT.</div><div>Downgrade to an older version of firmware than what is installed on the SUT.</div><div>It is not allowed to downgrade to an older version of firmware with lower VCN.</div></div><div>Depending on the Intel® ME development milestone at which this test is being executed, it may not be possible to fully execute this test with available firmware due to upgrade / downgrade firmware compatibility limitations. In this case, the results for this test become 'Not Available' or 'N/A' untill, such time at which suitable firmware images become available to allow full execution of this test.</div></div>																			
References	For details on Intel® ME firmware tools, refer to the Intel® ME System Tools User Guide.																			

## 6.4.3 Intel® ME Firmware Partition Update for Secure Output Locale

<b>ID</b>	<b>CS_021</b>
<b>Title</b>	Intel® ME Firmware Partition Update for Secure Output Locale
<b>Requirement</b>	Mandatory



<b>ID</b>	<b>CS_021</b>				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input checked="" type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS with test operator interaction				
<b>Description</b>	This is a test of the Secure Output sprite locale update performed by Local Manageability Service (LMS) on a Microsoft* Windows platform.				
<b>Objective</b>	Verify that the Secure Output localization partition in Intel® ME firmware region is correctly updated with the locale resources matching those specified by the end user in Intel® MSS.				
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running.				
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Open the Intel® MSS Application;<ol style="list-style-type: none"><li>a. Select the <i>Advanced</i> tab, and</li><li>b. Change the selected Secure Output message language.</li></ol></li><li>2. Trigger a Secure Output event (i.e., User Consent confirmation request via KVM, SOL, or Storage Redirection) and verify that the message appears in the selected language. Intel® PETS in combination with one of the Intel® AMT Redirection tests with User Consent enabled can be used to facilitate this test step.</li><li>3. Use the Intel® MSS to return the Secure Output message language to the setting selected before the test was run.</li></ol>				
<b>Pass Criteria</b>	The test passes, if the Secure Output message is displayed in the language chosen in the Intel® MSS.				
<b>References</b>	For details on Intel® MSS settings, refer to the <i>Intel® Management and Security Status User's Guide</i> .				



## 6.4.4 Intel® ME Firmware Partition Update for WLAN µCode

ID	CS_022				
Title	Intel® ME Firmware Partition Update for WLAN µCode				
Requirement	Mandatory - Exempt where only one kind of WLAN NIC is supported on the platform				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS with test operator interaction				
Description	This is a test of the WLAN uCode (microcode) update performed by Local Manageability Service (LMS) on a Microsoft* Windows platform.				
Objective	Verify that the WLAN uCode partition in Intel® ME firmware region is correctly updated with the uCode resources matching those required for the installed WLAN NIC.				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running.				
Procedure	<ol style="list-style-type: none"> <li>1. Shutdown the SUT to G3, and replace the WLAN NIC with a different WLAN NIC, which also supports Intel® vPro™ Technology.</li> <li>2. Boot the SUT with the new WLAN card.</li> <li>3. Open the Intel® MSS and verify that an event is created indicating a partition update occurred.</li> <li>4. Ensure that basic Intel® AMT wireless connectivity is functional. The Intel® AMT wireless network tests relying on Web UI access at the beginning of this chapter can be used to facilitate this test step.</li> <li>5. Shutdown the SUT to G3, and replace the WLAN NIC with the original WLAN NIC used at the start of this test.</li> </ol>				
Pass Criteria	The test passes, if the event indicating the WLAN uCode partition update occurred as seen with Intel® MSS, and Intel® AMT connectivity is confirmed using the alternate WLAN NIC.				
References	For details on WLAN uCode update, refer to the <i>Intel® ME System Tools User Guide</i> .				

## 6.5 USB Key Based Configuration

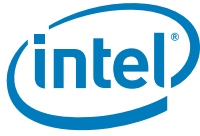
The section serves as a checklist for the environment setup and testing of Intel® ME firmware configuration via USB Key feature support.

### 6.5.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Windows\* supported by Intel® PETS, and the SUT should have a version of Windows\* supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one HDD.

#### Tools for Testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- System Under Test (SUT): Should be connected to Intel® APS 3. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.



- USB Keys formatted to FAT16. It is recommended to test also with a FAT32 USB Key but it is not mandatory.

If using Intel® APS 3, Intel® PETS can make use of automation using the USB Key Switching feature. To use this feature, ensure that the USB feature is connected to the management console and SUT as follows:

- **Intel® APS 3 to SUT:** USB cable from 'USB 1 out' of the Intel® APS 3 unit to the SUT.
- **Intel® APS 3 to management console:** USB cable from 'USB 2 out' of the Intel® APS 3 unit to the management console.
- Insert a USB Key to the 'USB SW' port on the APS.

The system under test is to be un-configured at start of each test, unless otherwise stated.





## 6.5.2 USB Key File Version 2.1 with Consumable Record

<b>ID</b>	<b>CS_030</b>																		
<b>Title</b>	USB Key File Version 2.1 with Consumable Record																		
<b>Requirement</b>	Mandatory																		
<b>System</b>	<table border="1"> <thead> <tr> <th colspan="2">Form Factor</th><th>System Power Model</th><th colspan="2">Intel® AMT Network Interface</th></tr> </thead> <tbody> <tr> <td><input checked="" type="checkbox"/> Desktop</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input type="checkbox"/> LAN</td><td><input checked="" type="checkbox"/> Either Used</td></tr> <tr> <td><input checked="" type="checkbox"/> Mobile</td><td></td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input type="checkbox"/> WLAN</td><td><input type="checkbox"/> Not Used</td></tr> </tbody> </table>				Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used
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<b>Method</b>	Automated by Intel® PETS with test operator interaction																		
<b>Description</b>	Validate that the BIOS can recognize USB Key file format version 2.1, and pass a record to the Intel® MEBX.																		
<b>Objective</b>	Verify that the BIOS is able to read the USB Key file format version 2.1, process it, and correctly mark it as read.																		
<b>Setup</b>	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked 'USB SW' <b>before</b> starting the test.																		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</li> <li>2. If the Intel® APS 3 is used, the Intel® PETS performs necessary calibrations to determine, which Intel® APS 3 USB port is connected to the SUT and which is connected to the management console.</li> <li>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</li> <li>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li> <li>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured to <b>enable</b> USB Key provisioning are dependent on Intel® APS usage: <ul style="list-style-type: none"> <li>— If the Intel® APS <b>is</b> used, Intel® PETS checks, if the Intel® ME is configured to perform un-configure operation on RTC clear: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME is un-configured by RTC-clear, Intel® PETS ensures Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, before booting the SUT to Host OS.</li> <li>ii. In the case that Intel® ME is <b>not</b> un-configured by RTC-clear, the test operator is prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> <li>— If the Intel® APS <b>is not</b> used, Intel® PETS prompts the test operator in one of the following two ways: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME is un-configured by RTC-clear, then the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> <li>ii. In the case that Intel® ME is <b>not</b> un-configured by RTC-clear, the test operator is prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> </ul> </li> </ol>																		

ID	CS_030
Procedure (continued)	<p>7. The following step(s) are dependent on Intel® APS 3 usage:</p> <ul style="list-style-type: none"> <li>— If used, the Intel® PETS switches the USB Key to the management console.</li> <li>— If <b>not</b> used, the Intel® PETS prompts the test operator to insert a formatted USB Key into the management console.</li> </ul> <p>8. Place a file called Setup.bin on the USB Key, containing a single consumable record (USB file version 2.1) including the following configuration information:</p> <ol style="list-style-type: none"> <li>Intel® MEBX password (both old and new) If Intel® PETS is used, the password, which is entered in the SUT configuration for the Intel® ME password shall be used as the new password.</li> <li>FQDN "provisionServer.compliance.com" (to update ConfigServerFQDN)</li> <li>Certificate Authority (CA) hash</li> </ol> <p>9. The following step(s) are dependent on Intel® APS 3 usage:</p> <ul style="list-style-type: none"> <li>— If used, Intel® PETS switches the USB Key from the management console to the SUT.</li> <li>— If <b>not</b> used, Intel® PETS prompts the test operator to switch the USB Key from the management console to the SUT manually.</li> </ul> <p>10. Request the test operator to acknowledge the provisioning prompt on the SUT during the next boot. The system should continue booting to Host OS.</p> <p>11. Restart the SUT to the base state of S0/MeOn. The test operator should acknowledge the provisioning prompt during the boot process and the system should continue booting to Host OS.</p> <p>12. Verify the SUT has booted to Host OS.</p> <p>13. On the SUT, confirm the FQDN and CA hash are passed correctly to Intel® ME firmware.</p> <p>14. Restart the SUT to the base state of S0/MeOn.</p> <p>15. Verify the SUT has booted to Host OS.</p> <p>16. Request the test operator to confirm that SUT has booted to Host OS with no provisioning prompts during the boot process.</p> <p>17. The following step(s) are dependent on Intel® APS 3 usage:</p> <ul style="list-style-type: none"> <li>— If used, the Intel® PETS switches the USB Key from the SUT to the management console.</li> <li>— If <b>not</b> used, the Intel® PETS prompts the test operator to switch the USB Key from the SUT to the management console manually.</li> </ul> <p>18. Read the Setup.bin from USB Key and verify that the file is updated correctly to erase the used configuration record.</p>
Pass Criteria	The test passes, if the SUT is configured with USB Key file format version 2.1. The configuration record is erased from the USB Key, and SUT boots normally afterwards.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .



### 6.5.3 USB Key File Version 2.1 with Non-Consumable Record

<b>ID</b>	<b>CS_031</b>																		
<b>Title</b>	USB Key File Version 2.1 with Non-Consumable Record																		
<b>Requirement</b>	Mandatory																		
<b>System</b>	<table border="1"> <thead> <tr> <th colspan="2">Form Factor</th><th>System Power Model</th><th colspan="2">Intel® AMT Network Interface</th></tr> </thead> <tbody> <tr> <td><input checked="" type="checkbox"/> Desktop</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input type="checkbox"/> LAN</td><td><input checked="" type="checkbox"/> Either Used</td></tr> <tr> <td><input checked="" type="checkbox"/> Mobile</td><td></td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input type="checkbox"/> WLAN</td><td><input type="checkbox"/> Not Used</td></tr> </tbody> </table>				Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used
Form Factor		System Power Model	Intel® AMT Network Interface																
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<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used															
<b>Method</b>	Automated by Intel® PETS with test operator interaction																		
<b>Description</b>	Validate that the BIOS can recognize USB Key file format version 2.1, and pass a record to the Intel® MEBX.																		
<b>Objective</b>	Verify that the BIOS is able to read the USB Key file format version 2.1, process it, and correctly mark it as read if it is non-consumable.																		
<b>Setup</b>	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked 'USB SW' <b>before</b> starting the test.																		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</li> <li>2. If the Intel® APS 3 is used, the Intel® PETS performs necessary calibrations to determine, which Intel® APS 3 USB port is connected to the SUT and is connected to the management console.</li> <li>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</li> <li>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li> <li>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured to <b>enable</b> USB Key provisioning are dependent on Intel® APS usage: <ol style="list-style-type: none"> <li>a. If the Intel® APS <b>is</b> used, Intel® PETS checks, if the Intel® ME is configured to perform un-configure operation on RTC clear: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME is un-configured by RTC-clear, Intel® PETS ensures Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, before booting the SUT to Host OS.</li> <li>ii. In the case that Intel® ME is <b>not</b> un-configured by RTC-clear, the test operator will be prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> <li>b. If the Intel® APS <b>is not</b> used, Intel® PETS prompts the test operator in one of the following two ways: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME is un-configured by RTC-clear, the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> <li>ii. In the case that Intel® ME is <b>not</b> un-configured by RTC-clear, the test operator will be prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> </ol> </li> </ol>																		

ID	CS_031
Procedure (continued)	<p>7. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Reboot the SUT and enter the Intel® MEBX, then</li> <li>From the Intel® MEBX menu, change the default 'admin' password to 'Admin!98' (or if using Intel® PETS, the same Intel® ME password, which is provided in the Intel® PETS SUT configuration), and then</li> <li>Exit the Intel® MEBX menu and allow the system to boot to Host OS.</li> </ol> <p>8. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, the Intel® PETS switches the USB Key to the management console.</li> <li>If <b>not</b> used, the Intel® PETS prompts the test operator to insert a formatted USB Key into the management console.</li> </ol> <p>9. Place a file called Setup.bin on the USB Key, containing a single <b>non</b>-consumable record (USB file version 2.1) including the following configuration information:</p> <ol style="list-style-type: none"> <li>Intel® MEBX password: "Admin!98" (same password for both old and new) If Intel® PETS is used, the same password, which is entered in the SUT configuration for the Intel® ME password that shall be used for both the old and new passwords.</li> <li>FQDN "<a href="https://provisionServer.compliance.com">provisionServer.compliance.com</a>" (to update ConfigServerFQDN)</li> <li>Certificate Authority (CA) hash</li> </ol> <p>10. The following step(s) are dependent on Intel® APS 3 usage:</p> <ul style="list-style-type: none"> <li>If used, Intel® PETS switches the USB Key from the management console to the SUT.</li> <li>If <b>not</b> used, Intel® PETS prompts the test operator to switch the USB Key from the management console to the SUT manually.</li> </ul> <p>11. Request the test operator to acknowledge the provisioning prompt on the SUT during the next boot. The system should continue booting to Host OS.</p> <p>12. Restart the SUT to the base state of S0/MeOn. The test operator should acknowledge the provisioning prompt during the boot process and the system should continue booting to Host OS.</p> <p>13. Verify the SUT has booted to Host OS.</p> <p>14. On the SUT, confirm the FQDN and CA hash are passed correctly to Intel® ME firmware.</p> <p>15. Request the test operator to acknowledge the provisioning prompt on the SUT during the next boot. The system should continue booting to Host OS.</p> <p>16. Restart the SUT to the base state of S0/MeOn. The test operator should acknowledge the provisioning prompt during the boot process and the system should continue booting to Host OS.</p> <p>17. Verify the SUT has booted to Host OS.</p> <p>18. Request the test operator to confirm that a provisioning prompt is presented on the SUT.</p> <p>19. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, the Intel® PETS switches the USB Key from the SUT to the management console.</li> <li>If <b>not</b> used, the Intel® PETS prompts the test operator to switch the USB Key from the SUT to the management console manually.</li> </ol> <p>20. Read the Setup.bin from USB Key and verify that the file is updated correctly to allow re-use of the configuration record, and the file was not changed by comparing the file content and header before and after the configuration.</p>
Pass Criteria	The test passes, if the SUT is configured with USB Key file format version 2.1, and correctly handles non-consumable records.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .



## 6.5.4 USB Key File Version 3 with Consumable Record

<b>ID</b>	<b>CS_032</b>																		
<b>Title</b>	USB Key File Version 3 with Consumable Record																		
<b>Requirement</b>	Mandatory																		
<b>System</b>	<table border="1"> <thead> <tr> <th colspan="2">Form Factor</th><th>System Power Model</th><th colspan="2">Intel® AMT Network Interface</th></tr> </thead> <tbody> <tr> <td><input checked="" type="checkbox"/> Desktop</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input type="checkbox"/> LAN</td><td><input checked="" type="checkbox"/> Either Used</td></tr> <tr> <td><input checked="" type="checkbox"/> Mobile</td><td></td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input type="checkbox"/> WLAN</td><td><input type="checkbox"/> Not Used</td></tr> </tbody> </table>				Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used
Form Factor		System Power Model	Intel® AMT Network Interface																
<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used															
<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used															
<b>Method</b>	Automated by Intel® PETS with test operator interaction																		
<b>Description</b>	<p>Validate that the BIOS can recognize USB file format version 3, and pass a record to the Intel® MEBX.</p> <p>The term "Version 3" does not refer to USB 3.0. It refers to the 3<sup>rd</sup> revision USB configuration file format introduced in with Intel® ME 6 platforms.</p>																		
<b>Objective</b>	Verify that the BIOS is able to read the USB Key file format version 3, process it, and correctly mark it as read.																		
<b>Setup</b>	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked "USB SW" <b>before</b> starting the test.																		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</li> <li>2. If the Intel® APS 3 is used, the Intel® PETS will perform necessary calibrations to determine which Intel® APS 3 USB port is connected to the SUT and which is connected to the management console.</li> <li>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</li> <li>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li> <li>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured to <b>enable</b> USB Key provisioning are dependent on Intel® APS usage: <ol style="list-style-type: none"> <li>a. If the Intel® APS <b>is</b> used, Intel® PETS will check, if the Intel® ME has been configured to perform un-configure operation on RTC clear: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, Intel® PETS will ensure Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, before booting the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> <li>b. If the Intel® APS is not used, Intel® PETS will prompt the test operator in one of the following two ways: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> </ol> </li> </ol>																		



ID	CS_032
Procedure (continued)	<ol style="list-style-type: none"> <li>7. The following step(s) are dependent on Intel® APS 3 usage:               <ol style="list-style-type: none"> <li>a. If used, the Intel® PETS will switch the USB Key to the management console.</li> <li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to insert a formatted USB Key into the management console.</li> </ol> </li> <li>8. Place a file called Setup.bin on the USB Key, containing a single consumable record (USB file version 3) including the following configuration information:               <ol style="list-style-type: none"> <li>a. Intel® MEBX password (both old and new)                   <ul style="list-style-type: none"> <li>If Intel® PETS is used, the password, which was entered in the SUT configuration for the Intel® ME password shall be used as the new password.</li> </ul> </li> <li>b. FQDN "<a href="https://provisionServer.compliance.com">provisionServer.compliance.com</a>" (to update ConfigServerFQDN)</li> <li>c. Certificate Authority (CA) hash</li> </ol> </li> <li>9. The following step(s) are dependent on Intel® APS 3 usage:               <ol style="list-style-type: none"> <li>a. If used, Intel® PETS will switch the USB Key from the management console to the SUT.</li> <li>b. If not used, Intel® PETS will prompt the test operator to switch the USB Key from the management console to the SUT manually.</li> </ol> </li> <li>10. Request the test operator to acknowledge the provisioning prompt on the SUT during the next boot. The system should continue booting to Host OS.</li> <li>11. Restart the SUT to the base state of S0/MeOn. The test operator should acknowledge the provisioning prompt during the boot process and the system should continue booting to Host OS.</li> <li>12. Verify the SUT has booted to Host OS.</li> <li>13. On the SUT, confirm the FQDN and CA hash were passed correctly to Intel® ME firmware.</li> <li>14. Restart the SUT to the base state of S0/MeOn.</li> <li>15. Verify the SUT has booted to Host OS.</li> <li>16. Request the test operator to confirm that SUT has booted to Host OS with no provisioning prompts during the boot process.</li> <li>17. The following step(s) are dependent on Intel® APS 3 usage:               <ol style="list-style-type: none"> <li>a. If used, the Intel® PETS will switch the USB Key from the SUT to the management console.</li> <li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to switch the USB Key from the SUT to the management console manually.</li> </ol> </li> <li>18. Read the Setup.bin from USB Key and verify that the file was updated correctly to erase the used configuration record.</li> </ol>
Pass Criteria	The test passes, if the SUT is configured with USB Key file format version 3. The configuration record is erased from the USB Key, and SUT boots normally afterwards.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .



## 6.5.5 USB Key File Version 4 with Consumable Record

<b>ID</b>	<b>CS_033</b>																		
<b>Title</b>	USB Key File Version 4 with Consumable Record																		
<b>Requirement</b>	Mandatory																		
<b>System</b>	<table border="1"> <thead> <tr> <th colspan="2">Form Factor</th><th>System Power Model</th><th colspan="2">Intel® AMT Network Interface</th></tr> </thead> <tbody> <tr> <td><input checked="" type="checkbox"/> Desktop</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input type="checkbox"/> LAN</td><td><input checked="" type="checkbox"/> Either Used</td></tr> <tr> <td><input checked="" type="checkbox"/> Mobile</td><td></td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input type="checkbox"/> WLAN</td><td><input type="checkbox"/> Not Used</td></tr> </tbody> </table>				Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used
Form Factor		System Power Model	Intel® AMT Network Interface																
<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used															
<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used															
<b>Method</b>	Automated by Intel® PETS with test operator interaction																		
<b>Description</b>	Validate that the BIOS can recognize USB file format version 4, and pass a record to the Intel® MEBX.																		
<b>Objective</b>	Verify that the BIOS is able to read the USB Key file format version 4, process it, and correctly mark it as read.																		
<b>Setup</b>	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked 'USB SW' <b>before</b> starting the test.																		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</li> <li>2. If the Intel® APS 3 is used, the Intel® PETS will perform necessary calibrations to determine which Intel® APS 3 USB port is connected to the SUT and which is connected to the management console.</li> <li>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</li> <li>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li> <li>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured to <b>enable</b> USB Key provisioning are dependent on Intel® APS usage: <ol style="list-style-type: none"> <li>a. If the Intel® APS is used, Intel® PETS will check if the Intel® ME has been configured to perform un-configure operation on RTC clear: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, Intel® PETS will ensure Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, before booting the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> <li>b. If the Intel® APS is not used, Intel® PETS will prompt the test operator in one of the following two ways: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> </ol> </li> </ol>																		



ID	CS_033
Procedure (continued)	<ol style="list-style-type: none"><li>7. The following step(s) are dependent on Intel® APS 3 usage:<ol style="list-style-type: none"><li>a. If used, the Intel® PETS will switch the USB Key to the management console.</li><li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to insert a formatted USB Key into the management console.</li></ol></li><li>8. Place a file called Setup.bin on the USB Key, containing a single consumable record (USB file version 4) including the following configuration information:<ol style="list-style-type: none"><li>a. Intel® MEBX password (both old and new) If Intel® PETS is used, the password which was entered in the SUT configuration for the Intel® ME password shall be used as the new password.</li><li>b. FQDN "<a href="https://provisionServer.compliance.com">provisionServer.compliance.com</a>" (to update ConfigServerFQDN)</li><li>c. Certificate Authority (CA) hash</li></ol></li><li>9. The following step(s) are dependent on Intel® APS 3 usage:<ol style="list-style-type: none"><li>a. If used, Intel® PETS will switch the USB Key from the management console to the SUT.</li><li>b. If <b>not</b> used, Intel® PETS will prompt the test operator to switch the USB Key from the management console to the SUT manually.</li></ol></li><li>10. Request the test operator to acknowledge the provisioning prompt on the SUT during the next boot. The system should continue booting to Host OS.</li><li>11. Restart the SUT to the base state of S0/MeOn. The test operator should acknowledge the provisioning prompt during the boot process and the system should continue booting to Host OS.</li><li>12. Verify the SUT has booted to Host OS.</li><li>13. On the SUT, confirm the FQDN and CA hash were passed correctly to Intel® ME firmware.</li><li>14. Restart the SUT to the base state of S0/MeOn.</li><li>15. Verify the SUT has booted to Host OS.</li><li>16. Request the test operator to confirm that SUT has booted to Host OS with no provisioning prompts during the boot process.</li><li>17. The following step(s) are dependent on Intel® APS 3 usage:<ol style="list-style-type: none"><li>a. If used, the Intel® PETS will switch the USB Key from the SUT to the management console.</li><li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to switch the USB Key from the SUT to the management console manually.</li></ol></li><li>18. Read the Setup.bin from USB Key and verify that the file was updated correctly to erase the used configuration record.</li></ol>
Pass Criteria	The test passes, if the SUT is configured with USB Key file format version 4. The configuration record is erased from the USB Key, and SUT boots normally afterwards.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .





## 6.5.6 USB Key File with Multiple Consumable Records

ID	CS_034				
Title	USB Key with Multiple Consumable Records				
Requirement	Mandatory				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*		<input type="checkbox"/> LAN <input type="checkbox"/> WLAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS with test operator interaction				
Description	Verify that multiple machines can be provisioned using one USB Key. This tests the ability of the BIOS to mark records on the USB Key as used and to process USB file that contains consumed records.				
Objective	Verify that the BIOS will to mark records on the USB Key as used, and also for the BIOS to recover gracefully, when there are no unmarked records on the USB Key.				
Setup	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked “USB SW’ <b>before</b> starting the test.				
Procedure	<div>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</div> <div>2. If the Intel® APS 3 is used, the Intel® PETS will perform necessary calibrations to determine, which Intel® APS 3 USB port is connected to the SUT and which is connected to the management console.</div> <div>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</div> <div>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</div> <div>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</div> <div>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured to <b>enable</b> USB Key provisioning are dependent on Intel® APS usage:<div><div>a. If the Intel® APS <b>is</b> used, Intel® PETS will check, if the Intel® ME has been configured to perform un-configure operation on RTC clear:<div><div>i. In the case that Intel® ME will be un-configured by RTC-clear, Intel® PETS will ensure Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, before booting the SUT to Host OS.</div><div>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</div></div></div><div>b. If the Intel® APS <b>is not</b> used, Intel® PETS will prompt the test operator in one of the following two ways:<div><div>i. In the case that Intel® ME will be un-configured by RTC-clear, the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</div><div>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</div></div></div></div></div>				

ID	CS_034
Procedure (continued)	<p>7. Request the test operator to:</p> <ol style="list-style-type: none"> <li>reboot the SUT and enter the Intel® MEBX, then</li> <li>from the Intel® MEBX menu, change the default 'admin' password to 'Admin!98' (or if using Intel® PETS, the same Intel® ME password, which was provided in the Intel® PETS SUT configuration), and then</li> <li>exit the Intel® MEBX menu and allow the system to boot to Host OS.</li> </ol> <p>8. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, the Intel® PETS will switch the USB Key to the management console.</li> <li>If <b>not</b> used, the Intel® PETS will prompt the test operator to insert a formatted USB Key into the management console.</li> </ol> <p>9. Place a file called SetUp.bin on the USB Key, containing a two consumable records including the following configuration information:</p> <ol style="list-style-type: none"> <li>Intel® MEBX password: "Admin!98" (same password for both old and new) If Intel® PETS is used, the same password which was entered in the SUT configuration for the Intel® ME password shall be used for both the old and new passwords.</li> <li>FQDN "<a href="https://provisionServer.compliance.com">provisionServer.compliance.com</a>" (to update ConfigServerFQDN)</li> <li>Certificate Authority (CA) hash</li> </ol> <p>10. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, Intel® PETS will switch the USB Key from the management console to the SUT.</li> <li>If <b>not</b> used, Intel® PETS will prompt the test operator to switch the USB Key from the management console to the SUT manually.</li> </ol> <p>11. Request the test operator to acknowledge the provisioning prompt on the SUT during the next boot. The system should continue booting to Host OS.</p> <p>12. Restart the SUT to the base state of S0/MeOn. The test operator should acknowledge the provisioning prompt during the boot process and the system should continue booting to Host OS.</p> <p>13. Verify the SUT has booted to Host OS.</p> <p>14. On the SUT, confirm the FQDN and CA hash were passed correctly to Intel® ME firmware.</p> <p>15. Repeat steps 10 through 14.</p> <p>16. Restart the SUT for the third time to the base state of S0/MeOn.</p> <p>17. Verify the SUT has booted to Host OS.</p> <p>18. Request the test operator to confirm that SUT has booted to Host OS with no provisioning prompts during the boot process. There should no longer be any unmarked provisioning records in the USB Key. However, the BIOS should continue gracefully, when all records in the USB Key are marked as used, and the boot should continue to the OS.</p> <p>19. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, the Intel® PETS will switch the USB Key from the SUT to the management console.</li> <li>If <b>not</b> used, the Intel® PETS will prompt the test operator to switch the USB Key from the SUT to the management console manually.</li> </ol> <p>20. Read the Setup.bin from USB Key and verify that the file was updated correctly to erase the used configuration records.</p>
Pass Criteria	The test passes, if the first two (2) configuration attempts succeed, and the final iteration fails. The final iteration should continue to boot to the OS, without configuring the system.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .



## 6.5.7 USB Key File Configuration Process Cancellation

<b>ID</b>	<b>CS_035</b>				
<b>Title</b>	USB Key File Configuration Process Cancellation				
<b>Requirement</b>	Mandatory				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS with test operator interaction				
<b>Description</b>	Validate that BIOS can continue booting the system if the end-user chooses not to continue with the provisioning process.				
<b>Objective</b>	Verify that BIOS can detect provisioning process override and continue to boot.				
<b>Setup</b>	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked "USB SW" <b>before</b> starting the test.				
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</li> <li>2. If the Intel® APS 3 is used, the Intel® PETS will perform necessary calibrations to determine, which Intel® APS 3 USB port is connected to the SUT and which is connected to the management console.</li> <li>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</li> <li>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li> <li>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured to <b>enable</b> USB Key provisioning are dependent on Intel® APS usage: <ol style="list-style-type: none"> <li>a. If the Intel® APS <b>is</b> used, Intel® PETS will check, if the Intel® ME has been configured to perform un-configure operation on RTC clear: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, Intel® PETS will ensure Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, before booting the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> <li>b. If the Intel® APS <b>is not</b> used, Intel® PETS will prompt the test operator in one of the following two ways: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</li> </ol> </li> </ol> </li> </ol>				



ID	CS_035
Procedure (continued)	<ol style="list-style-type: none"><li>7. The following step(s) are dependent on Intel® APS 3 usage:<ol style="list-style-type: none"><li>a. If used, the Intel® PETS will switch the USB Key to the management console.</li><li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to insert a formatted USB Key into the management console.</li></ol></li><li>8. Place a file called Setup.bin on the USB Key, containing a single consumable record (USB file version 4) including the following configuration information:<ol style="list-style-type: none"><li>a. Intel® MEBX password (both old and new) If Intel® PETS is used, the password which was entered in the SUT configuration for the Intel® ME password shall be used as the new password.</li><li>b. FQDN "<a href="https://provisionserver.compliance.com">provisionServer.compliance.com</a>" (to update ConfigServerFQDN)</li><li>c. Certificate Authority (CA) hash</li></ol></li><li>9. The following step(s) are dependent on Intel® APS 3 usage:<ol style="list-style-type: none"><li>a. If used, Intel® PETS will switch the USB Key from the management console to the SUT.</li><li>b. If <b>not</b> used, Intel® PETS will prompt the test operator to switch the USB Key from the management console to the SUT manually.</li></ol></li><li>10. Request the test operator to <b>not</b> acknowledge the provisioning prompt (respond 'No' to the prompt) on the SUT during the next boot. The system should continue booting to Host OS.</li><li>11. Restart the SUT to the base state of S0/MeOn. The test operator should <b>not</b> acknowledge the provisioning prompt (respond 'No' to the prompt) during the boot process and the system should continue booting to Host OS.</li><li>12. Verify the SUT has booted to Host OS.</li><li>13. On the SUT, confirm the SUT <b>remains</b> in <i>Pre-provisioning</i> mode.</li><li>14. The following step(s) are dependent on Intel® APS 3 usage:<ol style="list-style-type: none"><li>a. If used, the Intel® PETS will switch the USB Key from the SUT to the management console.</li><li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to switch the USB Key from the SUT to the management console manually.</li></ol></li><li>15. Read the Setup.bin from USB Key and verify that the file records were <b>not changed</b>.</li></ol>
Pass Criteria	The test passes, if the SUT is not configured and instead boots normally; the file records on the USB Key are not changed.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .



## 6.5.8 USB Key Drive Compliancey

ID	CS_036				
Title	USB Key Drive Compliancey				
Requirement	Mandatory - for FAT16 format, optional for FAT32 formatted USB Keys				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS with test operator interaction				
Description	Validate that the BIOS can recognize USB file format version 4, and pass a record to the Intel® MEBX on various sizes of USB Keys from various vendors formatting with FAT16. Optionally, USB Keys with FAT32 formatting may be validated as well.				
Objective	Verify that the BIOS is able to read the USB Key formatted FAT16 with file format version 4, process it, and correctly mark it as read. It is recommended to test also with FAT32 USB Key				
Setup	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked "USB SW" <b>before</b> starting the test.				
Procedure	<div>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</div> <div>2. If the Intel® APS 3 is used, the Intel® PETS will perform necessary calibrations to determine, which Intel® APS 3 USB port is connected to the SUT and which is connected to the management console.</div> <div>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</div> <div>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</div> <div>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</div> <div>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured to <b>enable</b> USB Key provisioning are dependent on Intel® APS usage:</div> <div><div>a. If the Intel® APS <b>is</b> used, Intel® PETS will check, if the Intel® ME has been configured to perform un-configure operation on RTC clear:</div><div><div>i. In the case that Intel® ME will be un-configured by RTC-clear, Intel® PETS will ensure Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, before booting the SUT to Host OS.</div><div>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</div></div><div>b. If the Intel® APS <b>is not</b> used, Intel® PETS will prompt the test operator in one of the following two ways:</div><div><div>i. In the case that Intel® ME will be un-configured by RTC-clear, the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</div><div>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured to <b>enable</b> USB Key provisioning, and then boot the SUT to Host OS.</div></div></div>				

ID	CS_036
Procedure (continued)	<p>7. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, the Intel® PETS will switch the USB Key to the management console.</li> <li>If <b>not</b> used, the Intel® PETS will prompt the test operator to insert a formatted USB Key into the management console.</li> </ol> <p>8. Place a file called Setup.bin on the USB Key, containing a single consumable record (USB file version 4) including the following configuration information:</p> <ol style="list-style-type: none"> <li>Intel® MEBX password (both old and new)           <p>If Intel® PETS is used, the password which was entered in the SUT configuration for the Intel® ME password shall be used as the new password.</p> </li> <li>FQDN "provisionServer.compliance.com" (to update ConfigServerFQDN)</li> <li>CA (Certificate Authority) hash</li> </ol> <p>9. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, Intel® PETS will switch the USB Key from the management console to the SUT.</li> <li>If <b>not</b> used, Intel® PETS will prompt the test operator to switch the USB Key from the management console to the SUT manually.</li> </ol> <p>10. Request the test operator to acknowledge the provisioning prompt on the SUT during the next boot. The system should continue booting to Host OS.</p> <p>11. Restart the SUT to the base state of S0/MeOn. The test operator should acknowledge the provisioning prompt during the boot process and the system should continue booting to Host OS.</p> <p>12. Verify the SUT has booted to Host OS.</p> <p>13. On the SUT, confirm the FQDN and CA hash were passed correctly to Intel® ME firmware.</p> <p>14. Restart the SUT to the base state of S0/MeOn.</p> <p>15. Verify the SUT has booted to Host OS.</p> <p>16. Request the test operator to confirm that SUT has booted to Host OS with no provisioning prompts during the boot process.</p> <p>17. The following step(s) are dependent on Intel® APS 3 usage:</p> <ol style="list-style-type: none"> <li>If used, the Intel® PETS will switch the USB Key from the SUT to the management console.</li> <li>If <b>not</b> used, the Intel® PETS will prompt the test operator to switch the USB Key from the SUT to the management console manually.</li> </ol> <p>18. Read the Setup.bin from USB Key and verify that the file was updated correctly to erase the used configuration record.</p> <p>19. Prompt the user to repeat this test with different USB Keys from different vendors and with different sizes.</p>
Pass Criteria	The test passes, if the system is configured with each USB Key in FAT16 format, without any errors. If FAT32 format is tested, the system should be configured with the USB Key that was formatted with a FAT32 file system.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .

## 6.5.9 USB Key File Configuration Disabled at Factory Default

ID	CS_037																		
Title	USB Key File Configuration Disabled at Factory Default																		
Requirement	Mandatory																		
System	<table border="1"> <thead> <tr> <th colspan="2">Form Factor</th><th>System Power Model</th><th colspan="2">Intel® AMT Network Interface</th></tr> </thead> <tbody> <tr> <td><input checked="" type="checkbox"/> Desktop</td><td><input checked="" type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input type="checkbox"/> LAN</td><td><input checked="" type="checkbox"/> Either Used</td></tr> <tr> <td><input checked="" type="checkbox"/> Mobile</td><td></td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input type="checkbox"/> WLAN</td><td><input type="checkbox"/> Not Used</td></tr> </tbody> </table>				Form Factor		System Power Model	Intel® AMT Network Interface		<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used
Form Factor		System Power Model	Intel® AMT Network Interface																
<input checked="" type="checkbox"/> Desktop	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input type="checkbox"/> LAN	<input checked="" type="checkbox"/> Either Used															
<input checked="" type="checkbox"/> Mobile		<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> WLAN	<input type="checkbox"/> Not Used															
Method	Automated by Intel® PETS with test operator interaction																		
Description	Validate that BIOS prevents the USB Key provisioning flow with factory default settings.																		
Objective	Verify that USB Key configuration is not possible, when factory default system BIOS settings are applied to the SUT.																		



ID	CS_037
Setup	If running this test using the Intel® APS 3, ensure that a formatted USB Key is inserted into the back of the device in the port marked "USB SW" <b>before</b> starting the test.
Procedure	<ol style="list-style-type: none"> <li>1. Bring the SUT to the base state of S0/MeOn. This is done to ensure that it can be safely shutdown from any prior test.</li> <li>2. If the Intel® APS 3 is used, the Intel® PETS will perform necessary calibrations to determine, which Intel® APS 3 USB port is connected to the SUT and which is connected to the management console.</li> <li>3. For a provisioned SUT, set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). This is done to ensure that the Intel® ME moves to the MeOff state after system shutdown.</li> <li>4. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li> <li>5. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>6. The following step(s) to perform Intel® ME un-configuration and verify the system BIOS is configured with factory default settings are dependent on Intel® APS usage: <ol style="list-style-type: none"> <li>a. If the Intel® APS <b>is</b> used, Intel® PETS will check, if the Intel® ME has been configured to perform un-configure operation on RTC clear: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, Intel® PETS will ensure Intel® ME is not configured by clearing the CMOS, and then prompt the test operator to ensure the system BIOS is configured with factory default settings, before booting the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure the Intel® ME by system-specific means, ensure that the system BIOS is configured with factory default settings, and then boot the SUT to Host OS.</li> </ol> </li> <li>b. If the Intel® APS <b>is not</b> used, Intel® PETS will prompt the test operator in one of the following two ways: <ol style="list-style-type: none"> <li>i. In the case that Intel® ME will be un-configured by RTC-clear, the test operator will be prompted to safely bring the system to G3 state, disconnect the CMOS battery, wait 15 seconds for all electricity to dissipate from the system, reattach the CMOS battery, reattach AC-power, ensure the system BIOS is configured with factory default settings, and then boot the SUT to Host OS.</li> <li>ii. In the case that Intel® ME will <b>not</b> be un-configured by RTC-clear, the test operator will be prompted to manually un-configure Intel® ME by system-specific means, ensure the system BIOS is configured with factory default settings, and then boot the SUT to Host OS.</li> </ol> </li> </ol> </li> <li>7. The following step(s) are dependent on Intel® APS 3 usage: <ol style="list-style-type: none"> <li>a. If used, the Intel® PETS will switch the USB Key to the management console.</li> <li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to insert a formatted USB Key into the management console.</li> </ol> </li> <li>8. Place a file called SetUp.bin on the USB Key, containing a single consumable record (USB file version 4) including the following configuration information: <ol style="list-style-type: none"> <li>a. Intel® MEBX password (both old and new) If Intel® PETS is used, the password which was entered in the SUT configuration for the Intel® ME password shall be used as the new password.</li> <li>b. FQDN "<a href="https://provisionServer.compliance.com">provisionServer.compliance.com</a>" (to update ConfigServerFQDN)</li> <li>c. Certificate Authority (CA) hash</li> </ol> </li> <li>9. The following step(s) are dependent on Intel® APS 3 usage: <ol style="list-style-type: none"> <li>a. If used, Intel® PETS will switch the USB Key from the management console to the SUT.</li> <li>b. If <b>not</b> used, Intel® PETS will prompt the test operator to switch the USB Key from the management console to the SUT manually.</li> </ol> </li> <li>10. Request the test operator to verify that there is <b>no</b> provisioning prompt displayed on the SUT during the next boot. The system should continue booting to Host OS.</li> <li>11. Restart the SUT to the base state of S0/MeOn.</li> <li>12. Verify the SUT has booted to Host OS.</li> <li>13. Request the test operator to confirm that <b>no</b> provisioning prompt appeared on the SUT during the boot.</li> <li>14. On the SUT, confirm the SUT <b>remains</b> in <i>Pre-provisioning</i> mode.</li> <li>15. The following step(s) are dependent on Intel® APS 3 usage: <ol style="list-style-type: none"> <li>a. If used, the Intel® PETS will switch the USB Key from the SUT to the management console.</li> <li>b. If <b>not</b> used, the Intel® PETS will prompt the test operator to switch the USB Key from the SUT to the management console manually.</li> </ol> </li> <li>16. Read the Setup.bin from USB Key and verify that the file records were <b>not changed</b>.</li> </ol>
Pass Criteria	The test passes, if the SUT is not configured and instead boots normally; the file records on the USB Key are not changed.
References	For details on the USB Key processing, refer to the <i>Intel® ME BIOS Specification</i> . Additional details about USB Key contents are available in the <i>Intel® Management Engine USB Key Local Provisioning Architecture Specification EDS</i> .



## 6.6 Remote and Host Based Configuration

The section serves as a checklist for the environment setup and testing of Intel® ME firmware Remote Configuration (RCFG) and Host Based Configuration feature support.

### 6.6.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Windows\* supported by Intel® PETS, and the SUT should have a version of Windows\* supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one HDD.

#### Tools for Testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- System Under Test (SUT): Should be connected to Intel® APS 3. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.

### 6.6.2 Remote Configuration Support

<b>ID</b>	<b>CS_040</b>				
<b>Title</b>	Remote Configuration Support				
<b>Requirement</b>	Mandatory - exempt for systems that do not support Remote Configuration (PKI-CH)				
<b>System</b>	<b>Form Factor</b>		<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
<b>Method</b>	Automated by Intel® PETS				
<b>Description</b>	Verify that the necessary settings to allow the Intel® ME system to be remotely configured are present on the SUT.				
<b>Objective</b>	Verify that the Intel® AMT platform can be provisioned using certificates under DHCP and automatic configuration mode. Remote Configuration (also called 'Zero Touch Configuration') is a feature that can help IT customers deploy and activate Intel® AMT.				
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.				
<b>Procedure</b>	1. On the SUT, extract the root certificate hashes. 2. Confirm that Remote Configuration (RCFG) is enabled.				
<b>Pass Criteria</b>	The test passes, if Remote Configuration (RCFG) is enabled.				
<b>References</b>	For details on the Remote Configuration control, refer to the <i>Intel® Management Engine Bring Up Guide</i> .				





### 6.6.3 Hosted Based Configuration Support

ID	CS_041				
Title	Host Based Configuration Support				
Requirement	Mandatory				
System	Form Factor		System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS				
Description	Verify an Intel® AMT compliant system can be provisioned using Host Based Configuration. <b>NOTE:</b> At the end of the test, Intel® PETS will fully unprovision the SUT. User will have to manually reprovision the SUT to run other tests that require a provisioned system.				
Objective	Verify that Intel® AMT can be provisioned using Host Based Configuration into Client Control Mode (CCM).				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be fully unprovisioned. Intel® Management Engine BIOS Extension (Intel® MEBX) full unprovision menu, the CMOS clear mechanism, or the BIOS unconfigure without password mechanisms may be used to fully unprovision the SUT. Refer the <i>Intel® Management Engine BIOS Extension User's Guide</i> or <i>Intel® ME BIOS Specification</i> documents for details.				
Procedure	<ol style="list-style-type: none"> <li>1. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li> <li>2. If the SUT is provisioned, fully unprovision it.</li> <li>3. Verify that the LMS service is running.</li> <li>4. Get the \$\$OSAdmin credentials on the SUT via Intel® AMT.</li> <li>5. Use the credentials to get the Intel® AMT general settings digest realm.</li> <li>6. Compute a network administrator password based on the MD5 hash of the digest realm.</li> <li>7. Use the network administrator password to provision the SUT via Intel® AMT Host Based Configuration to Client Control Mode.</li> <li>8. Verify that the provisioning state of the SUT is <i>Post-Provisioning</i>.</li> <li>9. Fully unprovision the SUT via Intel® AMT.</li> </ol>				
Pass Criteria	Test passes, if Intel® AMT system is provisioned by Host Based Configuration into Client Control Mode.				

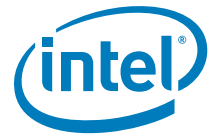
### 6.6.4 Embedded Host Based Configuration Support

ID	CS_042				
Title	Embedded Host Based Configuration Support				
Requirement	Optional - for use with embedded systems only				
System	Form Factor		System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS				
Description	<p>Verify an Intel® AMT compliant system can be provisioned using Embedded Host Based Configuration (EHBC), where supported, to enter Administrator Control Mode (ACM).</p> <p><b>Warning:</b> Platforms should not be configured to support EHBC, unless all security aspects has been understood and taken into account.</p> <p><b>NOTE:</b> At the end of the test, Intel® PETS will fully unprovision the SUT. User must manually reprovision the SUT to run other tests that require a provisioned system.</p>				



ID	CS_042
Objective	Verify that Intel® AMT can be provisioned using Embedded Host Based Configuration into Administrator Control Mode (ACM).
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be fully unprovisioned. Intel® Management Engine BIOS Extension (Intel® MEBX) full unprovision menu, the CMOS clear mechanism, or the BIOS unconfigure without password mechanisms may be used to fully unprovision the SUT. Refer the <i>Intel® Management Engine BIOS Extension User's Guide</i> or <i>Intel® ME BIOS Specification</i> documents for details.
Procedure	<ol style="list-style-type: none"><li>1. If the SUT is in an <i>In-Provisioning</i> state, return it to a <i>Pre-Provisioning</i> state.</li><li>2. If the SUT is provisioned, fully unprovision it.</li><li>3. Verify that the LMS service is running.</li><li>4. Get the \$\$OSAdmin credentials on the SUT via Intel® AMT.</li><li>5. Use the credentials to get the Intel® AMT general settings digest realm.</li><li>6. Compute a network administrator password based on the MD5 hash of the digest realm.</li><li>7. Use the network administrator password to provision the SUT via Intel® AMT Embedded Host Based Configuration to Administrator Control Mode.</li><li>8. Verify that the provisioning state of the SUT is <i>Post-Provisioning</i>.</li><li>9. Fully unprovision the SUT via Intel® AMT.</li></ol>
Pass Criteria	Test passes, if Intel® AMT system is provisioned by Embedded Host Based Configuration into Administrator Control Mode.

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## 7 SPI Flash Interface

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### Overview:

The test cases in this chapter are created to verify the correct configuration of the Intel® PCH SPI Host Controller. Test cases in this section verify implementation of SPI Dual and Quad I/O Fast Read, SPI Flash Descriptor mode, and ensure compliance with Intel® CSME and Intel® GbE requirements.

### Tools for Testing:

Intel® Platform Enablement Test Suite (PETS)—Use latest version of this kit. Refer to the Intel® PETS user guide available in the Intel® CSME Compliancy kit for details instructions on how to load and setup the Intel® PETS software.

Intel® Flash Image Tool (Fit.exe).

Intel® Flash Programming Tool—Available in DOS (Fpt.exe), EFI (Fpt.efi), Windows\* 32-bit (Ftpw.exe), and Windows\* 64-bit operating systems (Fptw-64).

### Test Environment:

The System Under Test (SUT) is to be configured in manual configuration mode with a wired LAN or wireless LAN dynamic IP address. The DHCP server connecting the SUT and Management Console (MC) must be configured to ensure that the wired LAN and wireless LAN addresses reside on separate subnets. The MC could be a laptop or desktop system running a version of Windows\* supported by PETS. The network configuration consists of a hub or switch, network cables, and a wireless Access Point (AP).



## 7.1 Test Coverage Summary

Test ID	Test Case Title	PETS/Manual	Form Factor	Network Factor
SPI_001	Descriptor Mode Test	PETS	DT/MB	LAN+WLAN; WLAN only
SPI_002	Serial Flash Discoverable Parameter Test	PETS	DT/MB	LAN+WLAN; WLAN only
SPI_003	4 Kbytes Erasable Blocks Test	PETS	DT/MB	LAN+WLAN; WLAN only
SPI_004	SPI Flash Size Test	PETS	DT/MB	LAN+WLAN; WLAN only
SPI_005	SPI Flash VSCC Test	PETS	DT/MB	LAN+WLAN; WLAN only
SPI_006	Flash Descriptor Security Override Test	PETS	DT/MB	LAN+WLAN; WLAN only
SPI_007	Single Input, Dual or Quad Output Fast Read Test	PETS	DT/MB	LAN+WLAN; WLAN only
SPI_008	Dual and Quad I/O Fast Read	PETS	DT/MB	LAN+WLAN; WLAN only



## 7.2 Descriptor Mode Test

Test ID	SPI_001
Test Case Title	Descriptor Mode Test
Mandatory/Optional	Mandatory
Description	Descriptor Mode is required for all SKUs of the PCH to ensure proper operation of features, such as the Intel® ME, Intel Integrated LAN driver, and PCH softstraps
Objective	Verify the SPI flash controller in the PCH is operating in Descriptor Mode
Procedure	<ol style="list-style-type: none"> <li>1. Boot to the target OS</li> <li>2. Verify the Flash Descriptor Valid Signature (FDBAR + 10h) is set to 0FF0A55Ah</li> </ol>
Test Pass/Fail Criteria	Test passes, if FDVS is 0FF0A55Ah

## 7.3 Serial Flash Discoverable Parameter Test

Test ID	SPI_002
Test Case Title	Serial Flash Discoverable Parameter (SFDP) Test
Mandatory/Optional	Mandatory
Description	Proper SFDP support in the SPI flash device may be used to enable advanced SPI features like the Quad I/O Fast Read.
Objective	Verify that the SPI flash controller in the PCH is able to detect a valid SFDP table in the SPI flash device.
Procedure	<ol style="list-style-type: none"> <li>1. Boot to target OS.</li> <li>2. Does flash device 0 in the SUT supports SFDP? <ul style="list-style-type: none"> <li>• If Yes, <ul style="list-style-type: none"> <li>— Verify that the Component Property Parameter Table Valid (CPPTV) bit 31 of the Vendor Specific Component Capabilities 0 register (VSCC0<sup>4</sup>) is set to 1b.</li> </ul> </li> <li>• If No, <ul style="list-style-type: none"> <li>— Inform the test operator that SFDP support in the SPI flash device may be used to enable advanced SPI features like the Quad I/O Fast Read<sup>3</sup>.</li> </ul> </li> </ul> </li> <li>3. Read the number of SPI parts by means of the Number of Components (NC) bits [9:8] in the Flash Map 0 (FLMAP0) register at (FDBAR + 14h). <ul style="list-style-type: none"> <li>• If the number of components is 01b (2 Components) continue to next step else end test.</li> </ul> </li> <li>4. Does flash device 1 in the SUT supports SFDP? <ul style="list-style-type: none"> <li>• If Yes, <ul style="list-style-type: none"> <li>— Verify that the Component Property Parameter Table Valid (CPPTV) bit 31 of the Vendor Specific Component Capabilities 1 register (VSCC1<sup>4</sup>) is set to 1b.</li> </ul> </li> <li>• If No, <ul style="list-style-type: none"> <li>— Inform the test operator that SFDP support in the SPI flash device may be used to enable advanced SPI features like that Quad I/O Fast Read<sup>3</sup>.</li> </ul> </li> </ul> </li> </ol> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. VSCC0 register is located at (VTBA<sup>4</sup> + C4h).</li> <li>2. VSCC1 register is located at (VTBA<sup>4</sup> + C4h + (n*8)h), where n=1.</li> <li>3. Test considered pass, this is just additional information to user.</li> <li>4. Refer to SPI Programming Guide for details of these registers.</li> </ol>
Test Pass/Fail Criteria	Test passes, if all steps return expected values.



## 7.4 4 Kbytes Erasable Blocks Test

Test ID	SPI_003
Test Case Title	4 Kbytes Erasable blocks Test
Mandatory/Optional	Mandatory
Description	The SPI Flash device must provide uniform 4 Kbytes erasable blocks/sectors throughout the entire part. This is required by Intel® CSME firmware.
Objective	Verify the SPI flash device supports uniform 4 Kbytes erasable blocks.
Procedure	<p>Part 1: Verify registers.</p> <ol style="list-style-type: none"><li>1. Boot to the target OS.</li><li>2. Verify the SUT is operating in Descriptor Mode by confirming that the Flash Descriptor Valid (FDV) bit 14 in the Hardware Sequencing Flash Status (HSFS) register (SPIBAR + 04h) has been set to '1'.</li><li>3. Verify all flash components support 4 Kbytes erasable blocks by confirming that the Block/Sector Erase Size (BERASE) bits [4:3] in the Hardware Sequencing Flash Status (HSFS) register (SPIBAR + 04) are set to 01b.</li></ol> <p>Part 2: Check against SPI flash device datasheet.</p> <ol style="list-style-type: none"><li>1. Using the "MEInfo"<sup>1</sup> tool, read the SPI flash device ID from the SUT.</li><li>2. Verify the SPI flash device ID(s) read from the SUT are found in the vsccommn.bin<sup>2</sup> SPI part registry cached in Intel® PETS.</li></ol> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The "MEInfo" tool is part of the Intel® Management Engine Firmware release package, under System Tools folder.</li><li>2. The vsccommn.bin file will be updated relative to the latest official version for each Intel® PETS release.</li></ol>
Test Pass/Fail Criteria	Test passes, if all steps return expected values.



## 7.5 SPI Flash Size Test

<b>Test ID</b>	<b>SPI_004</b>
<b>Test Case Title</b>	SPI Flash Size Test
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Intel® PCH SKUs each have different requirements for SPI flash sizes. This test verifies that the SPI flash device has enough space to store the whole SPI image created by Intel® FIT tool.
<b>Objective</b>	Verify the correct SPI flash size is used for a given PCH SKU contained in the SUT.
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Boot to target OS.</li> <li>2. Read following information from SPI Flash Descriptor in the SUT: <ul style="list-style-type: none"> <li>• The number of SPI parts by means of the Number of Components (NC) bits [9:8] in the Flash Map 0 (FLMAP0) register at (FDBAR + 14h).</li> <li>• The size of the first flash component by means of the Component 0 Density (C0DEN) bits [3:0] in the Flash Components Record (FLCOMP) register at (FCBA + 0h).</li> <li>• If the number of components is 01b (2 Components), read the size of the second flash component by means of the Component 1 Density (C1DEN) bits [7:4] in the Flash Components Record (FLCOMP) register at (FCBA + 0h).</li> </ul> </li> <li>3. Compare the SUT flash size against the: <ul style="list-style-type: none"> <li>• SPI flash device manufacturer datasheet<sup>1</sup>.</li> </ul> </li> </ol> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. Intel® PETS will maintain a list of SPI flash device sizes.</li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>The test passes, if the following conditions is true:</p> <ol style="list-style-type: none"> <li>1. The flash components sizes in the SUT are less than or equal to the size stated in the SPI device manufacturer datasheet.</li> </ol>

## 7.6 SPI Flash Vendor Specific Capabilities (VSCC) Test

Test ID	SPI_005
Test Case Title	SPI Flash Vendor Specific Component Capabilities (VSCC) Test.
Mandatory/Optional	Mandatory
Description	The VSCC registers are defined in two places. Host-based VSCCn registers (for example, VSCC0 and VSCC1) in memory mapped space and the Intel® CSME VSCC Table in the SPI Flash Descriptor. Intel® CSME only uses the VSCC table in the SPI Flash Descriptor, while the memory map VSCCn registers are used by BIOS and GbE software. The Intel® CSME VSCC table is created using the FIT tool by ODM/OEM, while the memory mapped VSCCn registers are programmed by BIOS. Incorrect VSCCn registers configuration may affect SPI flash functionality and also may lead to premature flash device wear out.
Objective	To verify VSCCn registers in memory mapped space and VSCC table in SPI Flash Descriptor is configured correctly.
Procedure	<ol style="list-style-type: none"> <li>1. Boot to the target OS.</li> <li>2. Read the Vendor Specific Component Capabilities Registers (VSCCn), in the memory mapped space, where these register are located at (SPIBAR + C4h) and (SPIDBAR + C4h + (1 * 8)h) respectively.</li> <li>3. Verify the VSCCn values with the SPI Flash device manufacturer datasheet.</li> <li>4. Read the VSCC table from the SPI flash device on the target system. The base address of the table is located at offset (FDBAR<sup>1</sup> + EFCh). The Intel® CSME VSCC Table Base Address (VTBA) and the Intel® CSME VSCC Table Length (VTL) are located at (FDBAR + EFCh).</li> <li>5. Every record in the table is 2 DWORDs long, the first 32 bits contain the SPI flash device's JEDEC ID, and the following 32 bits represent its VSCC value.</li> <li>6. Iterate through the VSCC table searching for the matching JEDEC ID of the SPI devices in use on the SUT and verify the associated VSCC values matches both the SPI flash device manufacturer datasheet and the Intel® CSME VSCC value.</li> </ol> <p><b>Note:</b> FDBAR is located at address 0 of the SPI flash device chip select 0.</p>
Test Pass/Fail Criteria	Test results pass, if VSCC0 or VSCC0 and VSCC1, and the VCSS table in SPI Flash Descriptor align with the Intel® CSME VSCC and SPI flash device manufacturer datasheet settings.

## 7.7 Flash Descriptor Security Override Test

Test ID	SPI_006
Test Case Title	Flash Descriptor Security Override Test
Mandatory/Optional	Mandatory
Description	This boots the platform in Intel® CSME Test Mode. This gives the ability to override Flash descriptor permissions debug/repair depot environments. This must NOT be default behavior.





Test ID	SPI_006
Objective	This test is to verify the platform has the ability to enable and disable Intel® CSME manufacturing mode, and to be able to reprogram the entire SPI flash.
Procedure	<ol style="list-style-type: none"> <li>1. Boot platform without having HDA_SDO asserted high on the rising edge of PWROK. Verify that FDOPSS is set to '1'. FDOPSS is in MMIO space (SPIBAR + 0x4) bit 13.</li> <li>2. Boot platform with having HDA_SDO asserted high on the rising edge of PWROK. Verify that FDOPSS is set to '0'. FDOPSS is in MMIO space (SPIBAR + 0x4) bit 13. This assertion of HDA_SDO can be with a jumper or through another external mechanism. Care should be taken to ensure that assertion of this mechanism to assert HDA_SDO <b>cannot</b> be done remotely.</li> </ol> <p>PETS will help automate testing of this capability. Perform the test by enabling "State after G3 to S5" at BIOS setting.</p> <p><b>Alternate Procedure:</b></p> <ol style="list-style-type: none"> <li>1. Configure the platform with Intel® CSME Firmware.</li> <li>2. Use FPT /d to dump the image.</li> <li>3. Use Flash Programming Tool (FPT) to lock the image down using the -closemfnf. Boot system from a G3 state.</li> <li>4. Use FPT /d to dump the image. This test should fail.</li> <li>5. Use the physical jumper to override the protection (asserts HDA_SDO high during rising edge of PWROK).</li> <li>6. Use FPT /d to dump the image. This test should now pass.</li> </ol>
Test Pass/Fail Criteria	Test passes, if FDOPSS bit is set to '1' by default and set to '0' when intending to enter Intel® CSME Test Mode.

## 7.8 Serial Flash Single Input, Dual, or Quad Output Fast Read Test

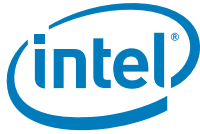
Test ID	SPI_007
Test Case Title	Single Input, Dual or Quad Output Fast Read Test
Mandatory/Optional	Mandatory
Description	This test is to verify that the flash parts will support Single Input, Dual, or Quad Output fast read if selected. This is a new mode of operation for serial flash that increases the read speed of SPI flash. If incorrectly configured there could be undesired operation.
Objective	This test is to verify that the flash parts will support Single Input, Dual, or Quad Output fast read if selected.
Procedure	<p>PETS will ask the user whether 'Single Input Dual or Quad Output Fast Read' is supported.</p> <p><b>If Yes,</b></p> <ol style="list-style-type: none"> <li>1. PETS will verify that FLCOMP bit 20 is set to 1b.</li> <li>2. PETS will then use Serial Flash Discovery Parameters to verify that all flash parts in the system support 'Single Input, Dual or Quad Output Fast Read'.</li> <li>3. PETS will check whether softstraps are enabled to support Dual or Quad Output Fast Read Function. <ol style="list-style-type: none"> <li>a. For Dual Output Read, PETS will check if FLCOMP bit 12 is set to 1.</li> <li>b. For Quad Output Read, PETS will check if FLCOMP bit 14 is set to 1.</li> </ol> </li> </ol> <p><b>Note:</b> Quad Output Fast Read is not supported if the Flash device does not have SFDP.</p> <p><b>If No,</b></p> <ol style="list-style-type: none"> <li>1. PETS will verify that FLCOMP bit 20 is set to 0b.</li> </ol>
Test Pass/Fail Criteria	<p>Test fails, if there is an invalid configuration with single input, dual, or quad output fast read.</p> <p>Test results passes, if settings are not invalid, and if single input, dual output fast read is verified by SFDP.</p>

Test ID	SPI_008
Test Case Title	Dual and Quad I/O Fast Read
Mandatory/Optional	Mandatory
Description	This test is to verify that the flash parts will support Dual or Quad I/O Fast Read. This is a new mode of operation for serial flash that increases the read speed of SPI flash. If incorrectly configured there could be undesired operation.



<b>Test ID</b>	<b>SPI_008</b>
<b>Objective</b>	This test is to verify that the flash parts will support Dual or Quad I/O Fast Read
<b>Procedure</b>	<p>PETS will ask the user whether "Dual or Quad I/O Fast Read" is supported.</p> <p><b>If Yes,</b></p> <ol style="list-style-type: none"> <li>1. PETS will use Serial Flash Discovery Parameters (SFDP) to verify that all flash parts in the system support 'Dual or Quad I/O Fast Read.</li> <li>2. PETS will then check, if             <ol style="list-style-type: none"> <li>a. If FLCOMP bit 13 is set to 1 if Dual I/O fast read is supported; or</li> <li>b. FLCOMP bit 15 is set to 1 if Quad I/O fast read is supported.</li> </ol> </li> <li>3. PETS will verify that FLCOMP bit 20 set to 1.</li> </ol> <p><b>If No,</b></p> <ol style="list-style-type: none"> <li>4. PETS will then check, if             <ol style="list-style-type: none"> <li>a. offset FLCOMP bit 13 is set to 0 if Dual I/O Fast Read is not supported; or</li> </ol> </li> <li>5. FLCOMP bit 15 is set to 0 if Quad I/O Fast Read is not supported.</li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>Test fails, if there is an invalid configuration with single input, Dual or Quad I/O Fast Read and if serial flash part does not support Serial Flash Discovery Parameters, Dual and Quad I/O Fast Read will not be supported.</p> <p>Test results passes, if settings are not invalid, and if single input, Dual or Quad I/O Fast Read is verified by SFDP.</p>

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## 8 Enhanced Serial Peripheral Interface (eSPI)

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The purpose of this chapter is to describe the test required in order to verify the eSPI configurations and functionality are according to Intel® compliancy. eSPI is a bus interface between the SoC/PCH and EC on Intel® IA platforms. It introduces Real-Time Flash Sharing through its MAF and SAF configurations, allocate low voltage of 1.8 V to I/O buffers, reduces pin count, and allows for higher bandwidth.

### 8.1 Test Environment Setup

Tests in this chapter differ in implementation according to the System Under Test (SUT's) configuration; where SUTs can be configured to run with MAF or SAF enabled.

### 8.2 Tools for Testing

- Intel® Flash Image Tool (Intel® FIT)
- Intel® Flash Programming Tool (Intel® FPT)
- Intel® MEManuf
- Intel® FWupdate Tool
- Intel® Platform Flash Tool (Intel® PFT)



## 8.3 Test Coverage Summary

Platform, Operating System Support, How? Column describes the test methodology.

OS Support: W = Microsoft\* Windows\*, AOS = Android\* OS

How?: A = Fully Automated using Intel® PETS, I = Interactive using Intel® PETS and M = Manual.

Test ID	Test Case Title	PETS Package Name	OS Supported	How?
eSPI_001	Bootting with MAF configurations (straps set to MAF defaults)	N/A	W	M
eSPI_003	Platform boots with EC region	N/A	W	M
eSPI_004	Platform boots with EC region in different location	N/A	W	M
eSPI_005	Platform boots without EC region	N/A	W	M
eSPI_006	IFWI with empty EC region	N/A	W	M
eSPI_007	IFWI with empty EC binary	N/A	W	M
eSPI_008	Platform boots with default EC region permissions	N/A	W	M
eSPI_009	Platform boots with EC Read-Only permission to BIOS region	N/A	W	M
eSPI_010	Platform boots with EC Read-Only permission to BIOS region and BIOS with RW permissions to EC	N/A	W	M
eSPI_011	Perform FWUpdate with MAF configurations	N/A	W	M



## 8.4 Booting with MAF Configurations (Straps Set to MAF Defaults)

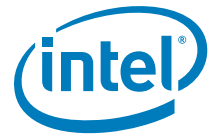
Test ID	eSPI_001
Test Case Title	Booting with MAF configurations (straps set to MAF defaults)
Platform	Platforms with MAF configuration
Mandatory/Optional	Mandatory
Objective	Verify that the platform boots with default MAF configuration
Test Pass Criteria	Test passes if platform boots to OS
Description	Platform should boot to OS with all MAF straps set to default
Procedure	<ol style="list-style-type: none"><li>1. Follow Intel® SPI Programming Guide and review all soft straps applicable to MAF.</li><li>2. Build IFWI with default straps for MAF using Intel® FIT.</li><li>3. Flash IFWI onto the platform.</li><li>4. Check that platform boots to OS.</li></ol>

## 8.5 Platform Boots with EC Region

Test ID	eSPI_003
Test Case Title	Platform boots with EC region
Platform	Platforms with SAF/MAF configuration
Mandatory/Optional	Mandatory
Objective	Verify that the platform boots with EC region
Test Pass Criteria	Test passes if platform boots to OS
Description	Setting the EC region in Intel® FIT and flashing the platform with IFWI that would successfully boot the platform to OS
Procedure	<ol style="list-style-type: none"><li>1. Create and IFWI in Intel® FIT with EC region.</li><li>2. Flash IFWI onto the platform.</li><li>3. Check that platform boots to OS.</li></ol>

## 8.6 Platform Boots with EC Region in Different Place

Test ID	eSPI_004
Test Case Title	Platform boots with EC region in different location
Platform	Platforms with SAF/MAF configuration
Mandatory/Optional	Mandatory
Objective	Verify that the platform boots with EC region set in a different place



Test ID	eSPI_004
Test Pass Criteria	Test passes if platform boots to OS
Description	Stitching an EC region from a different place and flashing the IFWI that would successfully boot the platform to OS
Procedure	<ol style="list-style-type: none"> <li>1. Create IFWI in Intel® FIT with EC region at a different location</li> <li>2. Flash IFWI onto the platform</li> <li>3. Check that the platform is booting to OS</li> </ol>

## 8.7 Platform Boots without EC Region

Test ID:	eSPI_005
Test Case Title	Platform boots without EC region
Platform	Platform configured with No Flash Sharing
Mandatory/Optional	Mandatory
Objective	Verify that the platform boots successfully to OS without EC region
Test Pass Criteria	Test passes if platform boots to OS
Description	No Flash Sharing is a configuration in which EC resides on its own separate flash device.
Procedure	<ol style="list-style-type: none"> <li>1. Create IFWI in Intel® FIT with EC region disabled</li> <li>2. Make sure Intel® FIT tool does not return any errors</li> <li>3. Flash IFWI onto the platform</li> <li>4. Check that the platform is booting to OS</li> </ol>

## 8.8 IFWI with Empty EC Region

Test ID	eSPI_006
Test Case Title	IFWI with empty EC region
Platform	Platforms with SAF/MAF configuration
Mandatory/Optional	Mandatory
Objective	Ensure that Intel® FIT tool prevents building an image with empty EC region
Test Pass Criteria	Intel® FIT does not build IFWI with empty EC region
Description	EC region is mandatory when EC region is enabled in Intel® FIT. Intel® FIT should return error in building, when EC region is enabled but no EC binary is provided
Procedure	<ol style="list-style-type: none"> <li>1. Enable EC region in Intel® FIT</li> <li>2. Create IFWI without providing EC region</li> <li>3. Check that Intel® FIT does not build IFWI successfully</li> </ol>



## 8.9 IFWI with Empty EC Binary

Test ID	eSPI_007
Test Case Title	IFWI with empty EC binary
Platform	Platforms with SAF/MAF configuration
Mandatory/Optional	Mandatory
Objective	Verify that Intel® FIT does not create an IFWI if provided with an empty EC binary
Test Pass Criteria	Intel® FIT returns appropriate error and does not build IFWI
Description	Providing EC binary is mandatory in SAF and MAF configurations, Intel® FIT should prevent building an image with an empty EC binary
Procedure	<ol style="list-style-type: none"><li>1. Enable EC region in Intel® FIT</li><li>2. Do not provide 16byte EC binary as input</li><li>3. Provide EC FW binary as input only</li><li>4. Check that Intel® FIT does not complete IFWI building and return appropriate error</li></ol>

## 8.10 Platform Boots with Default EC Region Permissions

Test ID	eSPI_008
Test Case Title	Platform boots with default EC region permissions
Platform	Platforms with MAF configuration <b>(Requires EOM for EC region)</b>
Mandatory/Optional	Mandatory
Objective	Verify that EC region default permissions are loaded successfully and platform boots to OS
Test Pass Criteria	Test passes, if platform boots to OS, EOM is set, and Intel® MEManuf-EOL check passes
Description	EC region is set with default Read/Write permissions to its own region.
Procedure	<ol style="list-style-type: none"><li>1. Create IFWI with default descriptor permissions in Intel® FIT</li><li>2. Flash IFWI onto the platform</li><li>3. Boot platform to OS</li><li>4. Run Intel® FPT -closemef EC</li><li>5. Run Intel® MEManuf -EOL</li><li>6. Make sure that Intel® MEManuf -EOL check passes</li></ol>

## 8.11 Platform Boots with EC Read-Only Permission to BIOS Region

Test ID	eSPI_009
Test Case Title	Platform boots with EC Read-Only permission to BIOS region
Platform	Platforms with MAF configuration <b>(Requires EOM for EC region)</b>
Mandatory/Optional	Mandatory
Objective	This test is to verify that the platform will be boot successfully to OS with EC having only read permission to BIOS region and with default permission for the other regions





<b>Test ID</b>	<b>eSPI_009</b>
<b>Test Pass Criteria</b>	Test passes if platform boots to OS, EOM is set, and Intel® MEManuf -EOL check passes
<b>Description</b>	EC region can be configured to Read-Only from BIOS region
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Create IFWI with EC Read-Only access to BIOS region in descriptor permissions in Intel® FIT. They should be as follows: <ol style="list-style-type: none"> <li>a. EC read access should have a value of 0x103 in Intel® FIT.</li> </ol> </li> <li>2. Flash IFWI onto the platform.</li> <li>3. Boot platform to OS.</li> <li>4. Run Intel® FPT -closemfn EC.</li> <li>5. Run Intel® MEManuf -EOL.</li> <li>6. Make sure that Intel® MEManuf -EOL check passes.</li> </ol>

## 8.12 Platform Boots with EC Read-Only Permission to BIOS Region and BIOS with RW Permissions to EC

<b>Test ID</b>	<b>eSPI_010</b>
<b>Test Case Title</b>	Platform boots with EC Read-Only permission to BIOS region and BIOS with RW permissions to EC
<b>Platform</b>	Platforms with MAF configuration <b>(Requires EOM for EC region)</b>
<b>Mandatory/Optional</b>	Mandatory
<b>Objective</b>	This test is to verify that the platform will be boot successfully to OS with EC having only read permission to BIOS region and with BIOS have RW permissions to EC region
<b>Test Pass Criteria</b>	Test passes, if platform boots to OS, EOM is set, and Intel® MEManuf -EOL check passes
<b>Description</b>	EC region can be configured to Read-Only from BIOS region as well as having BIOS with RW permissions to EC region
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Create IFWI with EC Read-Only access to BIOS region and BIOS with RW permissions to EC region in descriptor permissions in Intel® FIT. They should be as follows: <ul style="list-style-type: none"> <li>— EC read access should have a value of 0x103 in Intel® FIT.</li> <li>— Host CPU/BIOS read access should have a value of either 0x10F or 0x11F.</li> <li>— Host CPU/BIOS write access should have a value of either 0x10A or 0x11A.</li> </ul> </li> <li>2. Flash IFWI onto the platform.</li> <li>3. Boot platform to OS.</li> <li>4. Run Intel® FPT -closemfn EC.</li> <li>5. Run Intel® MEManuf -EOL.</li> <li>6. Make sure that Intel® MEManuf -EOL check passes.</li> </ol>



## 8.13 Perform FWUpdate with MAF Configurations

Test ID	eSPI_011
Test Case Title	Perform FWUpdate with MAF configurations
Platform	Platforms with MAF configurations
Mandatory/Optional	Mandatory
Objective	This test is to verify that the FWupdate flow will work properly with MAF configurations and platform boots to OS
Test Pass Criteria	Test passes, if FWupdate flow is successfully completed with MAF configurations in place.
Description	Ensuring that the platform would successfully boot with MAF configurations after performing a FWUpdate flow
Procedure	<ol style="list-style-type: none"><li>1. Follow steps 1 and 2 of test eSPI_001.</li><li>2. Perform FWUpdate process on the platform - Refer to the System Tools User Guide for more information on the FWUpdate flow.</li><li>3. Verify that platform can boot to OS after FWUpdate is completed.</li></ol>

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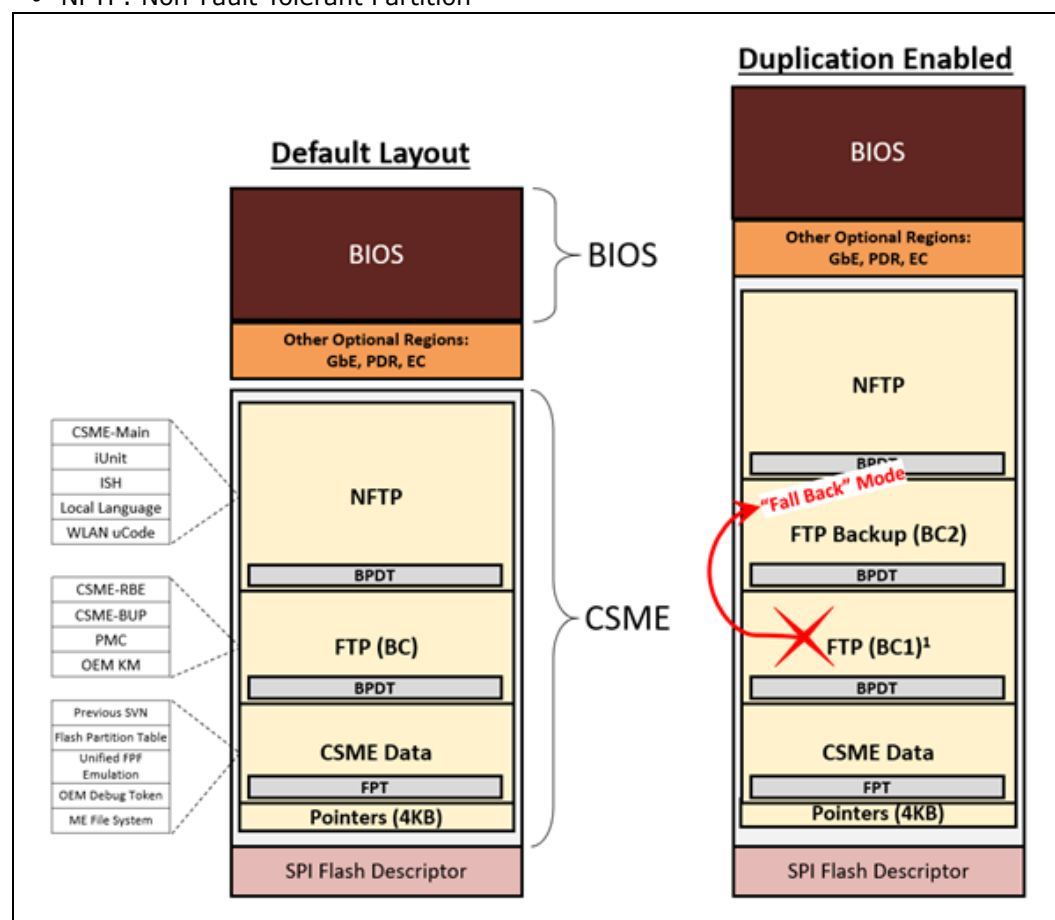
## 9 Intel® CSME Resiliency Compliance

The Intel® Converged Security and Management Engine Resiliency Compliance section serves test list for confirming CSME resiliency feature is enabled properly on OEM platform

### 9.1 Intel® CSME Layout Overview with Boot Critical Redundancy

Below is a high-level diagram depicting Intel® CSME layout relative to other SPI regions, where:

- FTP: Fault Tolerant Partition
- BC: Boot Critical
- NFTP: Non-Fault Tolerant Partition





**Note:** TGL/RKL supports TCSS components included in BC1/2. Duplication of “Pointers” region also optionally available through an Intel® FIT configuration.

### 9.1.1 Intel® CSME Layout Pointers

Intel® CSME ROM will look for layout configuration at the beginning of CSME region starting with the Pointers region. Intel® FIT tool will generate the locations and the pointers where ROM will use to find each of the main partitions from above diagram (FTP, NFTP, Data).

Offset (bytes) Layout 1.6 (CSME 12, 14)	Offset (bytes) Layout 1.7 (CSME 13, 15)	Description (Boot Critical Redundancy Disabled)
19 to 16	27:24	Data partition base offset (pointer to Flash partition Table)
23 to 20	31:28	Data partition size
27 to 24	35:32	FTP (boot critical) partition base offset (Pointer to logical boot partition 1 - BPDT 1)
31 to 28	39:36	FTP (boot critical) partition size
35 to 32	43:40	NFTP partition base offset (Pointer to logical boot partition 2 - BPDT 2)
39 to 36	47:44	NFTP partition size

Offset (bytes) Layout 1.6 (CSME 12, 14)	Offset (bytes) Layout 1.7 (CSME 13, 15)	Description (Boot Critical Redundancy Enabled)
19 to 16	27:24	Data partition base offset (pointer to Flash partition Table)
23 to 20	31:28	Data partition size
27 to 24	35:32	Primary FTP (BC1) partition base offset (Pointer to logical Boot Partition 1 - BPDT 1)
31 to 28	39:36	Primary FTP (BC1) partition size (Boot Partition 1)
35 to 32	43:40	Backup FTP (BC2) partition base offset (Pointer to logical boot partition 2 - BPDT 2)
39 to 36	47:44	Backup FTP (BC2) partition size (Boot Partition 2)
43 to 40	51:48	NFTP partition base offset (Pointer to logical boot partition 3 - BPDT 3)
47 to 44	55:52	NFTP partition size (Boot Partition 3)

### 9.1.2 Boot Partition Descriptor Table (BPDT)

The Boot Partition Descriptor Table (BPDT) is a table of offsets to all individual sub-partitions contained within each of the LBPs (Logical Boot Partition). A sub-partition is as a sub-division of the logical boot partition.

The BPDT contains a header, immediately followed by 0 or more entries (number of following entries is indicated in the header).

Note that the BPDT is not signed and therefore its consumers must treat its contents with care.

**Table 9-1. BPDT Layout in Intel® CSME Region**

BPDT Header			
Field Name	Offset	Size (bytes)	Description
Signature	0	4	Validity signature. For a valid BPDT (aka "green"), this value must be 0x000055AA. During IFWI update, this value is modified. The value of 0x00AA55AA indicates the BPDT is valid and can be booted from, however the firmware update is still in progress (aka "yellow" - recovery mode). Any other value indicates an invalid BPDT structure (aka "red").
Descriptor Count	4	2	Number of BPDT entries following this header
Version	6	1	Version of this BPDT structure. '1' - Layout 1.6 (CSME 12 & 14) '2' - Layout 1.7 (CSME 13 & 15)
Reserved	7	1	Reserved
CRC32 checksum	8	4	CRC32 checksum of entire BPDT structure (Header and Entries) –The signature bytes [3:0] will not be checked
IFWI Version	12	4	Version of the particular IFWI build as marked by the build server
FIT Tool Version	16	8	Major/Minor/Build/Hotfix version of the FIT tool that was used to stitch the image. Not used by firmware
BPDT Entry			
Type	0	4	Bits 0:15 - type of the logical sub-partition indicated by this entry. Should be one of the following: 1 = CSME RBE 2 = CSME BUP 7 = CSME Main 8 = ISH 14 = PMC 15 = iUnit 18 = WLAN uCode 19 = Local Language 20 = OEM Key Manifest 21 = CSME Defaults 23 = IOM FW (TypeC)
Sub-partition offset	4	4	Offset of the logical sub-partition indicated by this entry. The offset is indicated in bytes from the beginning of the Boot Partition.
Sub-partition size	8	4	Size of the logical sub-partition indicated by this entry. The size is indicated in bytes.



### 9.1.3 Intel® CSME High-Level Flow

1. CSME ROM finds BC1 offset from "Pointers" section attempts boot from BC1, if failure during boot (signature/integrity check fails), Reset and switch to BC2 and boot
2. When booting from BC2, continue boot to fully Normal CSME functionality with NFTP as well
3. Indicate in FWSTS that CSME booting from BC2 ("Fallback") while CSME remains in full functional working state as "Normal Mode"
4. To recover corrupted BC1, OEM may do normal CSME FW Update operation.

### 9.1.4 Intel® CSME Firmware Status (FWSTS1) Register Indication Scenarios

Primary FTP Failure (BC1) Status	NFTP Failure Status	FWSTS Indication	OEM Action Required	Expected Outcome
Yes	Yes	FWSTS1.bit0-3 (Current State): Recovery [2] FWSTS1.bit10 (BC1 Boot Failed): Yes [1]	CSME FW update	Recovered Primary FTP (BC1) Recovered NFTP
Yes	No	FWSTS1.bit0-3 (Current State): Normal [2] FWSTS1.bit10 (BC1 Boot Failed): Yes [1]	CSME FW update	Recovered Primary FTP (BC1)
No	Yes	FWSTS1.bit0-3 (Current State): Recovery [2] FWSTS1.bit10 (BC1 Boot Failed): No [0]	CSME FW update	Recovered NFTP
No	No	FWSTS1.bit0-3 (Current State): Normal [2] FWSTS1.bit10 (BC1 Boot Failed): No [0]	No action required	N/A



## 9.2 Test Environment

The system under test is to be configured with the Intel® CSME **not** in manufacturing mode (fpt -closemnf completed).

## 9.3 Test Coverage Summary

### Form Factor:

D = Desktop, M = Mobile, A = All in one

### Network:

LAN = systems with LAN interface and test is performed using LAN interface

WLAN = systems with WLAN interface and test is performed using the WLAN interface

Test ID	Test Case Title	PETS/Manual	Form Factor	Network
Resilience_01	Boot Critical Redundancy Enabled	Manual	D M A	LAN or WLAN
Resilience_02	Critical Code Corruption - BPDT	Manual	D M A	LAN or WLAN
Resilience_03	Critical Code Corruption - BUP	Manual	D M A	LAN or WLAN
Resilience_04	Critical Code Corruption - PMC	Manual	D M A	LAN or WLAN
Resilience_05	Critical Code Corruption - TCSS	Manual	D M A	LAN or WLAN
Resilience_06	Recovery of Corrupted Primary Boot Critical (BC1) Partition	Manual	D M A	LAN or WLAN

## 9.4 Boot Critical Redundancy Enabled

Test ID	Resilience_01
Test Case Title	Boot Critical Redundancy Enabled
Mandatory/Optional	Optional
Description	The system is not in the Intel® ME Manufacturing Mode—when the system completes this test. This test is to confirm Boot Critical Redundancy Resiliency Feature is properly enabled and recognized by CSME. Do not perform any image corruption in this test.
Objective	Verify "Boot Critical Code Redundancy" is properly enabled and system normally booting to primary partition
Procedure	<ol style="list-style-type: none"> <li>1. Build image using FIT with redundancy enabled: Build -&gt; Build Settings -&gt; under "Image Build Settings", set "Redundancy Enabled" to "True".</li> <li>2. Boot system at least once to OS.</li> <li>3. Confirm MEInfo output shows "Boot critical code redundancy" as "Enabled"</li> <li>4. Confirm "Current Boot Partition" is "1"</li> <li>5. Confirm FWSTS1.bit10 = "0" also indicating "Current Boot Partition" is Primary FTP/BC1 where "0" means no failure in booting BC1.</li> </ol>
Test Pass/Fail Criteria	Pass: "Boot critical code redundancy" = "Enabled" AND "Current Boot Partition" = "1" Fail: "Boot critical code redundancy" = "Disabled"



## 9.5 Critical Code Corruption - BPDT1

<b>Test ID</b>	<b>Resilience_02</b>
<b>Test Case Title</b>	Critical Code Corruption – BPDT
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	The system is not in the Intel® ME Manufacturing Mode—when the system completes this test. This test is to confirm CSME can fallback to Backup copy of FTP (BC2) when BC1 is corrupted.
<b>Objective</b>	Verify Intel® CSME automatically falls back to BC2 when BC1 is corrupted.
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Build image using FIT with redundancy enabled: Build -&gt; Build Settings -&gt; under "Image Build Settings", set "Redundancy Enabled" to "True".</li><li>2. Boot system at least once to OS.</li><li>3. Place system in G3 and dump full SPI image.</li><li>4. From Layout Pointers, retrieve offset of "Boot Partition 1 (BP1)" (offset value located @ 35:32 within layout pointers).</li><li>5. "Boot Partition 1" starts with BPD structure, manually corrupt structure writing "0xffffffff" at its offset 0 and save as "Corrupted_BPDT1.bin"</li><li>6. While system is in G3, flash Corrupted_BPDT1.bin image to SPI</li><li>7. Power up SUT and boot to OS</li><li>8. Confirm the following:<ol style="list-style-type: none"><li>a. MEInfo shows: "Current Boot Partition" = "2".</li><li>b. FWSTS1.bit0-3 (Current State): Normal [5].</li><li>c. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li></ol></li></ol>
<b>Test Pass/Fail Criteria</b>	<p>Pass: All below conditions must be met to pass the test:</p> <ol style="list-style-type: none"><li>1. MEInfo shows: "Current Boot Partition" = "2".</li><li>2. FWSTS1.bit0-3 (Current State): Normal [5].</li><li>3. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li></ol> <p>Fail: No Boot</p>





## 9.6 Critical Code Corruption - BUP

<b>Test ID</b>	<b>Resilience_03</b>
<b>Test Case Title</b>	Critical Code Corruption – BUP
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	The system is not in the Intel® ME Manufacturing Mode—when the system completes this test. This test is to confirm CSME can fallback to Backup copy of FTP (BC2) when BC1 is corrupted.
<b>Objective</b>	Verify Intel® CSME automatically falls back to BC2 when BC1 is corrupted.
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Build image using FIT with redundancy enabled: Build -&gt; Build Settings -&gt; under "Image Build Settings", set "Redundancy Enabled" to "True".</li> <li>2. Boot system at least once to OS.</li> <li>3. Place system in G3 and dump full SPI image.</li> <li>4. From Layout Pointers, retrieve offset of "Boot Partition 1 (BP1)" (offset value located @ 35:32 within layout pointers).</li> <li>5. "Boot Partition 1" starts with BPD1 structure. Within BPD1 find the BPD1 Entry for "CSME BUP" (type 2) and manually Corrupt partition content at offset 700KB [do 4 KB erase] and save as "Corrupted_BUP.bin" (See BPD1 details above).</li> <li>6. While system is in G3, flash Corrupted_BUP.bin image to SPI</li> <li>7. Power up SUT and boot to OS (expect to see global reset)</li> <li>8. Confirm the following: <ol style="list-style-type: none"> <li>a. MEInfo shows: "Current Boot Partition" = "2".</li> <li>b. FWSTS1.bit0-3 (Current State): Normal [5]</li> <li>c. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li> </ol> </li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>Pass: All below conditions must be met to pass the test:</p> <ol style="list-style-type: none"> <li>1. MEInfo shows: "Current Boot Partition" = "2".</li> <li>2. FWSTS1.bit0-3 (Current State): Normal [5].</li> <li>3. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li> </ol> <p>Fail: No Boot</p>



## 9.7 Critical Code Corruption - PMC

<b>Test ID</b>	<b>Resilience_04</b>
<b>Test Case Title</b>	Critical Code Corruption – PMC
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	The system is not in the Intel® ME Manufacturing Mode—when the system completes this test. This test is to confirm CSME can fallback to Backup copy of FTP (BC2) when BC1 is corrupted.
<b>Objective</b>	Verify Intel® CSME automatically falls back to BC2 when BC1 is corrupted.
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Build image using FIT with redundancy enabled: Build &gt; Build Settings &gt; under "Image Build Settings", set "Redundancy Enabled" to "True".</li><li>2. Boot system at least once to OS.</li><li>3. Place system in G3 and dump full SPI image.</li><li>4. From Layout Pointers, retrieve offset of "Boot Partition 1 (BP1)" (offset value located @ 35:32 within layout pointers).</li><li>5. "Boot Partition 1" starts with BPD1 structure. Within BPD1 find the BPD1 Entry for "PMC" (type 14 or 0xE) and manually Corrupt the 4KB pointed by sub-partition offset [do 4 KB erase] and save as "Corrupted_PMC.bin" (See BPD1 details above).</li><li>6. While system is in G3, flash Corrupted_PMC.bin image to SPI</li><li>7. Power up SUT and boot to OS (expect to see global reset)</li><li>8. Confirm the following:<ol style="list-style-type: none"><li>a. MEInfo shows: "Current Boot Partition" = "2".</li><li>b. FWSTS1.bit0-3 (Current State): Normal [2].</li><li>c. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li></ol></li></ol>
<b>Test Pass/Fail Criteria</b>	<p>Pass: All below conditions must be met to pass the test:</p> <ol style="list-style-type: none"><li>1. MEInfo shows: "Current Boot Partition" = "2".</li><li>2. FWSTS1.bit0-3 (Current State): Normal [5]</li><li>3. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li></ol> <p>Fail: No Boot</p>



## 9.8 Critical Code Corruption - TypeC

<b>Test ID</b>	<b>Resilience_05</b>
<b>Test Case Title</b>	Critical Code Corruption – TypeC
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	The system is not in the Intel® ME Manufacturing Mode—when the system completes this test. This test is to confirm CSME can fallback to Backup copy of FTP (BC2) when BC1 is corrupted.
<b>Objective</b>	Verify Intel® CSME automatically falls back to BC2 when BC1 is corrupted.
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Build image using FIT with redundancy enabled: Build -&gt; Build Settings -&gt; under "Image Build Settings", set "Redundancy Enabled" to "True".</li> <li>2. Boot system at least once to OS.</li> <li>3. Place system in G3 and dump full SPI image.</li> <li>4. From Layout Pointers, retrieve offset of "Boot Partition 1 (BP1)" (offset value located @ 35:32 within layout pointers).</li> <li>5. "Boot Partition 1" starts with BPD1 structure. Within BPD1 find the BPD1 Entry for "IOM FW (TypeC)" (type 23 or 0x17) and manually Corrupt the 4KB pointed by sub-partition offset [do 4 KB erase] and save as "Corrupted_TypeC.bin" (See BPD1 details above).</li> <li>6. While system is in G3, flash Corrupted_TypeC.bin image to SPI</li> <li>7. Power up SUT and boot to OS (expect to see global reset)</li> <li>8. Confirm the following: <ol style="list-style-type: none"> <li>a. MEInfo shows: "Current Boot Partition" = "2".</li> <li>b. FWSTS1.bit0-3 (Current State): Normal [5]</li> <li>c. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li> </ol> </li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>Pass: All below conditions must be met to pass the test:</p> <ol style="list-style-type: none"> <li>1. MEInfo shows: "Current Boot Partition" = "2".</li> <li>2. FWSTS1.bit0-3 (Current State): Normal [5].</li> <li>3. FWSTS1.bit10 (BC1 Boot Failed): Yes [1].</li> </ol> <p>Fail: No Boot</p>



## 9.9 Recovery of Corrupted Primary Boot Critical (BC1) Partition

<b>Test ID</b>	<b>Resilience_06</b>
<b>Test Case Title</b>	Recovery of Corrupted Primary Boot Critical (BC1) Partition
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	The system is not in the Intel® ME Manufacturing Mode—when the system completes this test. This test is to confirm CSME can boot from primary FTP (BC1) after FWupdate repaired corruption
<b>Objective</b>	Verify Intel® CSME boot normally form BC1 after a successful FWUpdate repair BC1 corruption
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Perform Resilience_03 test above</li><li>2. Perform CSME FW Update (using FWUpdLcl or OEM Capsule update)</li><li>3. Confirm the following:<ol style="list-style-type: none"><li>a. MEInfo shows: "Current Boot Partition" = "1"</li><li>b. FWSTS1.bit0-3 (Current State): Normal [5]</li><li>c. FWSTS1.bit10 (BC1 Boot Failed): No [0]</li></ol></li></ol>
<b>Test Pass/Fail Criteria</b>	<p>Pass: All below conditions must be met to pass the test:</p> <ol style="list-style-type: none"><li>1. MEInfo shows: "Current Boot Partition" = "1"</li><li>2. FWSTS1.bit0-3 (Current State): Normal [5]</li><li>3. FWSTS1.bit10 (BC1 Boot Failed): No [0]</li></ol> <p>Fail: Any of below conditions can fail this test:</p> <ol style="list-style-type: none"><li>1. MEInfo shows: "Current Boot Partition" = "2"</li><li>2. FWSTS1.bit0-3 (Current State): Recovery [2]</li><li>3. FWSTS1.bit10 (BC1 Boot Failed): Yes [1]</li></ol>

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# 10 Intel® Active Management Technology (Intel® AMT) Tests

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This chapter covers Intel® AMT related features and technologies. Among those, the following features require BIOS and/or system integration:

- System Management BIOS (SMBIOS) and Alert Standard Format (ASF)
- BIOS Boot Option Support and Hardware Inventory
- Platform Event Trap (PET) and Boot Audit Event (BAE)
- Remote Power Control
- Serial-Over-LAN (SOL) and Storage Redirection
- Keyboard, Video and Mouse (KVM) redirection
- Remote Access (Fast Call for Help)
- Settings, Storage, and Security Configuration
- Remote Secure Erase

Intel® AMT feature integration with other Intel technologies, third-party technologies, and extensions of Intel® AMT are also covered:

- Intel® ME Power Gating
- Modern Standby
- Microsoft\* Windows InstantGo\*
- Discrete Graphics and Switchable Graphics
- Remote Screen Blank (RSB) (extension of Intel® AMT)
- Discrete LAN
- Host and dock TBT

## 10.1 Intel® AMT Over Different LAN Solutions

Intel® AMT legacy LAN solution is based on integrated LAN as part of PCH, Starting Comet Lake, AMT supports additional two LAN options as described below:

- **Discrete LAN:** The new generation of LAN supports 2.5G as discrete LAN. vPro system supports discrete LAN in order to provide the customer AMT features and use the benefit of 2.5G LAN.

An additional use case that is supported in TGL timeframe is Remote Intel AMT Manageability over a discrete NIC connected on board (such as FXVL GbE). The interfaces to the NIC is MCTP over PCIe and MCTP over SMBus, same interfaces used for OOB communication with NIC in the dock.

In a configuration where the integrated GbE is enabled (phy on board) and FXVL is also on board, AMT supports OOB manageability only over the integrated GbE

- **TBT Dock with discrete LAN:** Thunderbolt dock is an on-desk docking station that connects to the host through a USB TypeC cable and enables the connection of multiple peripherals (monitors, keyboard, mouse, wired network (Ethernet), printer, back-up drives, speakers, headset, etc.) and provides charging power to a laptop that is connected to the dock. Thunderbolt™ vPro™ dock connected to a Thunderbolt™ vPro™ supported host does all the above but also enables the vPro capabilities of the system across the network connection on the Thunderbolt™ vPro™ docking station. The Thunderbolt™ vPro™ Dock is connected to the



Thunderbolt™ vPro™ enabled laptop through Type C connector/cable using TBT technology. The system solution consists of a host implementing Thunderbolt vPro support connected directly to a stand-alone Thunderbolt™ docking device. The overall solution allows IT to remotely perform AMT management tasks on the PC connected to the dock – both In-Band and Out Of Band (OOB).

#### Active LAN Based on Dock Status:

Dock Status	Active Connectivity Type
Dock connected	LAN in dock + Wireless
Dock disconnected	Platform Integrated or discrete LAN + Wireless

#### Active BUS Based on Power State Status:

Power State	Active BUS	Comment
S0	PCI <sub>e</sub> or SMBUS	PCI <sub>e</sub> is active during TCPIP session.
S <sub>x</sub>	SMBUS	

## 10.2 Test System Power Model

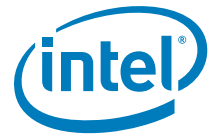
Each test in this chapter contains a table describing the system configuration to which the test is applicable. Below is an example environment for a given test:

Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input checked="" type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN

**Form Factor:** Describes the kind of system for which the test is applicable. These tests cover feature availability for associated platform. For Workstation form factors, the term 'Intel® AMT Server' may be also used for systems, which support Intel® AMT and run a server operating system.

**System Power Model:** Describes, which System Power Model the test is applicable under. A system with 'Standard' configuration follows traditional OS power model, wherein sending the system to Sleep results in S3 resting system state. Systems that support Modern Standby or Microsoft\* Windows InstantGo\* will move to S0 Low Power Idle state upon being sent to Sleep. This is usually defined by feature support relative to the operating system in conjunction with BIOS and system device support, but may also be due to the nature of the operating system itself relative to the goals of the test.

**Intel® AMT Network Interface:** Describes the Intel® AMT networking interface used by the test, if any. 'LAN' and 'WLAN' indicate that the test is explicitly using the respective LAN and/or wireless LAN (WLAN) interface. 'Either Used' indicates that an Intel® AMT network interface is used during the test, but the test itself is not specifically defined in which specific interface is to be used. 'Not Used' indicates that



the test procedure does not rely on the Intel® AMT network interface; even though Intel® Platform Enablement Test Suite (Intel® PETS) or other test methodology may require general networking access to the SUT.

**LAN Type:** Describe which LAN type is in used in the setup, it can be one of the three

- Integrated LAN: Integrated LAN which is part of PCH.
- Discrete LAN: Discrete LAN (a.k.a FXVL) in SUT.
- TBT Dock LAN: LAN which is located in TBT dock.

**Note:** Not all Workstation and Intel® AMT Server designs may have Intel® AMT wireless LAN interface support.

## 10.3 Test Coverage Summary

The following describes column in the test coverage summary below. The **Test ID** is the reference identifier for the test in this document and any related tools, which reference this document. The **Title** is the name of the test. The Requirement (**Req.**) column describes the requirement for test execution. The **Form Factor**, Operating System (**OS**), and Intel® AMT Network Interface (**Net**) indicate the applicable test system configuration (refer the [Section 10.2](#) for details). **How?** column describes the test methodology.

**Req.:** M = Mandatory, C = Conditional<sup>1</sup>, and O = Optional

<sup>1</sup> Considered the same as Mandatory but with exemptions. Refer test for details.

**Form Factor:** D = Desktop, M = Mobile, and W = Workstation

**Power Model:** S = Standard, and M/I = Modern Standby or Microsoft\* Windows\* InstantGo\* (refer above for details)

**Net:** L = LAN, W = WLAN, E = Either Used, and N = Not Used

**LAN Type:** **I** = Integrated LAN, **D** = Discrete LAN in SUT, **T** = TBT Dock LAN, **E** = Either Used, and **N** = Not Used

**How?:** A = Fully automated using Intel® PETS, I = Interactive using Intel® PETS automation, and M = Manual

**Table 10-2. Intel® AMT Test Coverage Summary**

Test ID	Title	Req.	Form Factor D M W	Power Model S M/I	Net	LAN Type	How?
<b>BIOS Tables</b>							
AMT_001	System Management BIOS (SMBIOS) Table Generation	M	☑ ☑ ☑	☑ ☑	N	N	I
AMT_002	Alert Standard Format (ASF) Table Generation	M	☑ ☑ ☑	☑ ☑	N	N	I
<b>Boot Options, Platform Event Traps, Hardware Assets, and Boot Audit Entry</b>							
AMT_010	BIOS Boot Option Read and Clear	M	☑ ☑ ☑	☑ ☑	E	E	I
AMT_011	Platform Event Trap (PET) Boot Progress Event Support	M	☑ ☑ ☑	☑ ☑	E	E	I
AMT_013	BIOS Hardware Asset Table Update	M	☑ ☑ ☑	☑ ☑	E	E	I
AMT_014	Boot Audit Entry (BAE) Platform Event Trap (PET) Support	M	☑ ☑ ☑	☑ ☑	E	E	I



Table 10-2. Intel® AMT Test Coverage Summary

Test ID	Title	Req.	Form Factor D M W	Power Model S M/I	Net	LAN Type	How?
AMT_015	Boot Audit Entry (BAE) Platform Event Trap (PET) Support with Alternate Boot Device	C	☑ ☑ ☑	☑ ☑	E	E	I
<b>Remote Power Control</b>							
AMT_020	Remote Power Control via Intel® AMT LAN Network Interface for Mobile Systems	M	☐ ☑ ☐	☑ ☑	L	E	A
AMT_021	Remote Power Control via Intel® AMT WLAN Network Interface for Mobile Systems	M	☐ ☑ ☐	☑ ☑	W	N	A
AMT_022	Remote Power Control via Intel® AMT LAN Network Interface for Non-Mobile Systems	M	☑ ☐ ☑	☑ ☐	L	E	A
AMT_023	Remote Power Control via Intel® AMT WLAN Network Interface for Non-Mobile Systems	M	☑ ☐ ☑	☑ ☐	W	N	A
AMT_024	Remote Power Control with S0 Low Power Idle via Intel® AMT LAN Network Interface	M	☐ ☑ ☐	☐ ☑	L	E	I
AMT_025	Remote Power Control with S0 Low Power Idle via Intel® AMT WLAN Network Interface	M	☐ ☑ ☐	☐ ☑	W	N	I
AMT_026	Remote Power Control via Intel® AMT WLAN Network Interface for Mobile Systems supporting Wake On Wireless LAN	C	☐ ☑ ☐	☑ ☐	W	N	A
AMT_027	Remote Power Control via Intel® AMT WLAN Network Interface for Non-Mobile Systems supporting Wake On Wireless LAN	C	☑ ☐ ☑	☑ ☐	W	N	A
AMT_028	Remote Power Control with Host OS interaction via Intel® AMT LAN Network Interface	M	☑ ☑ ☑	☑ ☑	L	E	A
AMT_029	Remote Power Control with Host OS interaction via Intel® AMT WLAN Network Interface	M	☑ ☑ ☑	☑ ☑	W	N	A
<b>Serial-Over-LAN (SOL) and Storage Redirection</b>							
AMT_030	Serial-Over-LAN (SOL) Redirection and BIOS Setup Boot Option over Intel® AMT LAN Network Interface	C	☑ ☑ ☑	☑ ☑	L	E	I
AMT_031	Serial-Over-LAN (SOL) Redirection and BIOS Setup Boot Option over Intel® AMT WLAN Network Interface	C	☑ ☑ ☑	☑ ☑	W	N	I
AMT_032	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT LAN Network Interface	M	☑ ☑ ☑	☑ ☑	L	E	I
AMT_033	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT WLAN Network Interface	M	☑ ☑ ☑	☑ ☑	W	N	I
AMT_034	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT LAN Network Interface with User Consent Enabled	M	☑ ☑ ☑	☑ ☑	L	E	I
AMT_035	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT WLAN Network Interface with User Consent Enabled	M	☑ ☑ ☑	☑ ☑	W	N	I
AMT_036	Serial-Over-LAN (SOL) and Storage Redirection with Secure Boot	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_037	Serial-Over-LAN (SOL) Character Interpretation	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_038	Serial-Over-LAN (SOL) Redirection during System Restart	O	☑ ☑ ☑	☑ ☑	E	E	I
<b>Keyboard, Video, and Mouse (KVM) Redirection</b>							
AMT_040	Keyboard, Video, and Mouse (KVM) Redirection and BIOS Setup Boot Option over Intel® AMT LAN Network Interface	C	☑ ☑ ☑	☑ ☑	L	E	I
AMT_041	Keyboard, Video, and Mouse (KVM) Redirection and BIOS Setup Boot Option over Intel® AMT WLAN Network Interface	C	☑ ☑ ☑	☑ ☑	W	N	I
AMT_042	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT LAN Network Interface	C	☑ ☑ ☑	☑ ☑	L	E	I





Table 10-2. Intel® AMT Test Coverage Summary

Test ID	Title	Req.	Form Factor D M W	Power Model S M/I	Net	LAN Type	How?
AMT_043	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT WLAN Network Interface	C	☑ ☑ ☑	☑ ☑	W	N	I
AMT_044	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT LAN Network Interface with User Consent Enabled	C	☑ ☑ ☑	☑ ☑	L	E	I
AMT_045	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT WLAN Network Interface with User Consent Enabled	C	☑ ☑ ☑	☑ ☑	W	N	I
AMT_046	Keyboard, Video, and Mouse (KVM) Redirection during Warm Reset over Intel® AMT LAN Network Interface	C	☑ ☑ ☑	☑ ☑	L	E	I
AMT_047	Keyboard, Video, and Mouse (KVM) Redirection during Warm Reset over Intel® AMT WLAN Network Interface	C	☑ ☑ ☑	☑ ☑	W	N	I
AMT_048	Keyboard, Video, and Mouse (KVM) Redirection with S0 Low Power Idle via Intel® AMT LAN Network Interface	C	☐ ☑ ☐	☐ ☑	L	E	I
AMT_049	Keyboard, Video, and Mouse (KVM) Redirection with S0 Low Power Idle via Intel® AMT WLAN Network Interface	C	☐ ☑ ☐	☐ ☑	W	N	I
AMT_050	Keyboard, Video, and Mouse (KVM) Redirection in Discrete Graphics Mode	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_051	Keyboard, Video, and Mouse (KVM) Redirection and Switchable Graphics	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_052	Keyboard, Video, and Mouse (KVM) with Serial-Over-LAN (SOL) and Storage Redirection	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_053	Keyboard, Video, and Mouse (KVM) and USB Port Availability Check	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_054	Keyboard, Video, and Mouse (KVM) with Remote Screen Blank (RSB) Support	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_055	Keyboard, Video, and Mouse (KVM) with S0 Low Power Idle and Intel® ME Power Gating	C	☐ ☑ ☐	☐ ☑	W	E	I
AMT_056	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT WLAN Network Interface for Systems supporting Wake On Wireless LAN	C	☑ ☑ ☑	☑ ☐	W	N	I
AMT_059	Keyboard, Video, and Mouse (KVM) Redirection on Headless Configurations	C	☑ ☑ ☑	☑ ☑	E	E	I
<b>Remote Access (Fast Call for Help)</b>							
AMT_060	Fast Call for Help During System Boot	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_061	Fast Call for Help from Outside the Enterprise	O	☑ ☑ ☑	☑ ☑	E	E	I
AMT_062	Fast Call for Help from Inside the Enterprise	O	☑ ☑ ☑	☑ ☑	E	E	I
<b>Settings, Storage, and Security Configuration</b>							
AMT_070	General Settings Information	O	☑ ☑ ☑	☑ ☑	E	E	A
AMT_071	Security Administration Realm Interface	O	☑ ☑ ☑	☑ ☑	E	E	A
AMT_073	Transport Layer Security (TLS) Authentication	O	☑ ☑ ☑	☑ ☑	E	E	I
AMT_074	Alarm Wake from S5	O	☑ ☑ ☑	☑ ☑	E	E	A
AMT_075	Alarm Wake from S4	O	☑ ☑ ☑	☑ ☑	E	E	A
AMT_076	Alarm Wake from S3	O	☑ ☑ ☑	☑ ☑	E	E	A
<b>Remote Secure Erase</b>							
AMT_080	Clear Remote Secure Erase Boot Option	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_081	Remote Secure Erase without Drive Authentication	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_082	Remote Secure Erase with Drive Authentication via Serial-Over-LAN (SOL) Redirection	C	☑ ☑ ☑	☑ ☑	E	E	I



Table 10-2. Intel® AMT Test Coverage Summary

Test ID	Title	Req.	Form Factor D M W	Power Model S M/I	Net	LAN Type	How?
AMT_083	Remote Secure Erase with Drive Authentication via Keyboard, Video, and Mouse (KVM) Redirection	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_084	Remote Secure Erase with Drive Authentication via Direct Password Input	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_085	Remote Secure Erase with Drive Authentication Failure via SOL Redirection	C	☑ ☑ ☑	☑ ☑	E	E	I
AMT_086	Remote Secure Erase with Drive Authentication Failure via Direct Password Input	C	☑ ☑ ☑	☑ ☑	E	E	I
<b>Wire Connectivity Tests in Different Power States</b>							
AMT_090	Wired connectivity check in S0	M	☑ ☑ ☑	☑ ☐	L	D, T	A
AMT_091	Wired and wireless connectivity's check in S0	M	☑ ☑ ☑	☑ ☐	L,W	D	A
AMT_092	Wired connectivity check in S3	M	☑ ☑ ☑	☑ ☐	L	D, T	A
AMT_093	Wired connectivity check in S4	M	☑ ☑ ☑	☑ ☐	L	D, T	A
AMT_094	Wired connectivity check in S5	M	☑ ☑ ☑	☑ ☐	L	D, T	A
AMT_095	Wired Remote Power Control transition Check	M	☑ ☑ ☑	☑ ☐	L	D, T	A
AMT_096	Wired Connection Check Using IPV6	M	☑ ☑ ☑	☑ ☐	L	D, T	M
<b>AMT Over TBT Dock</b>							
AMT_100	Wired connectivity check in S0 with different TBT dock states.	M	☐ ☑ ☐	☑ ☐	L	T	I
AMT_101	Wired connectivity check in S3 with different TBT dock states.	M	☐ ☑ ☐	☑ ☐	L	T	I
AMT_102	Wired connectivity check in S4 with different TBT dock states.	M	☐ ☑ ☐	☑ ☐	L	T	I
AMT_103	Wired connectivity check in S5 with different TBT dock states.	M	☐ ☑ ☐	☑ ☐	L	T	I
AMT_104	Wired Remote Power Control transition Check with different TBT dock states.	M	☐ ☑ ☐	☑ ☐	L	T	I
AMT_106	Wired-Wireless connectivity check with connected TBT dock event.	M	☐ ☑ ☐	☑ ☐	L,W	T	I
AMT_107	Wired <b>IPV6</b> connectivity check in S0 with different TBT dock states.	M	☐ ☑ ☐	☑ ☐	L	T	M
AMT_108	Integrated\Discrete LAN connectivity check while dock is connected.	M	☐ ☑ ☐	☑ ☐	L	T	I
AMT_109	Wireless connectivity check with TBT dock which doesn't support vPro.	M	☐ ☑ ☐	☑ ☐	L	T	I

### 10.3.1 Test Environment Setup

When completing tests within this chapter, especially those which send the system to a specific S-state (S3, S4, S5, Deep Sx, etc.), it is important to ensure that the network wake events are properly configured for each applicable device (LAN and/or WLAN).

If not properly configured, the system may wake from a given S-state unexpectedly during test execution as a result of various network traffic within the test environment, and cause the test to result in a *false failure*.

The following Host OS LAN/WLAN driver settings allow the network device to process specific network frames **without** waking the system, where supported.

- Address Resolution Protocol (ARP) offload should be **enabled**.
- Neighbor Solicitation (NS) offload should be **enabled**.

The following Host OS LAN/WLAN driver settings allow the network device to wake the system, where supported, when specific network frames are received.



- Wake on Magic Packet should be **disabled**.
- Wake on Pattern Match should be **disabled**.
- Wake on Magic Packet from power off state should be **disabled**.

**Note:**

The wording used for the Host OS driver settings above may vary, and in some cases may not be available depending on driver support or system configuration.

For Wake on Wireless LAN testing described in this chapter, the following Host OS WLAN driver settings should be used:

- Allow device to wake the computer should be **enabled**.
- Allow the computer to turn off this device to save power should be **enabled**.
- Allow only Magic Packet to wake the computer should be **disabled**.
- Wake on Magic Packet should be **enabled**.
- Wake on Pattern Match should be **enabled**.

Beyond the guidance in this section, refer individual test setup information for details on specifically, when to enable relevant wake functionality in the network device, as applicable to the test. In all other cases, the above settings should be applied by default.

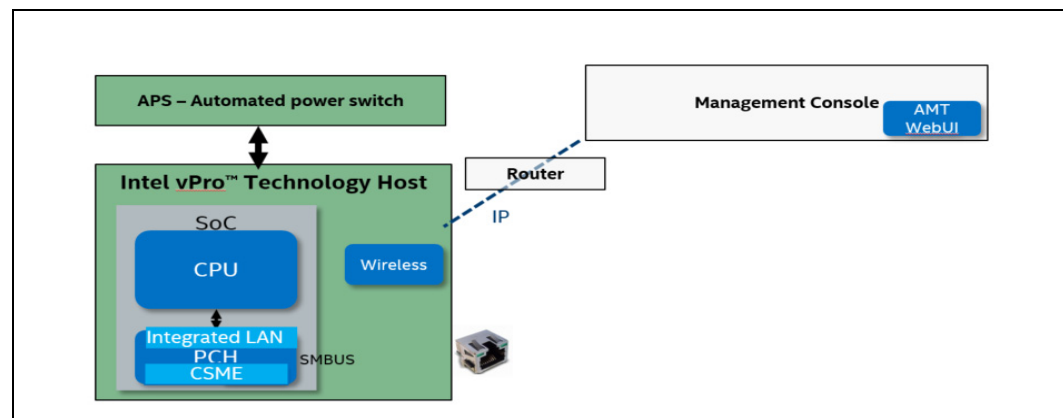
**Note:**

When WLAN network interface is used, ensure the TCP maximum data retransmission setting defined in the SUT profile applied both Management Console and SUT via Intel® AMT. If the configuration on the management console is not already aligned to the SUT profile setting, the network stack on the management console will need to be reset; leading to potential network connectivity loss for other applications on the system.

### 10.3.1.1 Setup of AMT Over Integrated LAN or WLAN

AMT over discrete LAN system contains the following ingredients:

- Desktop \ Workstation platform which contains:
  - Intel WLAN
  - Intel Integrated LAN



### 10.3.1.2 Intel® AMT Over Discrete LAN or WLAN Setup

AMT over discrete LAN system contains the following ingredients:

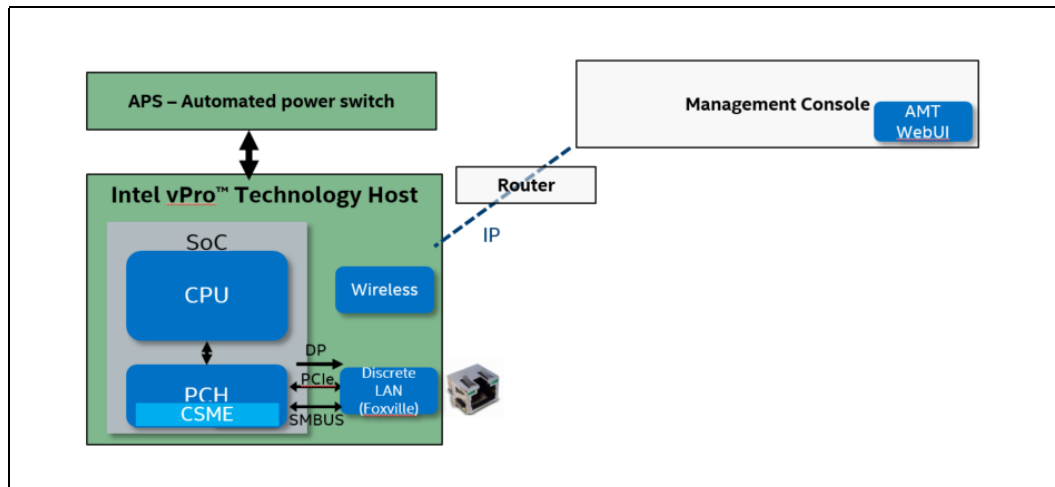
- Desktop \ Workstation platform which contains:

- Intel WLAN
- Intel discrete NIC

**Note:**

The tools below are required for system environment tests:

- Intel® LANCONF - Latest version of LAN tool from this KIT.
- Intel® MEManuf - Latest version of CSME tool from this KIT.
- Intel® MEInfo - Latest version of CSME tool from this KIT.



### 10.3.1.3 Intel® AMT Over TBT Dock or WLAN Setup

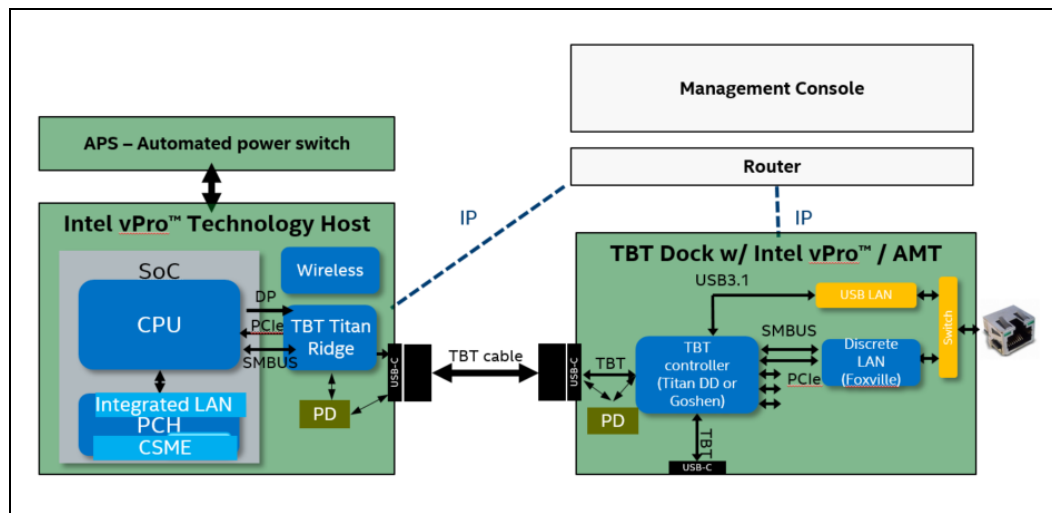
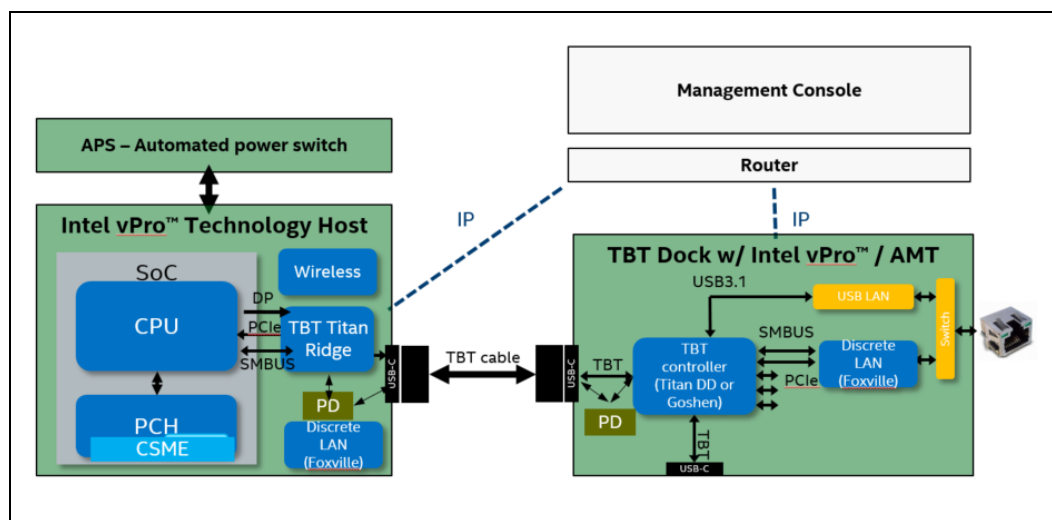
Setup of AMT over TBT Dock contains the following ingredients:

- Mobile platform which contains:
  - Intel WLAN
  - Intel integrated LAN
  - Intel TBT, burnside bridge or above
  - PD
- TBT dock station (Intel Reference TBT dock "Gatex Creek" or OEM TBT dock design)
  - Intel discrete LAN (such as FXVL I225-LM)
  - PD
  - TBT Goshen Ridge or above

**Note:**

The tools below are required for system environment tests:

- Intel® LANCONF - Latest version of LAN tool from this KIT.
- Intel® TenLira- Latest version of TBT tool from this KIT.
- Intel® MEManuf - Latest version of CSME tool from this KIT.
- Intel® MEInfo - Latest version of CSME tool from this KIT.

**AMT with SUT Integrated LAN and TBT Dock:****AMT with SUT Discrete LAN and TBT Dock:****10.3.2 WSMAN Commands Definition**

The table below describes the relevant WSMAN commands which are used during the tests to perform specific activity.

The command belows are used by PETS. In some cases WebUI application can be used to achieve same functionality.

WSMAN	Description	Supported By
AMT_EthernetPortSettings->PhysicalNicMedium	Query which BUS is active, SMBUS or PCIe?	PETS
AMT_GeneralSetting->ThunderboltDockEnabled	Query is vPro TBT dock is enabled in BIOS Values { "Disabled", "Enabled" }	PETS



WSMAN	Description	Supported By
CIM_SoftwareIdentity->VersionString	Query ME firmware version	PETS and WebUI
AMT_EthernetPortSettings	Query SMBUS type in used, Values { "SMBUS", "PCIe", "Reserved"}]	PETS

### 10.3.3 Setup Environment Tests

The following tests are defined as Setup Environment Test (SET) tests. These are intended to confirm basic test environment configuration and should be run before any other automated test described in this chapter.

#### 10.3.3.1 Intel® AMT Basic Connectivity with Integrated LAN and WLAN

ID	Check Intel® AMT Connectivity			
<b>Title</b>	Intel® AMT basic connectivity check in S0 with Host OS available			
<b>Requirement</b>	Optional			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	Before any testing is to begin, it is critical to confirm network connectivity with Intel® AMT. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.			
<b>Objective</b>	Verify that the Management Console can communicate with Intel® AMT on the SUT.			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Prompt the test operator to confirm that:               <ol style="list-style-type: none"> <li>The SUT supports Intel® AMT.</li> <li>The Host OS is booted on the SUT.</li> <li>Intel® AMT is provisioned on the SUT.</li> <li>The network connection to the Host OS on the SUT is confirmed for <b>all</b> available network interfaces.</li> </ol> </li> <li>Query the Intel® ME firmware and confirm that Intel® AMT is available.</li> <li>Verify on the SUT that:               <ol style="list-style-type: none"> <li>The Intel® MEI driver is installed.</li> <li>The Local Manageability Service (LMS) is installed and running.</li> </ol> </li> <li>Check on the SUT that the Intel® Management and Security Status (Intel® MSS) is installed and issue a warning otherwise (do not fail the test).</li> <li>Confirm for the following configuration information provided to Intel® PETS that:               <ol style="list-style-type: none"> <li>The administrator password for Intel® AMT is of a valid length.</li> <li>The IP address used to connect with Intel® AMT is valid.</li> </ol> </li> <li>If the WLAN network interface is available:               <ol style="list-style-type: none"> <li>Query the Intel® ME firmware and verify, there is no wireless micro-code mismatch.</li> <li>Verify that the Host OS WLAN profile and WLAN profile configured in Intel® AMT have the same Network Authentication and Encryption method settings applied.</li> </ol> </li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>			
<b>Pass Criteria</b>	The test passes, if all the steps above pass without failure.			



10.3.3.2

ID	Check Intel® AMT Feature Support			
<b>Title</b>	Intel® AMT basic feature support check in S0 with Host OS available.			
<b>Requirement</b>	Optional			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS			
<b>Description</b>	Before any testing is to begin, it is critical to confirm feature configuration check with Intel® AMT. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.			
<b>Objective</b>	Verify that the Intel® AMT on the SUT is properly configured to enable feature integration testing.			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
<b>Procedure</b>	1. Read the platform UUID and confirm that it is not all zero. 2. Query Intel® AMT and confirm that KVM support is enabled. 3. Query Intel® AMT and confirm that KVM is enabled in Intel® MEBX. 4. Verify that the Intel® AMT Serial-Over-LAN (SOL) device is available in the Host OS. 5. Verify that the Intel® AMT SOL and Storage Redirection features are enabled in Intel® MEBX by checking, if their interface state can be enabled. 6. Verify basic Windows* Management Instrumentation (WMI) support is available from Intel® AMT on the SUT by querying the <code>\$\$OsAdmin</code> account.			
<b>Pass Criteria</b>	The test passes, if all the steps above pass without failure.			

### 10.3.3.3 AMT Basic Connectivity with Discrete LAN and WLAN

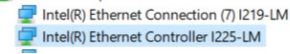
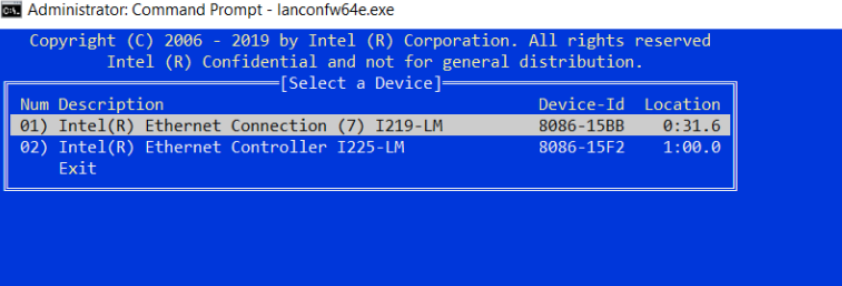
ID	Check Intel® AMT Connectivity using LAN Discrete			
<b>Title</b>	Intel® AMT basic connectivity check in S0 with Host OS available while <b>using LAN discrete.</b>			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Manual.			
<b>Description</b>	Before any testing is to begin, it is critical to confirm system readiness and check connectivity with Intel® AMT using discrete LAN.			
<b>Objective</b>	Verify vPro™ system readiness and check Management Console can communicate with Intel® AMT using discrete LAN.			



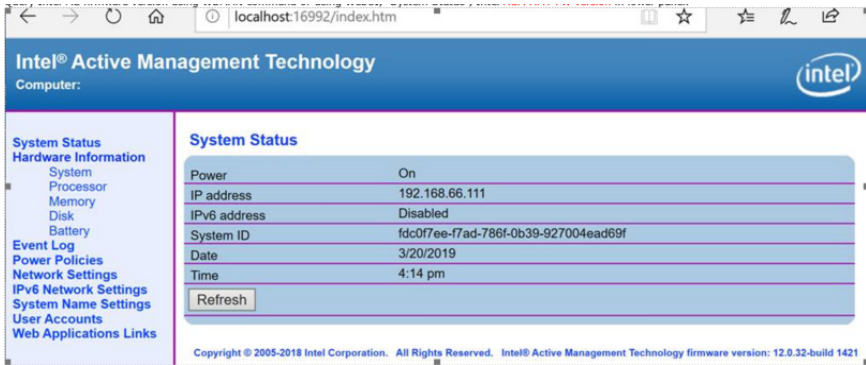
ID	Check Intel® AMT Connectivity using LAN Discrete																								
Setup	<p><b>NOTE:</b> Refer to vPro™ over LAN discrete <b>bring up guide</b> for details about setup preparation before continue to the steps below.</p> <ol style="list-style-type: none"><li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li><li>2. Intel AMT should be provisioned via manual mode.</li><li>3. IFWI image which enables discrete LAN in IFWI using FIT as defined below.</li></ol> <table><tr><th>Parameter</th><th>Value</th></tr><tr><td>Platform Discrete vPro NIC Enabled</td><td>YES</td></tr><tr><td>Platform Discrete vPro NIC SMBUS slave address</td><td>OEM specific</td></tr><tr><td>vPro Dock Enabled</td><td>NO</td></tr><tr><td>vPro NIC on dock slave SMBUS address</td><td>N/A</td></tr><tr><td>Type-C Port1 Tre-Timer I2C Address</td><td>N/A</td></tr><tr><td>Type-C Port2 Tre-Timer I2C Address</td><td>N/A</td></tr><tr><td>Type-C Port3 Tre-Timer I2C Address</td><td>N/A</td></tr><tr><td>Type-C Port4 Tre-Timer I2C Address</td><td>N/A</td></tr></table> <ol style="list-style-type: none"><li>4. BIOS setting should be set as follow:<table><tr><th>Parameter</th><th>Value</th></tr><tr><td>Intel Advanced Menu -&gt; PCH-FW Configuration -&gt; ME Debug Configuration -&gt; MCTP Broadcast Cycle</td><td>Enabled</td></tr><tr><td>TBT Setting....</td><td>N/A</td></tr></table></li></ol> <p><b>NOTE:</b> The BIOS item above is defined in Intel reference BIOS.</p> <ol style="list-style-type: none"><li>5. Install the following drivers from the KIT:<ol style="list-style-type: none"><li>a. MEI full drivers installation (includes LMS)</li><li>b. Discrete LAN</li></ol></li><li>6. Flash the following firmware ingredients:<ol style="list-style-type: none"><li>a. IFWI</li><li>b. Discrete LAN firmware</li></ol></li><li>7. SUT power port should be connected to power supply. AC-DC mode.</li><li>8. Connect SUT to Ethernet.</li><li>9. Verify SUT wireless connectivity available.</li><li>10. Copy MEInfo, MEManuf and LANConf tools to SUT host file system.</li></ol>	Parameter	Value	Platform Discrete vPro NIC Enabled	YES	Platform Discrete vPro NIC SMBUS slave address	OEM specific	vPro Dock Enabled	NO	vPro NIC on dock slave SMBUS address	N/A	Type-C Port1 Tre-Timer I2C Address	N/A	Type-C Port2 Tre-Timer I2C Address	N/A	Type-C Port3 Tre-Timer I2C Address	N/A	Type-C Port4 Tre-Timer I2C Address	N/A	Parameter	Value	Intel Advanced Menu -> PCH-FW Configuration -> ME Debug Configuration -> MCTP Broadcast Cycle	Enabled	TBT Setting....	N/A
Parameter	Value																								
Platform Discrete vPro NIC Enabled	YES																								
Platform Discrete vPro NIC SMBUS slave address	OEM specific																								
vPro Dock Enabled	NO																								
vPro NIC on dock slave SMBUS address	N/A																								
Type-C Port1 Tre-Timer I2C Address	N/A																								
Type-C Port2 Tre-Timer I2C Address	N/A																								
Type-C Port3 Tre-Timer I2C Address	N/A																								
Type-C Port4 Tre-Timer I2C Address	N/A																								
Parameter	Value																								
Intel Advanced Menu -> PCH-FW Configuration -> ME Debug Configuration -> MCTP Broadcast Cycle	Enabled																								
TBT Setting....	N/A																								





ID	Check Intel® AMT Connectivity using LAN Discrete
<p><b>Procedure</b></p>	<p><b>System Readiness Checks</b></p> <p>Request the test operator to perform the following steps</p> <ol style="list-style-type: none"> <li>Open Device manager and check the following drivers installation status:             <ol style="list-style-type: none"> <li>LAN</li> </ol> </li> </ol> <p><b>NOTE:</b> In case platform has also integrated LAN, two LAN instances should be displayed, One for integrated LAN (I219-LM) and second for discrete LAN (I225-LM), a.k.a FXVL.</p>  <ol style="list-style-type: none"> <li>MEI, view it under 'System Devices' tree</li> <li>LMS, view it under Windows Services</li> </ol> <ol style="list-style-type: none"> <li>Steps a through d, if the BIOS settings have <b>NOT</b> already been confirmed             <ol style="list-style-type: none"> <li>Boot the SUT to the BIOS menu.</li> <li>Verify the following BIOS values according to table in setup section.</li> <li>Save any BIOS settings changes.</li> <li>Shutdown the SUT to S5.</li> </ol> </li> <li>Turn on SUT and enter MEBX menu,</li> <li>Verify AMT is provisioned properly, if not, do AMT provisioning.</li> <li>Save any MEBX settings changes.</li> <li>Continue to load OS</li> <li>Verify link and firmware readiness by running CSME and LAN tools from host             <ol style="list-style-type: none"> <li>Run MEInfo -V to query CSME version.</li> <li>Run LANConf and verify discrete LAN appears, In case of FXVL discrete, Instance of LAN i225-LM should be displayed. Note: In case integrated LAN exists as well, two LAN instances should be displayed.</li> </ol> </li> </ol>  <ol style="list-style-type: none"> <li>Select LAN discrete instance and query firmware version using EPROM-&gt;NVM Image.</li> </ol> <ol style="list-style-type: none"> <li>Connect Ethernet cable to SUT and verify host OS network connection is functional properly using discrete LAN.</li> <li>Verify network connection using wireless.</li> </ol>



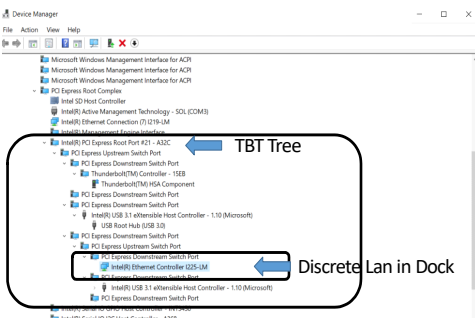
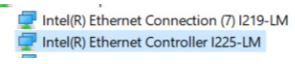
<b>ID</b>	<b>Check Intel® AMT Connectivity using LAN Discrete</b>
<b>Procedure (continued)</b>	<p><b>Basic Functionality Tests</b></p> <p>10. Open SUT local WebUI using browser, http://127.0.0.1:16992</p> <p>11. Login to AMT system</p> <p>12. Open "System Status" screen and verify Intel AMT FW version in lower panel.</p>  <p>13. Open System Information screen.</p> <p>14. Verify AMT IP is same as Host IP.</p> <p>15. Open remote WebUI using browser, http://&lt;SUT&gt;:16992</p> <p>16. Login to AMT system</p> <p>Check AMT firmware version.</p>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	For details on setup preparation, refer to the <i>Intel® AMT Over Discrete LAN bring up guide</i> .

### 10.3.3.4 Intel® AMT Basic Connectivity with WLAN, TBT Dock, and SUT Integrated LAN

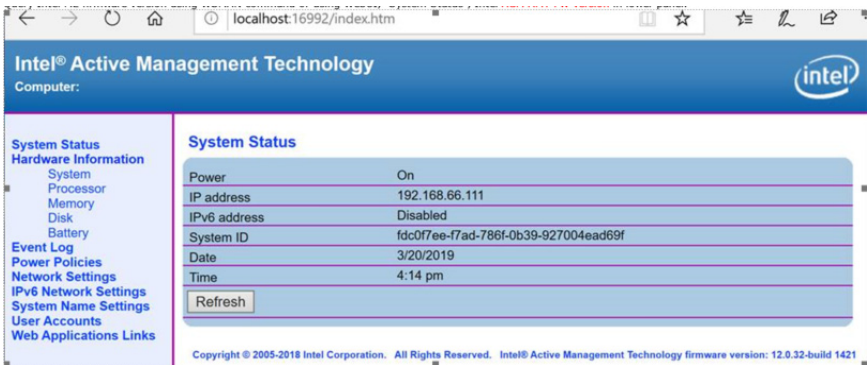
ID	Check Intel® AMT Connectivity using TBT dock station and SUT Integrated LAN																			
Title	Intel® AMT basic connectivity check in S0 with Host OS available while <b>using integrated LAN and TBT dock</b> .																			
Requirement	Mandatory.																			
System	<table><thead><tr><th>Form Factor</th><th>System Power Model</th><th>Intel® AMT Network Interface</th><th>LAN Type</th></tr></thead><tbody><tr><td><input type="checkbox"/> Desktop    <input type="checkbox"/> Workstation</td><td><input checked="" type="checkbox"/> Standard</td><td><input checked="" type="checkbox"/> LAN    <input type="checkbox"/> Either Used</td><td><input checked="" type="checkbox"/> Integrated LAN</td></tr><tr><td><input checked="" type="checkbox"/> Mobile</td><td><input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input checked="" type="checkbox"/> WLAN    <input type="checkbox"/> Not Used</td><td><input type="checkbox"/> Discrete LAN</td></tr><tr><td></td><td></td><td></td><td><input checked="" type="checkbox"/> TBT Dock LAN</td></tr></tbody></table>	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type	<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Integrated LAN	<input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Discrete LAN				<input checked="" type="checkbox"/> TBT Dock LAN			
Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type																	
<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used	<input checked="" type="checkbox"/> Integrated LAN																	
<input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Discrete LAN																	
			<input checked="" type="checkbox"/> TBT Dock LAN																	
Method	Manual.																			
Description	Before any testing is to begin, it is critical to confirm network connectivity with Intel® AMT using TBT dock. <b>NOTE:</b> This test assumes that mobile system and TBT dock with all relevant Ingredients are available, refer to test setup paragraph for more information.																			
Objective	Verify AMT over TBT dock system readiness and check Management Console can communicate with Intel AMT using integrated LAN and TBT dock station.																			



ID	Check Intel® AMT Connectivity using TBT dock station and SUT Integrated LAN																								
Setup	<p><b>NOTE:</b> Refer to AMT over TBT Dock bring up guide for details about setup preparation before continue to steps below.</p> <ol style="list-style-type: none"> <li>The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>Intel® AMT should be provisioned via manual mode.</li> <li>SUT should support vPro using TBT dock.</li> <li>IFWI image which enables integrated LAN and vPro dock as defined in FIT below:</li> </ol> <table border="1"> <thead> <tr> <th>Parameter</th><th>Value</th></tr> </thead> <tbody> <tr> <td>Platform Discrete vPro NIC Enabled</td><td>NO</td></tr> <tr> <td>Platform Discrete vPro NIC SMBUS slave address</td><td>N/A</td></tr> <tr> <td>vPro Dock Enabled</td><td>YES</td></tr> <tr> <td>vPro NIC on dock slave SMBUS address</td><td>OEM specific</td></tr> <tr> <td>Type-C Port1 Tre-Timer I2C Address</td><td>OEM specific</td></tr> <tr> <td>Type-C Port2 Tre-Timer I2C Address</td><td>OEM specific</td></tr> <tr> <td>Type-C Port3 Tre-Timer I2C Address</td><td>OEM specific</td></tr> <tr> <td>Type-C Port4 Tre-Timer I2C Address</td><td>OEM specific</td></tr> </tbody> </table> <ol style="list-style-type: none"> <li>BIOS setting should be set as below:  <b>NOTE:</b> For BIOS TBT setting, refer to vPro over TBT dock bring up guide for full setting list.</li> </ol> <table border="1"> <thead> <tr> <th>Parameter</th><th>Value</th></tr> </thead> <tbody> <tr> <td>Intel Advanced Menu -&gt; PCH-FW Configuration -&gt; ME Debug Configuration -&gt; MCTP Broadcast Cycle</td><td>Enabled</td></tr> <tr> <td>TBT Setting....</td><td>Refer to TBT BIOS setting guide</td></tr> </tbody> </table> <ol style="list-style-type: none"> <li>Install the following drivers from the KIT: <ol style="list-style-type: none"> <li>MEI full drivers installation (includes LMS)</li> <li>Thunderbolt™</li> <li>LAN</li> </ol> </li> <li>Flash the following firmware ingredients: <ol style="list-style-type: none"> <li>IFWI</li> <li>Discrete LAN in dock</li> <li>TBT in SUT and in dock</li> </ol> </li> <li>TBT dock should be connected to SUT.</li> <li>TBT dock should be connected to power supply.</li> <li>SUT power port should be connected to power dedicated power port (not TBT data port). AC-DC mode.</li> <li>Connect dock to Ethernet.</li> <li>Verify SUT wireless connectivity.</li> <li>Copy MEInfo, MEManuf, LANConf, TenLira to SUT Host OS file system.</li> </ol>	Parameter	Value	Platform Discrete vPro NIC Enabled	NO	Platform Discrete vPro NIC SMBUS slave address	N/A	vPro Dock Enabled	YES	vPro NIC on dock slave SMBUS address	OEM specific	Type-C Port1 Tre-Timer I2C Address	OEM specific	Type-C Port2 Tre-Timer I2C Address	OEM specific	Type-C Port3 Tre-Timer I2C Address	OEM specific	Type-C Port4 Tre-Timer I2C Address	OEM specific	Parameter	Value	Intel Advanced Menu -> PCH-FW Configuration -> ME Debug Configuration -> MCTP Broadcast Cycle	Enabled	TBT Setting....	Refer to TBT BIOS setting guide
Parameter	Value																								
Platform Discrete vPro NIC Enabled	NO																								
Platform Discrete vPro NIC SMBUS slave address	N/A																								
vPro Dock Enabled	YES																								
vPro NIC on dock slave SMBUS address	OEM specific																								
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TBT Setting....	Refer to TBT BIOS setting guide																								

ID	Check Intel® AMT Connectivity using TBT dock station and SUT Integrated LAN
<p><b>Procedure</b></p>	<p><b>System Readiness Checks</b></p> <p>Request the test operator to perform the following steps</p> <ol style="list-style-type: none"> <li>Open Device manager and check the following drivers installation status:             <ol style="list-style-type: none"> <li>TBT, TBT device should be appear, discrete LAN should be appear under PCIe TBT root tree.</li> </ol> </li> </ol>  <ol style="list-style-type: none"> <li>LAN driver                     <p>Note: Two LAN instances should be displayed, one for integrated LAN and second for discrete LAN in dock (e.g FXVL as I225).</p> </li> </ol>  <ol style="list-style-type: none"> <li>MEI driver</li> <li>LMS in services</li> </ol> <ol style="list-style-type: none"> <li>Steps a through d, if the BIOS settings have <b>NOT</b> already been confirmed             <ol style="list-style-type: none"> <li>Boot the SUT to the BIOS menu.</li> <li>Verify the following BIOS values according to table in setup section.</li> <li>Save any BIOS settings changes.</li> <li>Shutdown the SUT to S5.</li> </ol> </li> <li>Turn on SUT and enter MEBX menu,</li> <li>Verify AMT is provisioned properly, if not, do AMT provisioning.</li> <li>Save any MEBX settings changes.</li> <li>Continue to load OS</li> <li>Verify link and firmware readiness by running CSME, LAN and TBT tools from host OS file system,             <ol style="list-style-type: none"> <li>Run MEInfo -V to query CSME version.</li> <li>Run TenLira and check link to TBT dock.</li> <li>Run LANConf and verify discrete LAN appears, In case of FXVL discrete, Instance of LAN I225-LM should be displayed. Note: In case integrated LAN exists as well, two LAN instances should be displayed.</li> <li>Select LAN discrete instance and query firmware version using EPROM menu</li> <li>Query PD firmware version using BIOS menu.</li> </ol> </li> <li>Verify host OS network connection is functional properly using LAN in TBT dock.</li> <li>Disconnect the TBT dock and connect Ethernet cable to SUT.</li> <li>Verify host OS network connection is functional properly using LAN in SUT.</li> </ol>



<b>ID</b>	<b>Check Intel® AMT Connectivity using TBT dock station and SUT Integrated LAN</b>
<b>Procedure (Continued)</b>	<p><b>Basic Functionality Tests</b></p> <ol style="list-style-type: none"> <li>Open SUT local WebUI using browser, http://127.0.0.1:16992</li> <li>Login to AMT system</li> <li>Open "System Status" screen and verify Intel AMT FW version in lower panel.</li> </ol>  <ol style="list-style-type: none"> <li>Verify AMT IP is same as Host IP.</li> <li>Disconnect Ethernet cable from SUT</li> <li>Connect TBT dock to SUT and verify Ethernet cable is connected to dock.</li> <li>Query TBT dock IP using ipconfig command.</li> <li>From Management Console, open remote WebUI using TBT IP and port.</li> <li>Login to AMT</li> <li>Open AMT System Information screen.</li> <li>Verify CSME firmware version.</li> <li>Disconnect the dock and connect Ethernet cable to SUT.</li> <li>Query SUT IP using ipconfig command.</li> <li>From Management Console, open remote WebUI using SUT Integrated LAN IP and port.</li> <li>Login to AMT</li> <li>Open AMT System Information screen.</li> <li>Verify CSME firmware version.</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	For details on setup preparation, refer to the <i>AMT over TBT Dock bring up guide</i> .

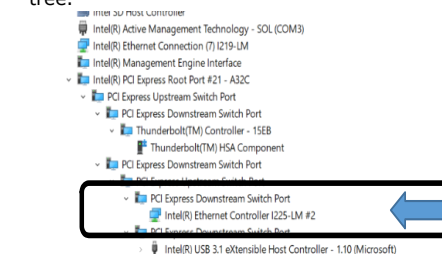

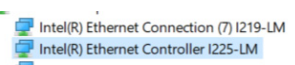
### 10.3.3.5 Intel® AMT Basic Connectivity with WLAN, TBT Dock, and Discrete SUT LAN

<b>ID</b>	<b>Check Intel® AMT Connectivity using TBT dock station and SUT discrete LAN</b>			
<b>Title</b>	Intel® AMT basic connectivity check in S0 with Host OS available while <b>using discrete LAN and TBT dock</b> .			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Manual.			
<b>Description</b>	<p>Before any testing is to begin, it is critical to confirm network connectivity with Intel® AMT using TBT dock.</p> <p><b>NOTE:</b> This test assumes that mobile system and TBT dock with all relevant Ingredients are available, refer to test setup paragraph for more information.</p>			




ID	Check Intel® AMT Connectivity using TBT dock station and SUT discrete LAN																								
Objective	Verify AMT over TBT dock system readiness and check Management Console can communicate with Intel AMT using discrete LAN and TBT dock station.																								
Setup	<p><b>NOTE:</b> Refer to vPro bring up guide for details about setup preparation before continue to steps below.</p> <ol style="list-style-type: none"><li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li><li>2. Intel® AMT should be provisioned via manual mode.</li><li>3. SUT should support vPro using TBT dock.</li><li>4. IFWI image which enables integrated LAN and vPro dock as defined in FIT below:</li></ol> <table><tr><th>Parameter</th><th>Value</th></tr><tr><td>Platform Discrete vPro NIC Enabled</td><td>YES</td></tr><tr><td>Platform Discrete vPro NIC SMBUS slave address</td><td>OEM specific</td></tr><tr><td>vPro Dock Enabled</td><td>YES</td></tr><tr><td>vPro NIC on dock slave SMBUS address</td><td>OEM specific</td></tr><tr><td>Type-C Port1 Tre-Timer I2C Address</td><td>OEM specific</td></tr><tr><td>Type-C Port2 Tre-Timer I2C Address</td><td>OEM specific</td></tr><tr><td>Type-C Port3 Tre-Timer I2C Address</td><td>OEM specific</td></tr><tr><td>Type-C Port4 Tre-Timer I2C Address</td><td>OEM specific</td></tr></table> <p>5. BIOS setting should be set as below:</p> <p><b>NOTE:</b> For BIOS TBT setting, refer to vPro over TBT dock bring up guide for full setting list.</p> <table><tr><th>Parameter</th><th>Value</th></tr><tr><td>Intel Advanced Menu -&gt; PCH-FW Configuration -&gt; ME Debug Configuration -&gt; MCTP Broadcast Cycle</td><td>Enabled</td></tr><tr><td>TBT Setting....</td><td>Refer to TBT BIOS setting guide</td></tr></table> <ol style="list-style-type: none"><li>6. Install the following drivers from the KIT:<ol style="list-style-type: none"><li>a. MEI full drivers installation (includes LMS)</li><li>b. Thunderbolt™</li><li>c. LAN</li></ol></li><li>7. Flash the following firmware ingredients:<ol style="list-style-type: none"><li>a. IFWI</li><li>b. Discrete LAN in dock</li><li>c. TBT in SUT and in dock</li></ol></li><li>8. TBT dock should be connected to SUT.</li><li>9. TBT dock should be connected to power supply.</li><li>10. SUT power port should be connected to power dedicated power port (not TBT data port). AC-DC mode.</li><li>11. Connect dock to Ethernet.</li><li>12. Verify SUT wireless connectivity.</li><li>13. Copy MEInfo, MEManuf, LANConf, TenLira to SUT Host OS file system.</li></ol>	Parameter	Value	Platform Discrete vPro NIC Enabled	YES	Platform Discrete vPro NIC SMBUS slave address	OEM specific	vPro Dock Enabled	YES	vPro NIC on dock slave SMBUS address	OEM specific	Type-C Port1 Tre-Timer I2C Address	OEM specific	Type-C Port2 Tre-Timer I2C Address	OEM specific	Type-C Port3 Tre-Timer I2C Address	OEM specific	Type-C Port4 Tre-Timer I2C Address	OEM specific	Parameter	Value	Intel Advanced Menu -> PCH-FW Configuration -> ME Debug Configuration -> MCTP Broadcast Cycle	Enabled	TBT Setting....	Refer to TBT BIOS setting guide
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ID	Check Intel® AMT Connectivity using TBT dock station and SUT discrete LAN
<p><b>Procedure</b></p>	<p><b>System Readiness Checks</b></p> <p>Request the test operator to perform the following steps</p> <ol style="list-style-type: none"> <li>Open Device manager and check the following drivers installation status:             <ol style="list-style-type: none"> <li>TBT device should be appear, discrete LAN should be appear under PCIe TBT root tree.</li> </ol> </li> </ol>   <ol style="list-style-type: none"> <li>LAN</li> </ol> <p><b>NOTE:</b> Two LAN instances should be display, one for integrated LAN and second for discrete LAN in dock (e.g FXVL as I225).</p>  <ol style="list-style-type: none"> <li>MEI</li> <li>LMS service in Windows services</li> </ol> <ol style="list-style-type: none"> <li>Steps a through d, if the BIOS settings have <b>NOT</b> already been confirmed             <ol style="list-style-type: none"> <li>Boot the SUT to the BIOS menu.</li> <li>Verify the following BIOS values according to table in setup section.</li> <li>Save any BIOS settings changes.</li> <li>Shutdown the SUT to S5.</li> </ol> </li> <li>Turn on SUT and enter MEBX menu,</li> <li>Verify AMT is provisioned properly, if not, do AMT provisioning.</li> <li>Save any MEBX settings changes.</li> <li>Continue to load OS</li> <li>Verify link and firmware readiness by running CSME, LAN and TBT tools from host OS file system,             <ol style="list-style-type: none"> <li>Run MEInfo -V to query CSME version</li> <li>Run TenLira and check link to TBT dock.</li> <li>Run LANConf and verify discrete LAN appears, In case of FXVL discrete, Instance of LAN i225-LM should be displayed. Note: In case integrated LAN exists as well, two LAN instances should be displayed.</li> <li>Select LAN discrete instance and query firmware version using EPROM menu</li> <li>Query PD firmware version using BIOS menu.</li> </ol> </li> <li>Verify host OS network connection is functional properly using LAN in TBT dock.</li> <li>Disconnect the TBT dock and connect Ethernet cable to SUT.</li> <li>Verify host OS network connection is functional properly using LAN in SUT.</li> </ol>



ID	Check Intel® AMT Connectivity using TBT dock station and SUT discrete LAN
Procedure	<b>Basic Functionality Tests</b> 11. Open SUT local WebUI using browser, http://127.0.0.1:16992 12. Login to AMT system 13. Open "System Status" screen and verify Intel AMT FW version in lower panel. 
	14. Verify AMT IP is same as Host IP. 15. Connect TBT dock to SUT and verify Ethernet cable is connected to dock and . 16. Query TBT dock IP using ipconfig command. 17. From Management Console, open remote WebUI using TBT IP and port. 18. Login to AMT 19. Open AMT System Information screen. 20. Verify CSME firmware version. 21. Disconnect the dock and connect Ethernet cable to SUT, discrete LAN RJ45 connector. 22. Query SUT discrete LAN IP using ipconfig command. 23. From Management Console, open remote WebUI using SUT discrete LAN IP and port. 24. Login to AMT 25. Open AMT System Information screen. 26. Verify CSME firmware version.
Pass Criteria	This test passes if each of the step above passed successfully.
References	For details on setup preparation, refer to the <i>AMT Over TBT Dock bring up guide</i> .

## 10.4 BIOS Tables

The section serves as a checklist for the environment setup and testing of BIOS tables.

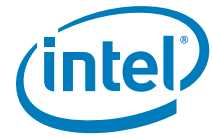
### 10.4.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows\* supported by Intel® PETS, and the SUT should have a version of Microsoft\* Windows\* supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one system drive attached.

#### Tools for Testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.





- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.



## 10.4.2 SMBIOS Table Generation

ID	AMT_001			
Title	System Management BIOS (SMBIOS) Table Generation			
Requirement	Mandatory			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input checked="" type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	<p>During POST, the BIOS creates several tables used by Intel® AMT. The BIOS communicates these tables to Intel® ME for storage.</p> <p>There are two aspects to this requirement:</p> <ol style="list-style-type: none"> <li>1. The tables exist and are formatted correctly within the SMBIOS Type Structures Table.</li> <li>2. Verify that the data is being transferred correctly to the Intel® ME.</li> </ol> <p>These tables include critical data used during Intel® AMT operation along with the following:</p> <ul style="list-style-type: none"> <li>• Type 0 - BIOS Information</li> <li>• Type 1 - System Information</li> <li>• Type 2 - Baseboard (or Module) Information</li> <li>• Type 3 - System Enclosure or Chassis</li> <li>• Type 4 - Processor Information</li> <li>• Type 17 - Memory Device</li> <li>• Type 18 - Memory Error Information (Optional)</li> <li>• Type 19 - Memory Array Mapped Address</li> <li>• Type 22 - Portable Battery (Optional)</li> <li>• Type 27 - Cooling Device (Optional)</li> <li>• Type 130 - Intel® AMT Specific</li> <li>• Type 131 - Intel® CSME Platform</li> </ul>			
Objective	Verify that the BIOS has created the required table data and communicated data to Intel® ME for storage.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
Procedure	<ol style="list-style-type: none"> <li>1. Extract the following SMBIOS Structures Table locally from the SUT and verify all SMBIOS tables existed automatically. Save the SMBIOS Structures Table to PETS log.             <ul style="list-style-type: none"> <li>• BIOS Information</li> <li>• System Information</li> <li>• Baseboard (or Module) Information</li> <li>• System Enclosure or Chassis</li> <li>• Processor Information</li> <li>• Memory Device</li> <li>• Memory Error Information (Optional)</li> <li>• Memory Array Mapped Address</li> <li>• Portable Battery (Optional)</li> <li>• Cooling Device (Optional)</li> <li>• Intel® AMT Specific</li> <li>• Intel® Management Engine Platform</li> </ul> </li> </ol> <p><b>NOTE:</b> For tables defined by Intel, only those with a length matching specification shall be saved. Those which are not aligned to Intel specification shall not be saved.</p> <ol style="list-style-type: none"> <li>2. Inform Test operator SMBIOS Structures Table are saved to PETS log and can review the tables and to verify that:             <ol style="list-style-type: none"> <li>i. All of the expected tables listed are included</li> <li>ii. All of the tables are formatted correctly</li> </ol> </li> </ol>			



ID	AMT_001
<b>Procedure</b> (continued)	3. Verify that the following tables are present with a length aligned to specification: <ul style="list-style-type: none"> <li>• Type 0 – BIOS Information</li> <li>• Type 1 – System Information</li> <li>• Type 2 – Baseboard (or Module) Information</li> <li>• Type 3 – System Enclosure or Chassis</li> <li>• Type 4 – Processor</li> <li>• Type 17 – Memory Device</li> <li>• Type 19 – Memory Array Mapped Address</li> </ul> 4. Verify fixed data in the SMBIOS Type 130 Intel® AMT Specific table. 5. Verify configurable data in SMBIOS Type 130 Intel® AMT Specific table. 6. If Table SMBIOS Type 22 Portable Battery or SMBIOS Type 27 Cooling Device are available, display them to the test operator, and request them to confirm that they are correct. 7. Open a remote connection to the SUT and display the information exposed by means of the Hardware Asset interface, and request the user to confirm that the information is correct. This will confirm that Asset Information is being generated and reported to Intel® ME for storage.
<b>Pass Criteria</b>	The test passes, if all the tables are correctly implemented with correct information.
<b>References</b>	For details on Type 130 and Type 131 tables, refer to the <i>Intel® ME BIOS Specification</i> .



### 10.4.3 ASF Table Generation

ID	AMT_002			
Title	Alert Standard Format (ASF) Table Generation			
Requirement	Mandatory			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input checked="" type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant BIOS must generate the following ASF tables and send this information to the Intel® ME firmware: <ul style="list-style-type: none"><li>• ASF! Description Table</li><li>• ASF_INFO</li><li>• ASF_ALRT</li><li>• ASF_RCTL</li><li>• ASF_RMCP</li><li>• ASF_ADDR</li></ul>			
Objective	Verify that BIOS creates the various ASF! Table Structures required for Intel® AMT functionality. The structures contain the information required by Intel® AMT for remote control, sensor polling, and boot options support.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
Procedure	<ol style="list-style-type: none"><li>1. Request Test Operation to fill in the following information:<ul style="list-style-type: none"><li>– If the SUT supports a Watchdog Timer</li><li>– System ID (OEM specific)</li><li>– IANA Manufacturer ID (OEM specific)</li><li>– If Sensors are supported</li><li>– Boot Options Capabilities with their supported/non-supported status</li><li>– RMCP Special Commands with their supported/non-supported status</li></ul></li><li>2. Extract the ASF! Tables locally from the SUT.</li><li>3. Verify that the Minimum Watchdog Reset value in ASF_INFO is 0 if watchdog timer is not supported, and some other value if it is supported.</li><li>4. Verify if the System ID from the ASF tables is valid.</li><li>5. Verify if the IANA Manufacturer ID from the ASF tables is valid.</li><li>6. Verify if all sensors are correct.</li><li>7. Verify that the ASF_RCTL structure contains the following remote operation command/data pairings:<ul style="list-style-type: none"><li>• 00h/03h - System reset</li><li>• 00h/02h - System power off</li><li>• 00h/01h - System power on</li><li>• 00h/04h - System power cycle reset</li></ul></li><li>8. Verify that the RMCP Boot Options Capabilities Bit Mask from ASF_RMCP table data:<ul style="list-style-type: none"><li>• Fields 16-31 must be 0x0.</li><li>• Fields 7-10 must be 0x0.</li><li>• Fields 3-4 must be 0x0.</li></ul></li><li>9. Verify all the Boot Options Capabilities from the RMCP Boot Options Capabilities Bit Mask in the ASF_RMCP table data.</li><li>10. Verify that the RMCP Special Commands Bit Mask in the ASF_RMCP table data:<ul style="list-style-type: none"><li>• Fields 13-15 must be 0x0.</li><li>• Fields 0-7 must be 0x0.</li></ul></li><li>11. Verify the RMCP Special Commands from the RMCP Special Commands Bit Mask in the ASF_RMCP table data.</li><li>12. Verify, if the ASF_ADDR table data is correct.</li></ol>			



ID	AMT_002
Procedure (continued)	<p>13. Extract the following remote control capabilities from both the BIOS and via the Intel® AMT network interface, and verify that they are identical:</p> <p><b>Boot Options (System Firmware) Capabilities</b></p> <ul style="list-style-type: none"> <li>· Firmware Verbosity/Screen Blank</li> <li>· Power Button Lock</li> <li>· Reset Button Lock</li> <li>· Lock Keyboard</li> <li>· Sleep Button Lock</li> <li>· User Password Bypass</li> <li>· Forced Progress Events</li> <li>· Firmware Verbosity/Verbose</li> <li>· Firmware Verbosity/Quiet</li> <li>· Configuration Data Reset</li> </ul> <p><b>Special Commands</b></p> <ul style="list-style-type: none"> <li>· Force PXE Boot</li> <li>· Force Hard-drive Boot</li> <li>· Force Hard-drive Safe-mode Boot</li> <li>· Force Diagnostic Boot</li> <li>· Force CD/DVD Boot</li> </ul> <p><b>System Capabilities</b></p> <ul style="list-style-type: none"> <li>· Power-Cycle Reset</li> <li>· Power-Down only</li> <li>· Power-Up</li> <li>· Reset</li> </ul> <p><b>Recommended Step (not included with any Intel-provided tool):</b> Use an SMBus sniffer to verify sensor polling is done according to the sensor in ASF_ALRT table.</p>
Pass Criteria	The test passes, if the Intel® PETS and the test operator are able to verify that all the tables have valid data.
References	The structure and description of the ASF tables can be found at the DMTF website in document DSP0136 at <a href="http://dmtof.org">http://dmtof.org</a> .

## 10.5 Boot Options, Platform Event Traps, Hardware Assets, and Boot Audit Entry

The section serves as a checklist for the environment setup and covers integration testing of BIOS boot options, Platform Event Traps (PET), hardware asset push, and Boot Audit Entry (BAE) event features in Intel® AMT.

### 10.5.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows supported by Intel® PETS, and the SUT should have a version of Microsoft\* Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one system drive attached.

#### Tools for testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliance and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.
- Bootable CD/DVD with OS for applicable tests.



Where applicable, the wireless LAN interface on Intel® AMT must be on a different network/subnet than the wired LAN interface. For details on how to enter the network interface details into Intel® PETS, consult the Intel® PETS User Guide.



## 10.5.2 BIOS Boot Option Read and Clear

ID	AMT_010			
Title	BIOS Boot Option Read and Clear			
Requirement	Mandatory			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	When the BIOS executes before OS boot, the BIOS must read the boot options from the Intel® ME by means of the Get Boot Options command. This test verifies that the BIOS reads and executes the sent options, and also clears the options for next boot.			
Objective	<p>Verify that the BIOS reads and executes boot options as specified by the remote console and then clears the options for next boot.</p> <p>Intel® AMT enables remote management of the platform, including providing capabilities to receive the boot options sent from a management console. Once the BIOS has successfully read the boot options, the BIOS must then reset/clear the sent boot options on the local Intel® AMT platform, so as to return it to the default state for the next boot.</p>			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. There should be only one bootable system drive attached to the SUT. Where attached, remove any additional bootable system drives from the SUT before testing.</p>			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>Obtain the boot options available from the SUT via Intel® AMT. Some systems may not support all possible boot options like force boot to CD/DVD device.</li> <li>Display the boot options supported by the SUT and ask the test operator to select a special command, plus one or more system boot capabilities.</li> </ol> <p>Special Commands:</p> <ul style="list-style-type: none"> <li>No Operation</li> <li>Force PXE Boot</li> <li>Force Hard Drive Boot</li> <li>Force Diagnostic Boot</li> <li>BIOS Pause</li> </ul> <p>System Boot Capabilities:</p> <ul style="list-style-type: none"> <li>Lock Power Button</li> <li>Lock Reset Button</li> <li>Lock Keyboard</li> <li>Lock Sleep Button</li> <li>Safe Mode</li> <li>User Password Bypass</li> <li>Configuration Data Reset</li> <li>Firmware Verbosity (System Default, Quiet, Verbose, and Screen Blank)</li> </ul> <p><b>NOTE:</b> Boot options related to KVM and Storage Redirection, the boot Progress Events boot capability, the Force CD/DVD Boot capability, and the BIOS Setup boot capability will not be provided to the test operator. Testing related to those features shall be covered by other tests.</p>			



ID	AMT_010
Procedure (continued)	<ol style="list-style-type: none"><li>5. Use Intel® AMT to apply the boot options, as specified by the test operator, to the SUT for the next boot.</li><li>6. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li><li>7. Perform a Remote Power-Up of the SUT via Intel® AMT.</li><li>8. Wait for the SUT to return to S0/MeOn. The depending on the boot option selected, it shall not be possible for Intel® PETS to programmatically, confirm the Host OS or final S0 system operational state (e.g. Force PXE Boot).</li><li>9. Request the test operator to verify that the boot was performed with selected boot options.</li><li>10. Request the test operator to gracefully shutdown the SUT. Depending on the boot option selected, it shall not be possible for Intel® PETS to programmatically shut down the system gracefully in all cases.</li><li>11. Wait for the SUT to move to S5/MeOn.</li><li>12. Inform the test operator that a system boot will be performed by Intel® PETS with no special options.</li><li>13. Perform a Remote Power-Up of the SUT via Intel® AMT.</li><li>14. Wait for the SUT to return to S0/MeOn with the Host OS running.</li><li>15. Request the test operator to verify that the boot, without any boot options applied, was performed correctly.</li><li>16. Display instructions describing to re-run this test as many times as needed to cover all remaining untested boot options available on the SUT.</li></ol>
Pass Criteria	The test passes, if each of the specified boot options passes, and if the subsequent boot shows that the option was cleared.
References	For details on the BIOS boot options, refer to the <i>Intel® ME BIOS Specification</i> .





### 10.5.3 PET Boot Progress Event Support

ID	AMT_011			
Title	Platform Event Trap (PET) Boot Progress Event Support			
Requirement	Mandatory			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	When the boot options sent remotely indicate FORCE PROGRESS EVENTS, the BIOS shall send at least one of the following progress messages as a PET event: <ul style="list-style-type: none"> <li>• BIOS Present</li> <li>• MemInit</li> <li>• HddInit</li> <li>• BspInit</li> <li>• APInit</li> <li>• PciResConfig</li> <li>• VideoInit</li> <li>• KbcInit</li> <li>• OSBoot</li> </ul>			
Objective	Verify that the defined boot progress message PET events are being sent by the BIOS under the appropriate conditions.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
Procedure	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME in S0, wake in Sx/AC).</li> <li>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>3. Clear the Intel® AMT Event Manager log on the SUT.</li> <li>4. Use Intel® AMT to set the FORCE PROGRESS EVENTS boot option on the SUT for the next boot.</li> <li>5. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>6. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>7. Wait for the SUT to return to S0/MeOn with the Host OS running.</li> <li>8. Dump the Event Manager log to a local file on the SUT.</li> <li>9. Transfer the Event Manager log file from the SUT to the management console.</li> <li>10. On the management console, parse the Event Manager log to verify that atleast one boot progress message PET alert was sent.</li> <li>11. Display from the Event Manager log all of the PET alerts received during the boot.</li> <li>12. Request the test operator to inspect and confirm all of the PET alerts logged are accurate.</li> </ol>			
Limitations	Intel provides no direct test for the other PET events and error/warning messages that the BIOS might have in-full or in-part. As such, the following recommendation is provided: <ol style="list-style-type: none"> <li>1. Test for PET alerts on all tests available for the SUT.</li> <li>2. Conduct a BIOS code review for all PET events not tested.</li> </ol> It is up to the BIOS vendor to verify implementation of retransmission mechanism per the Intel® ME BIOS Specification recommendations.			
Pass Criteria	The test passes, when atleast one of the progress message PET alerts are received, and code review shows that messages will be sent in cases not tested.			
References	For details on boot progress PET events, refer to the <i>Intel® ME BIOS Specification</i> .			

### 10.5.4 BIOS Hardware Asset Table Update

ID	AMT_013
Title	BIOS Hardware Asset Table Update



ID	AMT_013			
Requirement	Mandatory			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant BIOS shall implement appropriate Hardware Asset management.			
Objective	Verify that the BIOS reports add-on devices installed in the system.			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that Storage Redirection is enabled in the Intel® MEBX.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>If WLAN card is used as the additional PCI add-on card, the Wi-Fi function is not relevant to this test.</li> <li>If PCIe* SSD device is used as the additional PCI add-on device, additional Media device is added in the Hardware Asset table.</li> </ol>			
Procedure	<ol style="list-style-type: none"> <li>Before the test start, pop-up a message to inform user "Additional PCI card is required for this test. Prepare an add-on card that is applicable to SUT and leave it un-attached. The add-on card will be attached and detached during the test."</li> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>Retrieve the Hardware Asset information from the SUT via Intel® AMT.</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Use Intel® AMT to set the boot options to Force Storage Redirection Boot on the SUT for the next boot.</li> <li>Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to a redirected ISO OS image (without Serial-Over-LAN).</li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Wait for the SUT to return to S0/MeOn.</li> <li>Retrieve the Hardware Asset information from the SUT via Intel® AMT.</li> <li>Close the Storage Redirection session with the SUT via Intel® AMT.</li> <li>Perform a Remote Power-Down of the SUT via Intel® AMT.</li> </ol>			



<b>ID</b>	<b>AMT_013</b>
<b>Pass Criteria</b>	The test passes, if Intel® PETS detects a change in the Hardware Asset list, when the PCI device is added, there is no change after removal (as compared to the configuration at the start of the test), and Storage Redirection session does not result in any change in the Hardware Asset list.
<b>References</b>	For details on BIOS hardware asset tables sent to Intel® AMT, refer to the <i>Intel® ME BIOS Specification</i> .

## BAE PET Support

<b>ID</b>	<b>AMT_014</b>			
<b>Title</b>	Boot Audit Entry (BAE) Platform Event Trap (PET) Support			
<b>Requirement</b>	Mandatory			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	A Boot Audit Entry (BAE) Platform Event Trap (PET) alert must be sent, when booting to the default hard drive before passing control to the OS.			
<b>Objective</b>	Verify that a BAE PET alert indicating a normal boot is sent, when the system boots from the local hard drive for the third time in a row.			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>Clear the Intel® AMT Event Manager log on the SUT.</li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Wait for the SUT to return to S0/MeOn with the Host OS running.</li> <li>Repeat steps 3 through 5 each two more times. This yields a total three boots to the hard drive.</li> <li>Dump the Event Manager log to a local file on the SUT.</li> <li>Transfer the Event Manager log file from the SUT to the management console.</li> <li>On the management console, parse the Event Manager log, and verify that the most recent BAE PET alert sent by the SUT indicates a normal boot with the following Event Data:               <ul style="list-style-type: none"> <li>Event Data 1 is set to 0x40 (Progress Event)</li> <li>Event Data 2 is set to 0x13 (System Boot)</li> </ul> </li> </ol>			
<b>Pass Criteria</b>	The test passes, if all of the following are confirmed: <ul style="list-style-type: none"> <li>The SUT boots to the hard drive each time a normal boot is performed.</li> <li>BAE PET alert indicating normal boot is sent, when a normal boot is performed third time in a row (most BIOS implementations will indicate via BAE PET alert that a normal boot occurred the second time the system is booted).</li> </ul>			
<b>References</b>	For details on BAE PET events, refer to the <i>Intel® ME BIOS Specification</i> .			



## 10.5.5 BAE PET Support with Alternate Boot Device

ID	AMT_015			
Title	Boot Audit Entry (BAE) Platform Event Trap (PET) Support with Alternate Boot Device			
Requirement	Mandatory - exempt for systems that have <b>no</b> internal or removable CD/DVD drive support and can only boot via external USB-connected CD/DVD drive.			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	The BIOS must override the BIOS Boot Specification (BBS) table, when boot options are set, which designate a different boot device. A Boot Audit Entry (BAE) Platform Event Trap (PET) alert must be sent, when a new boot device has been designated between boots, or a boot is performed from an alternate device.			
Objective	Verify that the BIOS follows the specified boot option or defaults to the standard, when no boot option is sent. Verify that a BAE PET alert is sent, when the boot device is changed, or the SUT is booting from a removable device. Verify that a BAE PET alert indicating a normal boot is sent, when the system boots from the local hard drive for the second time in a row.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. This test checks multiple different boot flows to different devices including CD/DVD. Ensure to prepare a system which has a CD/DVD drive attached with bootable media inserted.			
Procedure	1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC). 2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used. 3. Clear the Intel® AMT Event Manager log on the SUT. 4. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b> . 5. Use Intel® AMT to set the boot option to Force CD/DVD Boot on the SUT for the next boot. 6. Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to the CD/DVD device. 7. Perform a Remote Power-Up of the SUT via Intel® AMT. 8. Wait for the SUT to return to S0/MeOn. It is not possible for Intel® PETS to programmatically confirm that the SUT actually booted to CD/DVD. 9. Request the test operator to: a. Confirm that system booted to the CD/DVD. b. Gracefully shutdown the SUT. 10. Wait for the SUT to move to S5/MeOn.			
	11. Use Intel® AMT to set the boot option to force CD/DVD Boot on the SUT for the next boot again. 12. Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to the CD/DVD device. 13. Perform a Remote Power-Up of the SUT via Intel® AMT. 14. Wait for the SUT to return to S0/MeOn. It is not possible for Intel® PETS to programmatically confirm that the SUT actually booted to CD/DVD. 15. Request the test operator to: a. Confirm that system booted to the CD/DVD. b. Gracefully shutdown the SUT, and c. Boot the SUT to Host OS. 16. Wait for the SUT to return to S0/MeOn with the Host OS running. 17. Dump the Event Manager log to a local file on the SUT. 18. Transfer the Event Manager log file from the SUT to the management console. 19. On the management console, parse the Event Manager log, and verify that the most recent BAE PET alert sent by the SUT indicates a 'unusual event' boot with the following Event Data: — Event Data 1 is set to 0xAA (OEM Specific). — Event Data 2 is set to 0x13 (System Boot). — Event Data 3 is set to 0x02 (Most Recent BAE: Boot to hard drive). — Event Data 4 is set to 0x03 (Next Most Recent BAE: Boot to removable device). — Event Data 5 is set to 0x03 (Oldest BAE: Boot to removable device).			



ID	AMT_015
Pass Criteria	<p>The test passes, if all of the following are confirmed:</p> <ul style="list-style-type: none"> <li>The SUT boots to CD/DVD when the boot option is set, and to the hard drive, when a normal boot is performed.</li> <li>BAE PET alert indicating new/removable device sent, whenever the boot device is changed, or boot performed from a removable device.</li> </ul>
References	For details on BAE PET events, refer to the <i>Intel® ME BIOS Specification</i> .

## 10.6 Remote Power Control

The section serves as a checklist for the environment setup and covers integration testing of the Remote Power Control feature in Intel® AMT.

### 10.6.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows supported by Intel® PETS, and the SUT should have a version of Microsoft\* Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one system drive attached.

#### Tools for Testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT

Where applicable, the wireless LAN interface on Intel® AMT must be on a different network/subnet than the wired LAN interface. For details on how to enter the network interface details into Intel® PETS, consult the Intel® PETS User Guide.

If the firmware image or the SUT configuration does not support some features, Intel® PETS will show those features as failing when tested. Intel® PETS cannot determine in all cases, which features have been deactivated and should thus be skipped during testing.



## 10.6.2 Remote Power Control via Intel® AMT LAN Network Interface for Mobile Systems

ID	AMT_020																													
Title	Remote Power Control via Intel® AMT LAN Network Interface for Mobile Systems																													
Requirement	Mandatory																													
System	<table><tr><th>Form Factor</th><th>System Power Model</th><th>Intel® AMT Network Interface</th><th colspan="2">LAN Type</th></tr><tr><td><input type="checkbox"/> Desktop   <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile</td><td><input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*</td><td><input checked="" type="checkbox"/> LAN <input type="checkbox"/> WLAN   <input type="checkbox"/> Either Used                   <input type="checkbox"/> Not Used</td><td colspan="2"><input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN</td></tr></table>	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type		<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> WLAN <input type="checkbox"/> Either Used <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN																				
Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type																											
<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> WLAN <input type="checkbox"/> Either Used <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN																											
Method	Automated by Intel® PETS																													
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"><li>• Reset</li><li>• Power-Up</li><li>• Power-Down</li><li>• Power-Cycle</li></ul>																													
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (reset, power-on/off/cycle). This test verifies that the BIOS has been properly enabled to support these usage models.																													
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.																													
Procedure	<div><div><div>1. Ensure the system power configuration is set to AC/DC.</div><div>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</div><div>3. Perform the following remote control operations across the given power states:</div></div><table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5/DS5<sup>1</sup></td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr></table><div><p>Each flow in the table above shall be executed as, if they are part of an independent sub-test.</p><div>4. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:</div><div><div>a. If shutdown, briefly press the Power Button on the SUT.</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Record the Host OS last boot time on the SUT (to verify successful restart).</div><div>d. Perform a graceful restart of the SUT via Host OS.</div><div>e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</div></div><p>If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</p><p>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</p><div><div>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</div></div><p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</p><div><div>a. Bring the system to G3 and wait 10 seconds.</div><div>b. Set system power configuration to AC/DC and wait another 10 seconds.</div><div>c. Briefly press the Power Button on the SUT.</div></div></div></div>					SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>	S3->	N/A	N/A	N/A	N/A	S4->	N/A	N/A	N/A	N/A	S5->	N/A	N/A	N/A	N/A
SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																										
S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>																										
S3->	N/A	N/A	N/A	N/A																										
S4->	N/A	N/A	N/A	N/A																										
S5->	N/A	N/A	N/A	N/A																										



ID	AMT_020																									
Procedure (continued)	5. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).																									
	6. Perform the following remote control operations across the given power states:																									
	<table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr></table>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5	S3->	N/A	S0	S0	S5	S4->	N/A	N/A	S0	N/A	S5->	N/A	N/A	S0	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5																					
	S3->	N/A	S0	S0	S5																					
	S4->	N/A	N/A	S0	N/A																					
	S5->	N/A	N/A	S0	N/A																					
	Each flow in the table above shall be executed as, if they are part of an independent sub-test. In the case of Modern Standby or Microsoft* Windows InstantGo* mode, the S3 test flows shall be skipped.																									
	7. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows in the chart above, perform the following additional sub-steps for two cycles each after the remote control operation has completed:																									
a. If shutdown, briefly press the Power Button on the SUT.																										
b. Verify that the Host OS on the SUT is available.																										
c. Record the Host OS last boot time on the SUT (to verify successful restart).																										
d. Perform a graceful restart of the SUT via Host OS.																										
e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.																										
If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.																										
Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:																										
a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
b. Verify that the Host OS on the SUT is available.																										
c. Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.																										
If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.																										
a. Bring the system to G3 and wait 10 seconds.																										
b. Set system power configuration to AC/DC and wait another 10 seconds.																										
c. Briefly press the Power Button on the SUT.																										
8. Set the SUT to DC-only power and repeat steps 2 through 7. Verify that the relevant power flow operations match the table in both steps 3 and 6 for both Power Package 1 and Power Package 2 using their associated verification methods in steps 4 and 7 respectively.																										
<sup>1</sup> In the case of Power Package 1 configuration or DC-only power configuration testing, the SUT will enter the relative Deep Sx state, when the BIOS has enabled Deep Sx.																										
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.																									
References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> .																									



### 10.6.3 Remote Power Control via Intel® AMT WLAN Network Interface for Mobile Systems

ID	AMT_021				
Title	Remote Power Control via Intel® AMT WLAN Network Interface for Mobile Systems				
Requirement	Mandatory				
System	Form Factor	System Power Model	Intel® AMT Network Interface		LAN Type
	<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS				
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"><li>• Reset</li><li>• Power-Up</li><li>• Power-Down</li><li>• Power-Cycle</li></ul>				
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (reset, power-on/off/cycle). This test verifies that the BIOS has been properly enabled to support these usage models.				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.				





ID	AMT_021																									
Procedure	<div>1. Ensure the system power configuration is set to AC/DC.</div> <div>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</div> <div>3. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0).</div> <div>4. Ensure the Host OS Wake on Wireless LAN is <b>disabled</b>.</div> <div>5. Verify that Intel® AMT is available via WLAN by requesting its version.</div> <div>6. Perform the following remote control operations across the given power states:</div> <table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5/DS5<sup>1</sup></td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr></table> <div>Each flow in the table above shall be executed as, if they are part of an independent sub-test.</div> <div>7. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:</div> <div><div>a. If shutdown, briefly press the Power Button on the SUT.</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Record the Host OS last boot time on the SUT (to verify successful restart).</div><div>d. Perform a graceful restart of the SUT via Host OS.</div><div>e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</div></div> <div>If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</div> <div>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</div> <div><div>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</div></div> <div>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</div> <div><div>a. Bring the system to G3 and wait 10 seconds.</div><div>b. Set system power configuration to AC/DC and wait another 10 seconds.</div><div>c. Briefly press the Power Button on the SUT.</div></div>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>	S3->	N/A	N/A	N/A	N/A	S4->	N/A	N/A	N/A	N/A	S5->	N/A	N/A	N/A	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>																					
	S3->	N/A	N/A	N/A	N/A																					
	S4->	N/A	N/A	N/A	N/A																					
	S5->	N/A	N/A	N/A	N/A																					



ID	AMT_021																									
Procedure (continued)	8. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).																									
	9. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).																									
	10. Perform the following remote control operations across the given power states:																									
	<table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr></table>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5	S3->	N/A	S0	S0	S5	S4->	N/A	N/A	S0	N/A	S5->	N/A	N/A	S0	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5																					
	S3->	N/A	S0	S0	S5																					
	S4->	N/A	N/A	S0	N/A																					
	S5->	N/A	N/A	S0	N/A																					
	Each flow in the table above shall be executed as, if they are part of an independent sub-test. In the case of Modern Standby or Microsoft* Windows InstantGo* mode, the S3 test flows shall be skipped.																									
11. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows in the chart above, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:																										
a. If shutdown, briefly press the Power Button on the SUT.																										
b. Verify that the Host OS on the SUT is available.																										
c. Record the Host OS last boot time on the SUT (to verify successful restart).																										
d. Perform a graceful restart of the SUT via Host OS.																										
e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.																										
If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.																										
Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:																										
a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
b. Verify that the Host OS on the SUT is available.																										
c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.																										
If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.																										
a. Bring the system to G3 and wait 10 seconds.																										
b. Set system power configuration to AC/DC and wait another 10 seconds.																										
c. Briefly press the Power Button on the SUT.																										
12. Set the SUT to DC-only power and repeat steps 2 through 11. Verify that the relevant power flow operations match the table in step 6 for both Power Package 1 (Link Policy 2) and Power Package 2 (Link Policy 3) respectively.																										
<sup>1</sup> In the case of Power Package 1 configuration or DC-only power configuration testing, the SUT will enter the relative Deep Sx state when the BIOS has enabled Deep Sx.																										
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.																									
References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> .																									



## 10.6.4 Remote Power Control via Intel® AMT LAN Network Interface for Non-Mobile Systems

ID	AMT_022																												
Title	Remote Power Control via Intel® AMT LAN Network Interface for Non-Mobile Systems																												
Requirement	Mandatory																												
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type																									
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN																									
Method	Automated by Intel® PETS																												
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"> <li>• Reset</li> <li>• Power-Up</li> <li>• Power-Down</li> <li>• Power-Cycle</li> </ul>																												
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (reset, power-on/off/cycle). This test verifies that the BIOS has been properly enabled to support these usage models.																												
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.																												
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>Perform the following remote control operations across the given power states:               <table border="1"> <thead> <tr> <th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr> </thead> <tbody> <tr> <td><b>S0-&gt;</b></td><td>S0</td><td>S0</td><td>N/A</td><td>S5/DS5<sup>1</sup></td></tr> <tr> <td><b>S3-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> <tr> <td><b>S4-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> <tr> <td><b>S5-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> </tbody> </table> </li> </ol> <p>Each flow in the table above shall be executed as if they are part of an independent sub-test.</p> <ol style="list-style-type: none"> <li>Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:               <ol style="list-style-type: none"> <li>If shutdown, briefly press the Power Button on the SUT.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Record the Host OS last boot time on the SUT (to verify successful restart).</li> <li>Perform a graceful restart of the SUT via Host OS.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</li> </ol> <p>If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</p> <p>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> </li> </ol>				SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	<b>S0-&gt;</b>	S0	S0	N/A	S5/DS5 <sup>1</sup>	<b>S3-&gt;</b>	N/A	N/A	N/A	N/A	<b>S4-&gt;</b>	N/A	N/A	N/A	N/A	<b>S5-&gt;</b>	N/A	N/A	N/A	N/A
SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																									
<b>S0-&gt;</b>	S0	S0	N/A	S5/DS5 <sup>1</sup>																									
<b>S3-&gt;</b>	N/A	N/A	N/A	N/A																									
<b>S4-&gt;</b>	N/A	N/A	N/A	N/A																									
<b>S5-&gt;</b>	N/A	N/A	N/A	N/A																									



ID	AMT_022																									
<div>Procedure</div> <div>(continued)</div>	<div>4. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</div> <div>5. Perform the following remote control operations across the given power states:</div> <table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr></table> <div>Each flow in the table above shall be executed as, if they are part of an independent sub-test.</div> <div>6. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows in the chart above, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:</div> <div><div>a. If shutdown, briefly press the Power Button on the SUT.</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Record the Host OS last boot time on the SUT (to verify successful restart).</div><div>d. Perform a graceful restart of the SUT via Host OS.</div><div>e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</div></div> <div>If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</div> <div>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</div> <div><div>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</div></div> <div>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</div> <div><div>a. Bring the system to G3 and wait 10 seconds.</div><div>b. Set system power configuration to AC/DC and wait another 10 seconds.</div><div>c. Briefly press the Power Button on the SUT.</div></div> <div><sup>1</sup> In the case of Power Package 1 configuration testing, the SUT will enter the relative Deep Sx state when the BIOS has enabled Deep Sx.</div>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5	S3->	N/A	S0	S0	S5	S4->	N/A	N/A	S0	N/A	S5->	N/A	N/A	S0	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5																					
	S3->	N/A	S0	S0	S5																					
	S4->	N/A	N/A	S0	N/A																					
	S5->	N/A	N/A	S0	N/A																					
	Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.																								
	References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> .																								



## 10.6.5 Remote Power Control via Intel® AMT WLAN Network Interface for Non-Mobile Systems

ID	AMT_023			
Title	Remote Power Control via Intel® AMT WLAN Network Interface for Non-Mobile Systems			
Requirement	Mandatory			
System	Form Factor	System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS			
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"> <li>• Reset</li> <li>• Power-Up</li> <li>• Power-Down</li> <li>• Power-Cycle</li> </ul>			
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (reset, power-on/off/cycle). This test verifies that the BIOS has been properly enabled to support these usage models.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			



ID	AMT_023																									
Procedure	<div>1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</div> <div>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0).</div> <div>3. Ensure the Host OS Wake on Wireless LAN is <b>disabled</b>.</div> <div>4. Verify that Intel® AMT is available via WLAN by requesting its version.</div> <div>5. Perform the following remote control operations across the given power states:</div>																									
	<table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5/DS5<sup>1</sup></td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr></table>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>	S3->	N/A	N/A	N/A	N/A	S4->	N/A	N/A	N/A	N/A	S5->	N/A	N/A	N/A	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>																					
	S3->	N/A	N/A	N/A	N/A																					
	S4->	N/A	N/A	N/A	N/A																					
	S5->	N/A	N/A	N/A	N/A																					
	<div>Each flow in the table above shall be executed as, if they are part of an independent sub-test.</div>																									
	<div>6. Verify that the relevant power flow operation succeeded for each flow in the table above.</div> <div>Additionally, for applicable Reset, Power-Cycle, and Power-Down flows, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:</div> <div><div>a. If shutdown, briefly press the Power Button on the SUT.</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Record the Host OS last boot time on the SUT (to verify successful restart).</div><div>d. Perform a graceful restart of the SUT via Host OS.</div><div>e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</div></div>																									
	<div>If a failure occurs at any point, during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</div>																									
<div>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</div> <div><div>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</div></div>																										
<div>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</div> <div><div>a. Bring the system to G3 and wait 10 seconds.</div><div>b. Set system power configuration to AC/DC and wait another 10 seconds.</div><div>c. Briefly press the Power Button on the SUT.</div></div>																										



ID	AMT_023																									
Procedure (continued)	7. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).																									
	8. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).																									
	9. Perform the following remote control operations across the given power states:																									
	<table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr></table>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5	S3->	N/A	S0	S0	S5	S4->	N/A	N/A	S0	N/A	S5->	N/A	N/A	S0	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5																					
	S3->	N/A	S0	S0	S5																					
	S4->	N/A	N/A	S0	N/A																					
	S5->	N/A	N/A	S0	N/A																					
	Each flow in the table above shall be executed as, if they are part of an independent sub-test.																									
10. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows in the chart above, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:																										
a. If shutdown, briefly press the Power Button on the SUT.																										
b. Verify that the Host OS on the SUT is available.																										
c. Record the Host OS last boot time on the SUT (to verify successful restart).																										
d. Perform a graceful restart of the SUT via Host OS.																										
e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.																										
If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.																										
Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:																										
a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
b. Verify that the Host OS on the SUT is available.																										
c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.																										
If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.																										
a. Bring the system to G3 and wait 10 seconds.																										
b. Set system power configuration to AC/DC and wait another 10 seconds.																										
c. Briefly press the Power Button on the SUT.																										
<sup>1</sup> In the case of Power Package 1 configuration testing, the SUT will enter the relative Deep Sx state when the BIOS has enabled Deep Sx.																										
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.																									
References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> .																									



### 10.6.6 Remote Power Control in S0 Low Power Idle State via Intel® AMT LAN Network Interface

ID	AMT_024				
Title	Remote Power Control with S0 Low Power Idle state, as with Modern Standby or Microsoft* Windows InstantGo* mode, via Intel® AMT LAN Network Interface				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile		<input type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS with test operator interaction				
Description	Ensure that an Intel® AMT complaint system responds to RCO power command after the Host OS switches to S0 Low Power Idle state.				
Objective	Verify that Intel® AMT responds in S0 Low Power Idle state to Remote Power Control commands.				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. The SUT must be configured to work in Modern Standby or Microsoft* Windows InstantGo* mode. <b>NOTE:</b> In order to fully implement RCO wake, the host BIOS must implement <b>Intel® Proprietary Wake</b> . Also, <b>HID Event Filter Driver</b> must be installed. Failure to properly implement the above may result in failures for this test.				
Procedure	<ol style="list-style-type: none"><li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li><li>2. Request the test operator to manually place the SUT into S0 Low Power Idle state.</li><li>3. Verify that the SUT has moved into S0 Low Power Idle state.</li><li>4. Inform the test operator that a graceful system shutdown will be performed by Intel® PETS and to acknowledge the forthcoming shutdown prompt, which will appear on the SUT.</li><li>5. Perform a Remote <b>Graceful</b> Shutdown to S5/MeOn of the SUT via Intel® AMT and then wait <b>10 seconds</b>.</li><li>6. Perform a Remote Power-Up of the SUT via Intel® AMT.</li><li>7. Wait for the SUT to return to S0/MeOn with the Host OS running.</li><li>8. Request the test operator to manually place the SUT into S0 Low Power Idle state.</li><li>9. Verify that the SUT has moved into S0 Low Power Idle state.</li></ol>				
Pass Criteria	The test passes, if Intel® AMT is able perform Remote Power Command from S0 Low Power Idle state, and the system can be booted back to, and enter into S0 Low Power Idle state again.				
References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> . For details on Intel® Proprietary Wake, refer to HID Event Filter in <i>BIOS Enabling Guide for Windows* 10</i> .				

### 10.6.7 Remote Power Control with S0 Low Power Idle via Intel® AMT WLAN Network Interface

ID	AMT_025				
Title	Remote Power Control with S0 Low Power Idle state, as with Modern Standby or Microsoft* Windows InstantGo* mode, via Intel® AMT WLAN Network Interface				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile		<input type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS with test operator interaction				
Description	Ensure that an Intel® AMT complaint system responds to RCO power command after the Host OS switches to S0 Low Power Idle state.				
Objective	Verify that Intel® AMT responds in S0 Low Power Idle state to Remote Power Control commands.				



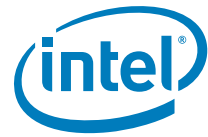


ID	AMT_025
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. The SUT must be configured to work in Modern Standby or Microsoft* Windows InstantGo* mode.
Procedure	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).</li> <li>3. Request the test operator to manually place the SUT into S0 Low Power Idle state.</li> <li>4. Verify that the SUT has moved into S0 Low Power Idle state.</li> <li>5. Inform the test operator that a graceful system shutdown will be performed by Intel® PETS and to acknowledge the forthcoming shutdown prompt which will appear on the SUT.</li> <li>6. Perform a Remote <b>Graceful</b> Shutdown to S5/MeOn of the SUT via Intel® AMT and then wait <b>10 seconds</b>.</li> <li>7. Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>8. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>9. Wait for the SUT to return to S0/MeOn with the Host OS running.</li> <li>10. Request the test operator to manually place the SUT into S0 Low Power Idle state.</li> <li>11. Verify that the SUT has moved into S0 Low Power Idle state.</li> </ol>
Pass Criteria	The test passes, if Intel® AMT is able perform Remote Power Command from S0 Low Power Idle state, and the system can be booted back to, and enter into S0 Low Power Idle state again.
References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.6.8 Remote Power Control via Intel® AMT WLAN Network Interface for Mobile Systems supporting Wake On Wireless LAN

ID	AMT_026			
Title	Remote Power Control via Intel® AMT WLAN Network Interface for Mobile Systems supporting Wake on Wireless LAN			
Requirement	Mandatory - exempt for systems that do not support Wake on Wireless LAN			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS			
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"> <li>• Reset</li> <li>• Power-Up</li> <li>• Power-Down</li> <li>• Power-Cycle</li> </ul>			
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (reset, power-on/off/cycle). This test verifies that the BIOS has been properly enabled to support these usage models.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.  <b>NOTE:</b> In order to fully implement Wake on Wireless LAN (WoWLAN) in Sx states, the host BIOS must set HOST_WLAN_PP_EN. For more further details, refer to the PCH <i>External Design Specification (EDS)</i> and the PCH <i>Platform Design Guide (PDG)</i> . Failure to properly set the HOST_WLAN_PP_EN bit may result in failures for this test.			



ID	AMT_026															
Procedure	<div><div><div>1. Ensure the system power configuration is set to AC/DC.</div><div>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</div><div>3. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0).</div><div>4. Ensure the Host OS Wake on Wireless LAN is <b>enabled</b>.</div><div>5. Verify that Intel® AMT is available via WLAN by requesting its version.</div><div>6. Perform the following remote control operations across the given power states:</div></div><table><thead><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr></thead><tbody><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5/DS5<sup>1</sup></td></tr><tr><td>S3 (WoWLAN) -&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5/DS5<sup>1</sup></td></tr></tbody></table><div><div>Each flow in the table above shall be executed as if they are part of an independent sub-test.</div><div>7. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:</div><div><div>a. If shutdown, briefly press the Power Button on the SUT.</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Record the Host OS last boot time on the SUT (to verify successful restart).</div><div>d. Perform a graceful restart of the SUT via Host OS.</div><div>e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</div></div><div><div>If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</div><div>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</div><div><div>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</div></div><div><div>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</div><div><div>a. Bring the system to G3 and wait 10 seconds.</div><div>b. Set system power configuration to AC/DC and wait another 10 seconds.</div><div>c. Briefly press the Power Button on the SUT.</div></div></div></div></div></div>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>	S3 (WoWLAN) ->	N/A	S0	S0	S5/DS5 <sup>1</sup>
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down											
	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>											
	S3 (WoWLAN) ->	N/A	S0	S0	S5/DS5 <sup>1</sup>											



ID	AMT_026																									
Procedure (continued)	8. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).																									
	9. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).																									
	10. Perform the following remote control operations across the given power states:																									
	<table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr></table>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5	S3->	N/A	S0	S0	S5	S4->	N/A	S0	S0	S5	S5->	N/A	S0	S0	S5
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5																					
	S3->	N/A	S0	S0	S5																					
	S4->	N/A	S0	S0	S5																					
	S5->	N/A	S0	S0	S5																					
	Each flow in the table above shall be executed as if they are part of an independent sub-test.																									
11. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows in the chart above, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:																										
a. If shutdown, briefly press the Power Button on the SUT.																										
b. Verify that the Host OS on the SUT is available.																										
c. Record the Host OS last boot time on the SUT (to verify successful restart).																										
d. Perform a graceful restart of the SUT via Host OS.																										
e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.																										
If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.																										
Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:																										
a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
b. Verify that the Host OS on the SUT is available.																										
c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.																										
If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.																										
a. Bring the system to G3 and wait 10 seconds.																										
b. Set system power configuration to AC/DC and wait another 10 seconds.																										
c. Briefly press the Power Button on the SUT.																										
<sup>1</sup> In the case of Power Package 1 configuration or DC-only power configuration testing, the SUT will enter the relative Deep Sx state when the BIOS has enabled Deep Sx.																										
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.																									
References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> as well as the <i>Intel® AMT and Wake On Wireless LAN Coexistence</i> feature overview.																									



## 10.6.9 Remote Power Control via Intel® AMT WLAN Network Interface for Non-Mobile Systems supporting Wake On Wireless LAN

ID	AMT_027				
Title	Remote Power Control via Intel® AMT WLAN Network Interface for Non-Mobile Systems supporting Wake on Wireless LAN				
Requirement	Mandatory - exempt for systems that do not support Wake on Wireless LAN				
System	Form Factor	System Power Model	Intel® AMT Network Interface		LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS				
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"> <li>• Reset</li> <li>• Power-Up</li> <li>• Power-Down</li> <li>• Power-Cycle</li> </ul>				
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (reset, power-on/off/cycle). This test verifies that the BIOS has been properly enabled to support these usage models.				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.  <b>NOTE:</b> In order to fully implement Wake on Wireless LAN (WoWLAN) in Sx states, the host BIOS must set HOST_WLAN_PP_EN. For more further details, refer to the PCH <i>External Design Specification (EDS)</i> and the PCH <i>Platform Design Guide (PDG)</i> . Failure to properly set the HOST_WLAN_PP_EN bit may result in failures for this test.				



ID	AMT_027																									
Procedure	<div>1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</div> <div>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0).</div> <div>3. Ensure the Host OS Wake on Wireless LAN is <b>enabled</b>.</div> <div>4. Verify that Intel® AMT is available via WLAN by requesting its version.</div> <div>5. Perform the following remote control operations across the given power states:</div> <table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5/DS5<sup>1</sup></td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5/DS5<sup>1</sup></td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr></table> <div>Each flow in the table above shall be executed as if they are part of an independent sub-test.</div> <div>6. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:</div> <div><div>a. If shutdown, briefly press the Power Button on the SUT.</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Record the Host OS last boot time on the SUT (to verify successful restart).</div><div>d. Perform a graceful restart of the SUT via Host OS.</div><div>e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</div></div> <div>If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</div> <div>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</div> <div><div>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</div></div> <div>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</div> <div><div>a. Bring the system to G3 and wait 10 seconds.</div><div>b. Set system power configuration to AC/DC and wait another 10 seconds.</div><div>c. Briefly press the Power Button on the SUT.</div></div>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>	S3->	N/A	S0	S0	S5/DS5 <sup>1</sup>	S4->	N/A	N/A	N/A	N/A	S5->	N/A	N/A	N/A	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5/DS5 <sup>1</sup>																					
	S3->	N/A	S0	S0	S5/DS5 <sup>1</sup>																					
	S4->	N/A	N/A	N/A	N/A																					
	S5->	N/A	N/A	N/A	N/A																					



ID	AMT_027																									
<div>Procedure (continued)</div>	<div>7. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</div> <div>8. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).</div> <div>9. Perform the following remote control operations across the given power states:</div> <table><tr><th>SUT Initial State</th><th>Reset</th><th>Power-Cycle</th><th>Power-Up</th><th>Power-Down</th></tr><tr><td>S0-&gt;</td><td>S0</td><td>S0</td><td>N/A</td><td>S5</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>S0</td><td>S0</td><td>S5</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>S0</td><td>N/A</td></tr></table> <div>Each flow in the table above shall be executed as if they are part of an independent sub-test.</div> <div>10. Verify that the relevant power flow operation succeeded for each flow in the table above. Additionally, for applicable Reset, Power-Cycle, and Power-Down flows in the chart above, perform the following additional sub-steps for two (2) cycles each after the remote control operation has completed:</div> <div><div>a. If shutdown, briefly press the Power Button on the SUT.</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Record the Host OS last boot time on the SUT (to verify successful restart).</div><div>d. Perform a graceful restart of the SUT via Host OS.</div><div>e. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>f. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</div></div> <div>If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</div> <div>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</div> <div><div>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div><div>b. Verify that the Host OS on the SUT is available.</div><div>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</div></div> <div>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</div> <div><div>a. Bring the system to G3 and wait 10 seconds.</div><div>b. Set system power configuration to AC/DC and wait another 10 seconds.</div><div>c. Briefly press the Power Button on the SUT.</div></div> <div><sup>1</sup> In the case of Power Package 1 configuration testing, the SUT will enter the relative Deep Sx state when the BIOS has enabled Deep Sx.</div>	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down	S0->	S0	S0	N/A	S5	S3->	N/A	S0	S0	S5	S4->	N/A	N/A	S0	N/A	S5->	N/A	N/A	S0	N/A
	SUT Initial State	Reset	Power-Cycle	Power-Up	Power-Down																					
	S0->	S0	S0	N/A	S5																					
	S3->	N/A	S0	S0	S5																					
	S4->	N/A	N/A	S0	N/A																					
	S5->	N/A	N/A	S0	N/A																					
	Pass Criteria	The test passes if Intel® PETS confirms each test step succeeded.																								
	References	For details on Remote Control Operations, refer to the <i>Intel® ME BIOS Specification</i> as well as the <i>Intel® AMT and Wake On Wireless LAN Coexistence</i> feature overview.																								



## 10.6.10 Remote Power Control with Host OS interaction via Intel® AMT LAN Network Interface

ID	AMT_028																												
Title	Remote Power Control with Host OS interaction via Intel® AMT LAN Network Interface																												
Requirement	Mandatory																												
System	Form Factor	System Power Model	Intel® AMT Network Interface																										
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN																									
Method	Automated by Intel® PETS																												
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"> <li>• Sleep</li> <li>• Hibernate</li> <li>• Graceful Power-Down</li> <li>• Graceful Power-Cycle</li> </ul>																												
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (Sleep, Hibernate, and graceful power-on/off/cycle). This test verifies that the system has been properly enabled to support these usage models.																												
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. The Local Manageability Service (LMS), included with the Intel® ME software package, must be installed and running on the SUT.																												
Procedure	<ol style="list-style-type: none"> <li>1. Ensure the system power configuration is set to AC/DC or AC-only.</li> <li>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>3. Perform the following remote control operations across the given power states:           <table border="1"> <thead> <tr> <th>SUT Initial State</th><th>Sleep</th><th>Hibernate</th><th>Graceful Power- Down</th><th>Graceful Power-Reset</th></tr> </thead> <tbody> <tr> <td><b>S0-&gt;</b></td><td>S3<sup>1</sup></td><td>S4/DS4<sup>1</sup></td><td>S5/DS5<sup>1</sup></td><td>S0</td></tr> <tr> <td><b>S3-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> <tr> <td><b>S4-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> <tr> <td><b>S5-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> </tbody> </table> </li> </ol> <p>Each flow in the table above shall be executed as if they are part of an independent sub-test. In each independent sub-test, before issuing the remote control operation, query Intel® AMT on the SUT for up to <b>4 minutes</b> at <b>30 second</b> intervals to ensure that the intended graceful remote power state is available. In the case of Modern Standby or Microsoft® Windows InstantGo* mode, the Sleep test flows shall be skipped.</p> <ol style="list-style-type: none"> <li>4. Verify that the relevant power flow operation succeeded for each flow in the table above. If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</li> </ol> <p>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>b. Verify that the Host OS on the SUT is available.</li> <li>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</p> <ol style="list-style-type: none"> <li>a. Bring the system to G3 and wait 10 seconds.</li> <li>b. Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>c. Briefly press the Power Button on the SUT.</li> </ol>				SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset	<b>S0-&gt;</b>	S3 <sup>1</sup>	S4/DS4 <sup>1</sup>	S5/DS5 <sup>1</sup>	S0	<b>S3-&gt;</b>	N/A	N/A	N/A	N/A	<b>S4-&gt;</b>	N/A	N/A	N/A	N/A	<b>S5-&gt;</b>	N/A	N/A	N/A	N/A
SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset																									
<b>S0-&gt;</b>	S3 <sup>1</sup>	S4/DS4 <sup>1</sup>	S5/DS5 <sup>1</sup>	S0																									
<b>S3-&gt;</b>	N/A	N/A	N/A	N/A																									
<b>S4-&gt;</b>	N/A	N/A	N/A	N/A																									
<b>S5-&gt;</b>	N/A	N/A	N/A	N/A																									





ID	AMT_028																									
Procedure (continued)	5. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).																									
	6. Perform the following remote control operations across the given power states:																									
	<table><tr><th>SUT Initial State</th><th>Sleep</th><th>Hibernate</th><th>Graceful Power- Down</th><th>Graceful Power-Reset</th></tr><tr><td>S0-&gt;</td><td>S3</td><td>S4</td><td>S5</td><td>S0</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr></table>	SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset	S0->	S3	S4	S5	S0	S3->	N/A	N/A	N/A	N/A	S4->	N/A	N/A	N/A	N/A	S5->	N/A	N/A	N/A	N/A
	SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset																					
	S0->	S3	S4	S5	S0																					
	S3->	N/A	N/A	N/A	N/A																					
	S4->	N/A	N/A	N/A	N/A																					
	S5->	N/A	N/A	N/A	N/A																					
	Each flow in the table above shall be executed as if they are part of an independent sub-test. In each independent sub-test, before issuing the remote control operation, query Intel® AMT on the SUT for up to <b>4 minutes</b> at <b>30 second</b> intervals to ensure that the intended graceful remote power state is available. In the case of Modern Standby or Microsoft* Windows InstantGo* mode, the Sleep test flows shall be skipped.																									
	7. Verify that the relevant power flow operation succeeded for each flow in the table above																									
If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.																										
Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:																										
a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																										
b. Verify that the Host OS on the SUT is available.																										
c. Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.																										
If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.																										
a. Bring the system to G3 and wait 10 seconds.																										
b. Set system power configuration to AC/DC and wait another 10 seconds.																										
c. Briefly press the Power Button on the SUT.																										
<sup>1</sup> In the case of Power Package 1 configuration testing, the SUT will enter the relative Deep Sx state when the BIOS has enabled Deep Sx.																										
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.																									
References	For details on Remote Control Operations, refer to the Intel® ME BIOS Specification.																									



## 10.6.11 Remote Power Control with Host OS interaction via Intel® AMT WLAN Network Interface

ID	AMT_029																												
Title	Remote Power Control with Host OS interaction via Intel® AMT WLAN Network Interface																												
Requirement	Mandatory																												
System	Form Factor	System Power Model	Intel® AMT Network Interface																										
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used																									
Method	Automated by Intel® PETS																												
Description	An Intel® AMT compliant system shall support the following remote control operations: <ul style="list-style-type: none"> <li>• Sleep</li> <li>• Hibernate</li> <li>• Graceful Power-Down</li> <li>• Graceful Power-Cycle</li> </ul>																												
Objective	Verify that the remote control management features of the Intel® AMT platform meet the requirements.  Intel® AMT enables remote management of the platform, including the capability to control platform power states (Sleep, Hibernate, and graceful power-on/off/cycle). This test verifies that the system has been properly enabled to support these usage models.																												
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. The Local Manageability Service (LMS), included with the Intel® ME software package, must be installed and running on the SUT.																												
Procedure	<ol style="list-style-type: none"> <li>1. Ensure the system power configuration is set to AC/DC or AC-only.</li> <li>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>3. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0).</li> <li>4. Ensure the Host OS Wake on Wireless LAN is <b>disabled</b>.</li> <li>5. Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>6. Perform the following remote control operations across the given power states:               <table border="1"> <thead> <tr> <th>SUT Initial State</th><th>Sleep</th><th>Hibernate</th><th>Graceful Power- Down</th><th>Graceful Power-Reset</th></tr> </thead> <tbody> <tr> <td><b>S0-&gt;</b></td><td>S3<sup>1</sup></td><td>S4/DS4<sup>1</sup></td><td>S5/DS5<sup>1</sup></td><td>S0</td></tr> <tr> <td><b>S3-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> <tr> <td><b>S4-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> <tr> <td><b>S5-&gt;</b></td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> </tbody> </table> </li> </ol> <p>Each flow in the table above shall be executed as if they are part of an independent sub-test. In each independent sub-test, before issuing the remote control operation, query Intel® AMT on the SUT for up to <b>4 minutes</b> at <b>30 second</b> intervals to ensure that the intended graceful remote power state is available. In the case of Modern Standby or Microsoft® Windows InstantGo* mode, the Sleep test flows shall be skipped.</p> <ol style="list-style-type: none"> <li>7. Verify that the relevant power flow operation succeeded for each flow in the table above. If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.</li> </ol> <p>Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>b. Verify that the Host OS on the SUT is available.</li> <li>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time:</p> <ol style="list-style-type: none"> <li>a. Bring the system to G3 and wait 10 seconds.</li> <li>b. Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>c. Briefly press the Power Button on the SUT.</li> </ol>				SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset	<b>S0-&gt;</b>	S3 <sup>1</sup>	S4/DS4 <sup>1</sup>	S5/DS5 <sup>1</sup>	S0	<b>S3-&gt;</b>	N/A	N/A	N/A	N/A	<b>S4-&gt;</b>	N/A	N/A	N/A	N/A	<b>S5-&gt;</b>	N/A	N/A	N/A	N/A
SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset																									
<b>S0-&gt;</b>	S3 <sup>1</sup>	S4/DS4 <sup>1</sup>	S5/DS5 <sup>1</sup>	S0																									
<b>S3-&gt;</b>	N/A	N/A	N/A	N/A																									
<b>S4-&gt;</b>	N/A	N/A	N/A	N/A																									
<b>S5-&gt;</b>	N/A	N/A	N/A	N/A																									



ID	AMT_029																									
Procedure (continued)	8. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).																									
	9. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).																									
	10. Perform the following remote control operations across the given power states:																									
	<table><tr><th>SUT Initial State</th><th>Sleep</th><th>Hibernate</th><th>Graceful Power- Down</th><th>Graceful Power-Reset</th></tr><tr><td>S0-&gt;</td><td>S3</td><td>S4</td><td>S5</td><td>S0</td></tr><tr><td>S3-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S4-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>S5-&gt;</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr></table>	SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset	S0->	S3	S4	S5	S0	S3->	N/A	N/A	N/A	N/A	S4->	N/A	N/A	N/A	N/A	S5->	N/A	N/A	N/A	N/A
	SUT Initial State	Sleep	Hibernate	Graceful Power- Down	Graceful Power-Reset																					
S0->	S3	S4	S5	S0																						
S3->	N/A	N/A	N/A	N/A																						
S4->	N/A	N/A	N/A	N/A																						
S5->	N/A	N/A	N/A	N/A																						
Each flow in the table above shall be executed as if they are part of an independent sub-test. In each independent sub-test, before issuing the remote control operation, query Intel® AMT on the SUT for up to <b>4 minutes at 30 second</b> intervals to ensure that the intended graceful remote power state is available. In the case of Modern Standby or Microsoft* Windows InstantGo* mode, the Sleep test flows shall be skipped.																										
11. Verify that the relevant power flow operation succeeded for each flow in the table above.																										
	If a failure occurs at any point during the flow above (including during any additional applicable sub-steps), the remainder of the steps related to the sub-test, may be skipped.																									
	Regardless of the prior sub-test overall results, before beginning the next sub-test, attempt to bring the SUT to a base state via the following:																									
	a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).																									
	b. Verify that the Host OS on the SUT is available.																									
	c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.																									
	If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.																									
	a. Bring the system to G3 and wait 10 seconds.																									
	b. Set system power configuration to AC/DC and wait another 10 seconds.																									
	c. Briefly press the Power Button on the SUT.																									
	<sup>1</sup> In the case of Power Package 1 configuration testing, the SUT will enter the relative Deep Sx state, when the BIOS has enabled Deep Sx.																									
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.																									
References	For details on Remote Control Operations, refer to the Intel® ME BIOS Specification.																									

## 10.7 Serial-Over-LAN and Storage Redirection

The section serves as a checklist for the environment setup and covers integration testing of the Serial-Over-LAN and Storage Redirection features in Intel® AMT.

### 10.7.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows\* supported by Intel® PETS, and the SUT should have a version of Microsoft\* Windows\* supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables.

#### Tools for testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.



In order for Intel® PETS to work properly, ensure the following:

- The SUT has a valid System UUID. This can be checked by confirming a non-zero value is reported by the Intel® MEInfo tool.
- The firmware image is configured to **not** require user consent on redirection. This can be done by checking the following value of the SPI image via the Intel® FIT tool in the 'Intel(R) AMT' tab: 'Redirection Configuration' | 'Redirection Privacy / Security Level' set to "Default".

Where applicable, the wireless LAN interface on Intel® AMT must be on a different network/subnet than the wired LAN interface. For details on how to enter the network interface details into Intel® PETS, consult the Intel® PETS User Guide.

If the firmware image or the SUT configuration does not support some features, Intel® PETS will show those features as failing when tested. Intel® PETS cannot determine in all cases, which features have been deactivated and should thus be skipped during testing.



## 10.7.2 SOL Redirection and BIOS Setup Boot Option over Intel® AMT LAN

ID	AMT_030			
Title	Serial-Over-LAN (SOL) Redirection and BIOS Setup Boot Option over Intel® AMT LAN Network Interface			
Requirement	Mandatory - exempt for systems that do not support the BIOS Setup boot option			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement BIOS boot screen redirection according to the boot options received from the GetBootOptions command.			
Objective	<p>Verify that the BIOS detects, and executes, a request (by means of boot options) to redirect text to the management console via SOL.</p> <p>Intel® AMT enables remote management of the platform, including providing capabilities to read the boot options sent from the management console. These boot options can include commands to send display text from the Intel® AMT platform to the remote console by means of Serial-Over-LAN functionality. Testing described in this section will verify that BIOS has been properly enabled to support these usage models.</p>			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL is enabled in the Intel® MEBX.</p> <p>The default number of rows shown in the Putty terminal window may differ from the number of rows displayed by the BIOS. When this occurs, the Putty terminal display will incur line wrapping problems. To avoid this problem, change the settings of the Putty application to align with the BIOS via the following steps:</p> <ol style="list-style-type: none"> <li>Open the ".\Intel(R) Platform Enablement Test Suite\Plugins\Me\Redirection\bin\" directory.</li> <li>Start putty.exe, and in the Category section:             <ol style="list-style-type: none"> <li>Select Window, and change the Rows value to the required number of rows.</li> <li>Select Session, then select <i>Default Settings</i>, and finally click the Save button.</li> </ol> </li> <li>Close the Putty Configuration window.</li> <li>To confirm, start putty.exe again, and make sure Row number is set to the new value.</li> </ol>			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Verify the SUT supports booting into BIOS by querying the Intel® AMT and checking the boot capabilities.             <ol style="list-style-type: none"> <li>If supported, use Intel® AMT to set the BIOS Setup boot option on the SUT for the next boot.</li> <li>If not supported, end the test and request the test operator to confirm the BIOS support of 'BIOS Setup' OEMCapabilities1 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Use Intel® AMT to set the SUT boot options to use SOL Redirection on the next boot.</li> <li>Close any open SOL Redirection session with the SUT via Intel® AMT.</li> </ol> <p>The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot into the BIOS setup menu.</li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to:             <ol style="list-style-type: none"> <li>Confirm that the BIOS setup screen of the SUT is displayed in the Putty window.</li> <li>Confirm that remote keyboard is working properly.</li> </ol> </li> </ol>			



ID	AMT_030
<b>Procedure</b> (continued)	13. Close any open SOL Redirection session with the SUT via Intel® AMT. 14. Close any Putty terminal window which may still be open. 15. Perform a Remote Reset of the SUT via Intel® AMT.
<b>Pass Criteria</b>	The test passes, if Intel® PETS indicates all steps have passed successfully.
<b>References</b>	For details on SOL and ASF Boot Options, refer to the <i>Intel® ME BIOS Specification</i> .



### 10.7.3 SOL Redirection and BIOS Setup Boot Option over Intel® AMT WLAN Network Interface

ID	AMT_031			
Title	Serial-Over-LAN (SOL) Redirection and BIOS Setup Boot Option over Intel® AMT WLAN Network Interface			
Requirement	Mandatory - exempt for systems that do not support the BIOS Setup boot option			
System	Form Factor	System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement BIOS boot screen redirection according to the boot options received from the GetBootOptions command.			
Objective	<p>Verify that the BIOS detects, and executes, a request (by means of boot options) to redirect text to the management console (SOL). Before running this test, ensure that SOL is enabled in the Intel® MEBX.</p> <p>Intel® AMT enables remote management of the platform, including providing capabilities to read the boot options sent from the management console. These boot options can include commands to send display text from the Intel® AMT platform to the remote console by means of Serial-Over-LAN functionality. Testing described in this section will verify that BIOS has been properly enabled to support these usage models.</p>			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.</p> <p>The default number of rows shown in the Putty terminal window may differ from the number of rows displayed by the BIOS. When this occurs, the Putty terminal display will incur line wrapping problems. To avoid this problem, change the settings of the Putty application to align with the BIOS via the following steps:</p> <ol style="list-style-type: none"> <li>Open the ".\Intel(R) Platform Enablement Test Suite\Plugins\Me\Redirection\bin\" directory.</li> <li>Start putty.exe, and in the Category section:             <ol style="list-style-type: none"> <li>Select Window, and change the Rows value to the required number of rows.</li> <li>Select Session, then select <i>Default Settings</i>, and finally click the Save button.</li> </ol> </li> <li>Close the Putty Configuration window.</li> <li>To confirm, start putty.exe again, and make sure Row number is set to the new value.</li> </ol>			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Verify the SUT supports booting into BIOS by querying the Intel® AMT and checking the boot capabilities.             <ol style="list-style-type: none"> <li>If supported, use Intel® AMT to set the BIOS Setup boot option on the SUT for the next boot.</li> <li>If not supported, end the test and request the test operator to confirm the BIOS support of 'BIOS Setup' OEMCapabilities1 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Use Intel® AMT to set the SUT boot options to use SOL Redirection on the next boot.</li> <li>Close any open SOL Redirection session with the SUT via Intel® AMT.</li> </ol> <p>The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot into the BIOS setup menu.</li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to:             <ol style="list-style-type: none"> <li>Confirm that the BIOS setup screen of the SUT is displayed in the Putty window.</li> <li>Confirm that remote keyboard is working properly.</li> </ol> </li> </ol>			



ID	AMT_031
<b>Procedure</b> (continued)	15. Close any open SOL Redirection session with the SUT via Intel® AMT. 16. Close any Putty terminal window which may still be open. 17. Perform a Remote Reset of the SUT via Intel® AMT.
<b>Pass Criteria</b>	The test passes if Intel® PETS indicates all steps have passed successfully.
<b>References</b>	For details on SOL and ASF Boot Options, refer to the <i>Intel® ME BIOS Specification</i> .





## 10.7.4 SOL and Storage Redirection over Intel® AMT LAN Network Interface

<b>ID</b>	<b>AMT_032</b>			
<b>Title</b>	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT LAN Network Interface			
<b>Requirement</b>	Mandatory			
<b>System</b>	<b>Form Factor</b>	<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	<b>LAN Type</b>
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	An Intel® AMT compliant system shall implement SOL and Storage Redirection according to the boot options received from the GetBootOptions command.			
<b>Objective</b>	<p>Verify that the BIOS detects, and executes, a request (by means of boot options) to redirect text to the management console via SOL and perform Storage Redirection to an ISO OS image.</p> <p>Intel® AMT enables remote management of the platform, including providing capabilities to read the boot options sent from the management console. These boot options can include commands to send display text from the Intel® AMT platform to the remote console by means of SOL functionality and to redirect the default platform boot device via Storage Redirection. Testing described in this section will verify that BIOS has been properly enabled to support these usage models.</p>			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL and Storage Redirection are enabled in the Intel® MEBX.			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Use Intel® AMT to set the SUT boot options to use SOL and Storage Redirection Boot on the next boot.</li> <li>Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT. The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</li> <li>Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to a redirected ISO OS image via Serial-Over-LAN.</li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>Open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to confirm that SUT boots from redirected ISO OS image.</li> </ol>			



ID	AMT_032
Procedure (continued)	<p>13. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT.</p> <p>14. Close any Putty terminal window which may still be open.</p> <p>15. Request the test operator to:</p> <ul style="list-style-type: none"><li>a. Gracefully reboot the SUT,</li><li>b. Enter the Intel® MEBX on the SUT and <b>disable</b> both SOL and Storage Redirection, and</li><li>c. Boot the SUT to Host OS.</li></ul> <p>16. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>17. Attempt to open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console. Failure to open the session by error indicating the SOL interface is disabled indicates success for the test step, otherwise the test step fails.</p> <p>18. Attempt to open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console. Failure to open the session by error indicating the Storage Redirection interface is disabled indicates success for the test step, otherwise the test step fails.</p> <p>19. Request the test operator to:</p> <ul style="list-style-type: none"><li>a. Boot the SUT,</li><li>b. Enter the Intel® MEBX on the SUT and <b>enable</b> both SOL and Storage Redirection, and</li><li>c. Boot the SUT to Host OS.</li></ul>
Pass Criteria	The test passes, if Intel® PETS indicates all steps have passed successfully.
References	For details on SOL and Storage Redirection, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.7.5 SOL and Storage Redirection Over Intel® AMT WLAN Network Interface

ID	AMT_033			
Title	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT WLAN Network Interface			
Requirement	Mandatory			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement SOL and Storage Redirection according to the boot options received from the GetBootOptions command.			
Objective	<p>Verify that the BIOS detects, and executes, a request (by means of boot options) to redirect text to the management console via SOL and perform Storage Redirection to an ISO OS image.</p> <p>Intel® AMT enables remote management of the platform, providing capabilities to read the boot options sent from the management console. These boot options can include commands to send display text from the Intel® AMT platform to the remote console by means of SOL functionality and to redirect the default platform boot device via Storage Redirection. Testing described in this section will verify that BIOS has been properly enabled to support these usage models.</p>			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL and Storage Redirection are enabled in the Intel® MEBX.			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Use Intel® AMT to set the SUT boot options to use SOL and Storage Redirection Boot on the next boot.</li> </ol>			
	<ol style="list-style-type: none"> <li>Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT. The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</li> <li>Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to a redirected ISO OS image via Serial-Over-LAN.</li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>Open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to confirm that SUT boots from redirected ISO OS image.</li> </ol>			



ID	AMT_033
Procedure (continued)	<p>15. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT.</p> <p>16. Close any Putty terminal window, which may still be open.</p> <p>17. Request the test operator to:</p> <ul style="list-style-type: none"><li>a. Gracefully reboot the SUT.</li><li>b. Enter the Intel® MEBX on the SUT and <b>disable</b> both SOL and Storage Redirection, and</li><li>c. Boot the SUT to Host OS.</li></ul> <p>18. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>19. Verify that Intel® AMT is available via WLAN by requesting its version.</p> <p>20. Attempt to open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console. Failure to open the session by error indicating the SOL interface is disabled indicates success for the test step, otherwise the test step fails.</p> <p>21. Attempt to open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console. Failure to open the session by error indicating the Storage Redirection interface is disabled indicates success for the test step, otherwise the test step fails.</p> <p>22. Request the test operator to:</p> <ul style="list-style-type: none"><li>a. Boot the SUT,</li><li>b. Enter the Intel® MEBX on the SUT and <b>enable</b> both SOL and Storage Redirection, and</li><li>c. Boot the SUT to Host OS.</li></ul>
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.
References	For details on SOL and Storage Redirection, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.7.6 SOL and Storage Redirection over Intel® AMT LAN Network Interface with User Consent Enabled

ID	AMT_034			
Title	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT LAN Network Interface with User Consent Enabled			
Requirement	Mandatory			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>NOTE:</b> Applies to systems with <b>discrete</b> graphics and also those with <b>integrated</b> graphics.				
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement SOL and Storage Redirection according to the boot options received from the GetBootOptions command. When user consent is enabled, a redirection session will be allowed only after the user consent code is accepted by Intel® AMT.			
Objective	<p>Verify that the BIOS detects, and executes, a request (by means of boot options) to redirect text to the management console via SOL and perform Storage Redirection to an ISO OS image.</p> <p>Intel® AMT enables remote management of the platform, including providing capabilities to read the boot options sent from the management console. These boot options can include commands to send display text from the Intel® AMT platform to the remote console by means of SOL functionality and to redirect the default platform boot device via Storage Redirection. Testing described in this section will verify that BIOS has been properly enabled to support these usage models.</p>			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL and Storage Redirection are enabled in the Intel® MEBX.			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> on the SUT.</li> <li>Initiate a new Intel® AMT user consent session with the SUT.</li> <li>In the case of integrated graphics:             <ol style="list-style-type: none"> <li>A user consent code will be displayed on the SUT screen.</li> <li>Verify via Intel® AMT that the user consent opt-in state on the SUT is "Displayed".</li> <li>Request the test operator to enter the user consent code to the text box on the management console.</li> <li>Forward the user consent code to the SUT via Intel® AMT.</li> </ol> </li> <li>In the case of discrete graphics:             <ol style="list-style-type: none"> <li>Perform a graceful restart of the SUT via Host OS. The SUT will boot and halt in Intel® MEBX to display the user consent code.</li> <li>Verify via Intel® AMT that the user consent opt-in state on the SUT is "Displayed".</li> <li>Request the test operator to enter the user consent code to the text box on the management console.</li> <li>Forward the user consent code to the SUT via Intel® AMT.</li> <li>The SUT will continue to boot to the Host OS. <b>Note:</b> It may be necessary to press ESC on the SUT to continue the boot process.</li> <li>Wait for the SUT to return to S0/MeOn with the Host OS running.</li> </ol> </li> <li>Use Intel® AMT to set the SUT boot options to use SOL and Storage Redirection Boot on the next boot.</li> </ol>			



ID	AMT_034
Procedure (continued)	<p>8. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT. The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>9. Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to a redirected ISO OS image via Serial-Over-LAN.</p> <p>10. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>11. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</p> <p>12. Open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console.</p> <p>13. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>14. Request the test operator to confirm that SUT boots from redirected ISO OS image.</p> <p>15. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT.</p> <p>16. Close any Putty terminal window, which may still be open.</p> <p>17. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</p> <p>18. Perform a Remote Reset of the SUT via Intel® AMT.</p>
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.
References	For details on SOL and Storage Redirection, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.7.7 SOL and Storage Redirection over Intel® AMT WLAN Network Interface with User Consent Enabled

ID	AMT_035			
Title	Serial-Over-LAN (SOL) and Storage Redirection over Intel® AMT WLAN Network Interface with User Consent Enabled			
Requirement	Mandatory			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Note:</b> Applies to systems with <b>discrete</b> graphics and also those with <b>integrated</b> graphics.				
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement SOL and Storage Redirection according to the boot options received from the GetBootOptions command. When user consent is enabled, a redirection session will be allowed only after the user consent code is accepted by Intel® AMT.			
Objective	<p>Verify that the BIOS detects, and executes, a request (by means of boot options) to redirect text to the management console via SOL and perform Storage Redirection to an ISO OS image.</p> <p>Intel® AMT enables remote management of the platform, including providing capabilities to read the boot options sent from the management console. These boot options can include commands to send display text from the Intel® AMT platform to the remote console by means of SOL functionality and to redirect the default platform boot device via Storage Redirection. Testing described in this section will verify that BIOS has been properly enabled to support these usage models.</p>			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL and Storage Redirection are enabled in the Intel® MEBX.			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> on the SUT.</li> <li>Initiate a new Intel® AMT user consent session with the SUT.</li> <li>In the case of integrated graphics:               <ol style="list-style-type: none"> <li>A user consent code will be displayed on the SUT screen.</li> <li>Verify via Intel® AMT that the user consent opt-in state on the SUT is "Displayed".</li> <li>Request the test operator to enter the user consent code to the text box on the management console.</li> <li>Forward the user consent code to the SUT via Intel® AMT.</li> </ol> </li> <li>In the case of discrete graphics:               <ol style="list-style-type: none"> <li>Perform a graceful restart of the SUT via Host OS. The SUT will boot and halt in Intel® MEBX to display the user consent code.</li> <li>Verify via Intel® AMT that the user consent opt-in state on the SUT is "Displayed".</li> <li>Request the test operator to enter the user consent code to the text box on the management console.</li> <li>Forward the user consent code to the SUT via Intel® AMT.</li> <li>The SUT will continue to boot to the Host OS.</li> </ol> </li> </ol> <p><b>NOTE:</b> It may be necessary to press ESC on the SUT to continue the boot process.</p> <ol style="list-style-type: none"> <li>Wait for the SUT to return to S0/MeOn with the Host OS running.</li> </ol> <ol style="list-style-type: none"> <li>Use Intel® AMT to set the SUT boot options to use SOL and Storage Redirection Boot on the next boot.</li> </ol>			



ID	AMT_035
Procedure (continued)	<p>9. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT. The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>10. Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to a redirected ISO OS image via Serial-Over-LAN.</p> <p>11. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>12. Verify that Intel® AMT is available via WLAN by requesting its version.</p> <p>13. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</p> <p>14. Open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console.</p> <p>15. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>16. Request the test operator to confirm that SUT boots from redirected ISO OS image.</p> <p>17. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT.</p> <p>18. Close any Putty terminal window which may still be open.</p> <p>19. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</p> <p>20. Perform a Remote Reset of the SUT via Intel® AMT.</p>
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.
References	For details on SOL and Storage Redirection, refer to the <i>Intel® ME BIOS Specification</i> .





## 10.7.8 SOL and Storage Redirection with Secure Boot

ID	AMT_036			
Title	Serial-Over-LAN (SOL) and Storage Redirection with Secure Boot			
Requirement	Mandatory - exempt for systems that do not support the Secure Boot BIOS boot option			
System	Form Factor	System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system supporting Secure Boot shall support Storage Redirection operations with non-secure images. It shall also support a boot option to enforce the secure boot even during the Storage Redirection boot flow.			
Objective	Verify that the BIOS by default disables the secure boot feature, when performing a Storage Redirection boot. Additionally, verify that when the flag to enforce secure boot during Storage Redirection is set, BIOS does not disable the secure boot feature when performing the Storage Redirection boot of an ISO OS image. Furthermore, it fail to boot with an insecure ISO OS image, but succeed to boot with a secured ISO OS image.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL and Storage Redirection are enabled in the Intel® MEBX. The SUT must have a UEFI BIOS and CSM disabled to allow Secure Boot testing. A secured ISO OS image must be created and placed on the management console hard drive; Intel® PETS does not include such an image.			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Gracefully reboot the SUT,</li> <li>Set the BIOS to enable Secure Boot, and</li> <li>Boot the SUT to Host OS.</li> </ol> </li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries.</li> </ol>			
	<p>The steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Use Intel® AMT to set the SUT boot options to use SOL and Storage Redirection Boot on the next boot.</li> <li>Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot to a redirected <b>un-secured</b> ISO OS image via Serial-Over-LAN.</li> <li>Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>Open a Storage Redirection session with the SUT via Intel® AMT using an <b>un-secured</b> ISO OS image on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to confirm that SUT boots from redirected <b>un-secured</b> ISO OS image.</li> </ol>			



ID	AMT_036
Procedure (continued)	<p>17. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT.</p> <p>18. Close any Putty terminal window which may still be open.</p> <p>The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>19. Perform a Remote Power-Down of the SUT via Intel® AMT.</p> <p>20. Use Intel® AMT to set the boot options to use SOL and Force <b>Secure</b> Storage Redirection Boot on the SUT for the next boot.</p> <p>21. Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS <b>securely</b> boot to a redirected <b>un-secured</b> ISO OS image via Serial-Over-LAN.</p> <p>22. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</p> <p>23. Open a Storage Redirection session with the SUT via Intel® AMT using an <b>un-secured</b> ISO OS image on the management console.</p> <p>24. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>25. Request the test operator to confirm that the redirected <b>un-secured</b> ISO OS image <b>did not boot</b>.</p>
	<p>26. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT.</p> <p>27. Close any Putty terminal window which may still be open.</p> <p>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>28. Perform a Remote Power-Down of the SUT via Intel® AMT.</p> <p>29. Use Intel® AMT to set the boot options to use SOL and Force <b>Secure</b> Storage Redirection Boot on the SUT for the next boot.</p> <p>30. Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS <b>securely</b> boot to a redirected <b>secured</b> ISO OS image via Serial-Over-LAN.</p> <p>31. Request the test operator to select a secure ISO OS image on the management console hard drive for Intel® PETS to use on the next boot.</p> <p>32. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</p> <p>33. Open a Storage Redirection session with the SUT via Intel® AMT using a the <b>secured</b> ISO OS image selected by the test operator on the management console.</p> <p>34. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>35. Request the test operator to confirm that the redirected <b>secured</b> ISO OS image boot screen is displayed in the Putty window.</p>
	<p>36. Close any open SOL and Storage Redirection session(s) with the SUT via Intel® AMT.</p> <p>37. Close any Putty terminal window which may still be open.</p> <p>38. Perform a Remote Reset of the SUT via Intel® AMT.</p>
Pass Criteria	The test passes, if Intel® PETS confirms each test step succeeded.
References	For details on Storage Redirection and Secure Boot, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.7.9 SOL Character Interpretation

ID	AMT_037			
Title	Serial-Over-LAN (SOL) Character Interpretation			
Requirement	Mandatory - exempt for systems that do not support the BIOS Setup boot option			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall have its BIOS interpret Serial-Over-LAN (SOL) characters input by means of a management console as ASCII characters.			
Objective	Verify that the BIOS correctly handles and processes characters input by means of the management console via SOL as ASCII characters, and not as keystrokes, or any other interpretation.			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL is enabled in the Intel® MEBX.</p> <p>The default number of rows shown in the Putty terminal window may differ from the number of rows displayed by the BIOS. When this occurs, the Putty terminal display will incur line wrapping problems. To avoid this problem, change the settings of the Putty application to align with the BIOS via the following steps:</p> <ol style="list-style-type: none"> <li>1. Open the ".\Intel(R) Platform Enablement Test Suite\Plugins\Me\Redirection\bin\" directory.</li> <li>2. Start putty.exe, and in the Category section:             <ol style="list-style-type: none"> <li>a. Select Window, and change the Rows value to the required number of rows.</li> <li>b. Select Session, then select <i>Default Settings</i>, and finally click the Save button.</li> </ol> </li> <li>3. Close the Putty Configuration window.</li> <li>4. To confirm, start putty.exe again, and make sure Row number is set to the new value.</li> </ol>			
Procedure	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>3. Verify the SUT supports booting into BIOS by querying the Intel® AMT and checking the boot capabilities. If not supported, end the test and request the test operator to confirm the BIOS support of 'BIOS Setup' OEMCapabilities1 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> <li>4. Request the test operator to:             <ol style="list-style-type: none"> <li>a. Gracefully reboot the SUT.</li> <li>b. Enter the BIOS menu and set a strong password (a combination of lower case, upper case, alphanumeric characters, as well as punctuation characters) for BIOS menu access, and</li> <li>c. Boot the SUT to Host OS.</li> </ol> </li> <li>5. Wait for the SUT to return to S0/MeOn with the Host OS running.</li> <li>6. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>7. Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>8. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>9. Use Intel® AMT to set the BIOS Setup boot option on the SUT for the next boot.</li> <li>10. Use Intel® AMT to set the SUT boot options to use SOL Redirection on the next boot.</li> </ol>			
	<ol style="list-style-type: none"> <li>11. Close any open SOL Redirection session with the SUT via Intel® AMT. The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</li> <li>12. Inform the test operator that a system boot will be performed by Intel® PETS requesting that the BIOS boot into the BIOS setup menu.</li> <li>13. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>14. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>15. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>16. Request the test operator to:             <ol style="list-style-type: none"> <li>a. Confirm that the BIOS setup screen of the SUT is displayed in the Putty window.</li> <li>b. Confirm that the strong password can be entered into the Putty window and that the BIOS accepts it.</li> </ol> </li> </ol>			



ID	AMT_037
<b>Procedure</b> (continued)	17. Close any open SOL session with the SUT via Intel® AMT. 18. Close any Putty terminal window which may still be open. 19. Perform a Remote Reset of the SUT via Intel® AMT. 20. Request the test operator to: <ol style="list-style-type: none"> <li>Repeat test multiple times to ensure that all lower case and upper case alphanumeric and punctuation characters are correctly handled and interpreted by the BIOS.</li> <li>When final testing is complete, clear the BIOS password (if possible).</li> </ol>
<b>Pass Criteria</b>	The test passes, if all attempted strong passwords can be sent to BIOS over SOL.
<b>References</b>	For details on Terminal Emulation, refer to the <i>Intel® ME BIOS Specification</i> .

## 10.7.10 SOL Redirection During System Restart

ID	AMT_038			
<b>Title</b>	Serial-Over-LAN (SOL) Redirection during System Restart			
<b>Requirement</b>	Optional			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	An Intel® AMT compliant system shall implement BIOS boot screen redirection according to the boot options received from the GetBootOptions command during system Restart.			
<b>Objective</b>	Verify that the BIOS detects, and executes, a request (by means of boot options) to redirect text to the management console via SOL.  Intel® AMT enables remote management of the platform, including providing capabilities to read the boot options sent from the management console. These boot options can include commands to send display text from the Intel® AMT platform to the remote console by means of Serial-Over-LAN functionality. Testing described in this section will verify that BIOS has been properly enabled to support these usage models.			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that SOL is enabled in the Intel® MEBX.  The default number of rows shown in the Putty terminal window may differ from the number of rows displayed by the BIOS. When this occurs, the Putty terminal display will incur line wrapping problems. To avoid this problem, change the settings of the Putty application to align with the BIOS via the following steps: <ol style="list-style-type: none"> <li>Open the ".\Intel(R) Platform Enablement Test Suite\Plugins\Me\Redirection\bin\" directory.</li> <li>Start putty.exe, and in the Category section:               <ol style="list-style-type: none"> <li>Select Window, and change the Rows value to the required number of rows.</li> <li>Select Session, then select <i>Default Settings</i>, and finally click the Save button.</li> </ol> </li> <li>Close the Putty Configuration window.</li> <li>To confirm, start putty.exe again, and make sure Row number is set to the new value.</li> </ol>			



ID	AMT_038
Procedure	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>3. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>4. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>5. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>6. Use Intel® AMT to set the SUT boot options to use SOL Redirection on the next boot.</li> </ol>
	<ol style="list-style-type: none"> <li>7. Close any open SOL Redirection session with the SUT via Intel® AMT. The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</li> <li>8. Inform the test operator that a system restart will be performed by Intel® PETS requesting that the BIOS boot with text output redirected via Serial-Over-LAN.</li> <li>9. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>10. Gracefully restart the SUT via the Host OS.</li> <li>11. Request the test operator to confirm that the redirected text from the BIOS boot flow was displayed in the Putty window.</li> </ol>
	<ol style="list-style-type: none"> <li>12. Close any open SOL session with the SUT via Intel® AMT.</li> <li>13. Close any Putty terminal window which may still be open.</li> <li>14. Perform a Remote Reset of the SUT via Intel® AMT.</li> </ol>
Pass Criteria	The test passes, if Intel® PETS indicates all steps have passed successfully and BIOS boot screen is redirected to the Putty terminal on the management console via Serial-Over-LAN.
References	For details on SOL and ASF Boot Options, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.8 Keyboard, Video, and Mouse (KVM) Redirection

The section serves as a checklist for the environment setup and covers integration testing of Keyboard, Video, and Mouse (KVM) Redirection in Intel® AMT.

### 10.8.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows supported by Intel® PETS, and the SUT should have a version of Microsoft\* Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables.

#### Tools for testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.
- USB Storage device (USB Key): Either USB 2.0 or USB 3.0 compliant, depending on what the SUT can support. If the SUT can support both USB 2.0 and USB 3.0, the USB Storage device used for testing should be the lower of the two (USB 2.0).

In order for Intel® PETS to work properly, ensure the following:

- The SUT has a valid System UUID. This can be checked by confirming a non-zero value is reported by the Intel® MEInfo tool.
- The firmware image is configured to **not** require user consent on redirection. This can be done by checking the following value of the SPI image via the Intel® FIT tool in the 'Intel(R) AMT' tab: 'Redirection Configuration' | 'Redirection Privacy / Security Level' set to "Default".
- The SUT should have integrated graphics. If it supports switchable graphics, graphics configuration should be set to **integrated** graphics.

Where applicable, the wireless LAN interface on Intel® AMT must be on a different network/subnet than the wired LAN interface. For details on how to enter the network interface details into Intel® PETS, consult the Intel® PETS User Guide.

If the firmware image or the SUT configuration does not support some features, Intel® PETS will show those features as failing, when tested. Intel® PETS cannot determine in all cases, which features have been deactivated and should thus be skipped during testing.

All KVM tests conducted with Intel® PETS shall use a default 8bpp (bits-per-pixel) color depth configuration, when connecting to the Intel® AMT KVM server. Compliancy test PASS/FAIL conditions are based on connectivity and testing conducted at an 8bpp color depth configuration. To enable extended product testing where supported, the test operator may specify a 16bpp color depth configuration via Intel® PETS package configuration options.

#### Note:

Use of 16bpp color depth, when connecting to an Intel® AMT KVM server may not be supported at ultra-high display resolutions and/or with some system configurations, and may result in connectivity errors. Use of 8bpp color depth, when connecting to a Intel® AMT KVM server may also not be supported at screen resolutions beyond



product specification. Refer the *Intel® AMT Product Requirements* document for further details about supported KVM resolutions and color depths.

When a KVM Redirection session is active, the SUT screen will have a colored line displayed around its edges. An icon on the upper right corner of the screen will also appear, indicating that a KVM Redirection session is now active on the SUT.

In S0, the CM0-PG and CM0 Intel® ME 'MeOn' states will appear the same from Intel® APS measurement perspective. Follow the procedure below via the Host OS on the SUT to confirm if the Intel® ME is Power Gated (CM0-PG):

1. Get the PWRMBASE (32-bits) by reading the PCI configuration space B0:D31:F2 (Bus:Device:Function) at offset 48h. Information describing how to access this value may be found in either the PCH EDS or the PCH BIOS Specification.
2. Read 32-bits at PWRMBASE + 590h and verify that bits 31:24 equal F9h.
3. Read 32-bits at PWRMBASE + 594h and verify that bits 7:0 equal FFh.

## 10.8.2 KVM Redirection and BIOS Setup Boot Option over Intel® AMT LAN Network Interface

ID	AMT_040			
Title	Keyboard, Video, and Mouse (KVM) Redirection and BIOS Setup Boot Option over Intel® AMT LAN Network Interface			
Requirement	Mandatory - exempt for systems which do not support KVM or the BIOS Setup boot option			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	Verify that a KVM Redirection session can be established and functions correctly in the pre-OS environment.			
Objective	This test will verify that a KVM Redirection session can be established, the remote screen is displayed correctly, and remote keyboard (and mouse where supported) are working when the system under test is booting into a Pre-OS environment.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			



ID	AMT_040
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Verify the SUT supports booting into BIOS by querying the Intel® AMT and checking the boot capabilities.               <ol style="list-style-type: none"> <li>If supported, use Intel® AMT to set the BIOS Setup boot option on the SUT for the next boot.</li> <li>If not supported, end the test and request the test operator to confirm the BIOS support of 'BIOS Setup' OEMCapabilities1 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>
	<p>The steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the SUT will soon be powered down and the VNC Viewer window will open. When the SUT starts to boot, request the test operator to:               <ol style="list-style-type: none"> <li>Verify that the BIOS setup menu appears on the SUT screen during boot.</li> <li>Try using the keyboard (and mouse where supported) to navigate the BIOS menus.</li> </ol> </li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the redirected BIOS setup screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard (and mouse where supported) can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> </ol>
	<ol style="list-style-type: none"> <li>Close any open KVM Redirection session with the SUT via Intel® AMT.</li> <li>Close any VNC Viewer window, which may still be open.</li> <li>Perform a Remote Reset of the SUT via Intel® AMT.</li> </ol>
Pass Criteria	The test passes, if the BIOS Setup screen is redirected to management console and remote keyboard (and mouse where supported) are confirmed to be working properly.
References	For details on KVM Redirection and ASF Boot Options, refer to the <i>Intel® ME BIOS Specification</i> .





### 10.8.3 KVM Redirection and BIOS Setup Boot Option over Intel® AMT WLAN Network Interface

ID	AMT_041			
Title	Keyboard, Video, and Mouse (KVM) Redirection and BIOS Setup Boot Option over Intel® AMT WLAN Network Interface			
Requirement	Mandatory - exempt for systems which do not support KVM or the BIOS Setup boot option			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	Verify that a KVM Redirection session can be established and functions correctly in the pre-OS environment.			
Objective	This test will verify that a KVM Redirection session can be established, the remote screen is displayed correctly, and remote keyboard (and mouse where supported) are working when the system under test is booting into a Pre-OS environment.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
Procedure	1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC). 2. Verify the SUT supports booting into BIOS by querying the Intel® AMT and checking the boot capabilities. <ol style="list-style-type: none"> <li>If supported, use Intel® AMT to set the BIOS Setup boot option on the SUT for the next boot.</li> <li>If not supported, end the test and request the test operator to confirm the BIOS support of 'BIOS Setup' OEMCapabilities1 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> 3. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC). 4. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT. 5. Cancel any existing Intel® AMT user consent session, which may be active on the SUT. 6. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT. 7. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT. 8. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.			
	The steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.           9. Inform the test operator that the SUT will soon be powered down and the VNC Viewer window will open. When the SUT starts to boot, request the test operator to: <ol style="list-style-type: none"> <li>Verify that the BIOS setup menu appears on the SUT screen during boot.</li> <li>Try using the keyboard (and mouse, where supported) to navigate the BIOS menus.</li> </ol> 10. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b> . 11. Verify that Intel® AMT is available via WLAN by requesting its version. 12. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console. 13. Perform a Remote Power-Up of the SUT via Intel® AMT. 14. Request the test operator to: <ol style="list-style-type: none"> <li>Confirm that the redirected BIOS setup screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard (and mouse, where supported) can control the Host OS via the management console via the VNC Viewer.</li> </ol>			
	15. Close any open KVM Redirection session with the SUT via Intel® AMT. 16. Close any VNC Viewer window which may still be open. 17. Perform a Remote Reset of the SUT via Intel® AMT.			
Pass Criteria	The test passes, if the BIOS Setup screen is redirected to management console and remote keyboard (and mouse where supported) are confirmed to be working properly.			
References	For details on KVM Redirection and ASF Boot Options, refer to the <i>Intel® ME BIOS Specification</i> .			



## 10.8.4 KVM Redirection over Intel® AMT LAN Network Interface

ID	AMT_042			
Title	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT LAN Network Interface			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support, when the system is in Sx state and moves to S0 state.			
Objective	This test will check that when the SUT moves from S4 or S5 to S0, when KVM has been initiated, the BIOS will <b>not</b> halt and wait for the user to give consent for the KVM Redirection session, and the user consent opt-in option should <b>not</b> be displayed on the platform under test. In all cases, the SUT's screen is visible in the Virtual Network Computing (VNC) Viewer on the management console.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
Procedure S5→S0 Flow	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol> <p>The steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the SUT will soon be powered down and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:               <ol style="list-style-type: none"> <li>Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during boot.</li> <li>Try using the keyboard and mouse to control the Host OS.</li> </ol> </li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> </ol>			



ID	AMT_042
<b>Procedure</b> (continued)  <b>S4→S0 Flow</b>  <b>Intel® MEBX</b> <b>Override Check</b>	<p>12. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>13. Close any VNC Viewer window which may still be open.</p> <p>14. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>15. Inform the test operator that the SUT will soon be sent into hibernation state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:</p> <ol style="list-style-type: none"> <li>Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during resume from hibernation.</li> <li>Try using the keyboard and mouse to control the Host OS.</li> </ol> <p>16. Hibernate to S4/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>17. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</p> <p>18. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>19. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol>
	<p>20. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>21. Close any VNC Viewer window which may still be open.</p> <p>22. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>23. The remaining steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>24. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Gracefully reboot the SUT.</li> <li>Enter the Intel® MEBX on the SUT and <b>disable</b> KVM, and</li> <li>Boot the SUT to Host OS.</li> </ol> <p>25. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>26. Attempt to open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console. Failure to open the session by error indicating the KVM interface is disabled indicates success for the test step, otherwise the test step fails.</p> <p>27. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Boot the SUT,</li> <li>Enter the Intel® MEBX on the SUT and <b>enable</b> KVM, and</li> <li>Boot the SUT to Host OS.</li> </ol>
	<p>28. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>29. Close any VNC Viewer window, which may still be open.</p>
<b>Pass Criteria</b>	<p>The test passes, if all attempted KVM Redirection sessions are viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT. During system boot or resume, the Intel® MEBX hot-key (Ctrl+P or other keystroke) prompt is not displayed on the SUT.</p>
<b>References</b>	<p>For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i>.</p>



## 10.8.5 KVM Redirection over Intel® AMT WLAN Network Interface

ID	AMT_043			
Title	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT WLAN Network Interface			
Requirement	Mandatory - exempt for systems, which do not support KVM with internal graphics			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support, when the system is in Sx state and moves to S0 state.			
Objective	This test will check that when the SUT moves from S4 or S5 to S0, when KVM has been initiated, the BIOS will <b>not</b> halt and wait for the user to give consent for the KVM Redirection session, and the user consent opt-in option should <b>not</b> be displayed on the platform under test. In all cases, the SUT's screen is visible in the Virtual Network Computing (VNC) Viewer on the management console.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
Procedure S5→S0 Flow	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).</li> <li>Ensure the Host OS Wake on Wireless LAN is <b>disabled</b>.</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol> <p>The steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the SUT will soon be powered down and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:               <ol style="list-style-type: none"> <li>Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during boot.</li> <li>Try using the keyboard and mouse to control the Host OS.</li> </ol> </li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> </ol>			



ID	AMT_043
<p><b>Procedure</b> (continued)</p> <p><b>S4→S0 Flow</b></p> <p><b>Intel® MEBX Override Check</b></p>	<p>15. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>16. Close any VNC Viewer window which may still be open.</p> <p>17. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>18. Inform the test operator that the SUT will soon be sent into hibernation state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:</p> <ol style="list-style-type: none"> <li>Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during resume from hibernation.</li> <li>Try using the keyboard and mouse to control the Host OS.</li> </ol> <p>19. Hibernate to S4/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>20. Verify that Intel® AMT is available via WLAN by requesting its version.</p> <p>21. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</p> <p>22. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>23. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> <p>24. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>25. Close any VNC Viewer window which may still be open.</p> <p>26. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>27. The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>28. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Gracefully reboot the SUT,</li> <li>Enter the Intel® MEBX on the SUT and <b>disable</b> KVM, and</li> <li>Boot the SUT to Host OS.</li> </ol> <p>29. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>30. Attempt to open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console. Failure to open the session by error indicating the KVM interface is disabled indicates success for the test step, otherwise the test step fails.</p> <p>31. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Boot the SUT,</li> <li>Enter the Intel® MEBX on the SUT and <b>enable</b> KVM, and</li> <li>Boot the SUT to Host OS.</li> </ol> <p>32. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>33. Close any VNC Viewer window which may still be open.</p>
<b>Pass Criteria</b>	The test passes, if all attempted KVM Redirection sessions are viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT. During system boot or resume, the Intel® MEBX hot-key (Ctrl+P or other keystroke) prompt is not displayed on the SUT.
<b>References</b>	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.8.6 KVM Redirection over Intel® AMT LAN Network Interface with User Consent Enabled

ID	AMT_044			
Title	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT LAN Network Interface with User Consent Enabled			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support, when the system is in Sx state and moves to S0 state.			
Objective	This test will check that when the SUT moves from S3, S4 or S5 to S0, when KVM has been initiated, the BIOS will halt and wait for the user to give consent for the KVM Redirection session, and the user consent opt-in option should be displayed on the platform under test. In all cases, the SUT's screen is visible in the Virtual Network Computing (VNC) Viewer on the management console.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>			
	<p>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the SUT will soon be powered down and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:               <ol style="list-style-type: none"> <li>Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during boot.</li> <li>Copy the user consent code from the SUT screen to the VNC Viewer.</li> <li>Try using the keyboard and mouse to control the Host OS.</li> </ol> </li> <li>Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT. A user consent code will be displayed on the SUT screen.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Enter the user consent code into the VNC Viewer on the management console.</li> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> </ol>			



ID	AMT_044
<b>Procedure</b> (continued) <b>S4→S0 Flow</b>	<p>12. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>13. Close any VNC Viewer window which may still be open.</p> <p>14. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</p> <p>15. Attempt to bring the SUT to a base state via the following:</p> <ul style="list-style-type: none"> <li>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>b. Verify that the Host OS on the SUT is available.</li> <li>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</li> </ul> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ul style="list-style-type: none"> <li>a. Bring the system to G3 and wait 10 seconds.</li> <li>b. Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>c. Briefly press the Power Button on the SUT.</li> </ul> <p>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>16. Inform the test operator that the SUT will soon be sent into hibernation state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:</p> <ul style="list-style-type: none"> <li>a. Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during resume from hibernation.</li> <li>b. Copy the user consent code from the SUT screen to the VNC Viewer.</li> <li>c. Try using the keyboard and mouse to control the Host OS.</li> </ul> <p>17. Hibernate to S4/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>18. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</p> <p>19. Perform a Remote Power-Up of the SUT via Intel® AMT. A user consent code will be displayed on the SUT screen.</p> <p>20. Request the test operator to:</p> <ul style="list-style-type: none"> <li>a. Enter the user consent code into the VNC Viewer on the management console.</li> <li>b. Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>c. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ul>



ID	AMT_044
<p><b>Procedure</b> (continued)</p> <p><b>S3→S0 Flow</b></p>	<p>21. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>22. Close any VNC Viewer window, which may still be open.</p> <p>23. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</p> <p>24. Attempt to bring the SUT to a base state via the following:</p> <ul style="list-style-type: none"> <li>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>b. Verify that the Host OS on the SUT is available.</li> <li>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</li> </ul> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ul style="list-style-type: none"> <li>a. Bring the system to G3 and wait 10 seconds.</li> <li>b. Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>c. Briefly press the Power Button on the SUT.</li> </ul> <p>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p><b>NOTE:</b> In the case the SUT is operating in Modern Standby or Microsoft* Windows InstantGo* mode, the test shall automatically end here, and the results thus far reported to the test operator as the final test results.</p> <p>25. Inform the test operator that the SUT will soon be sent into suspend state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:</p> <ul style="list-style-type: none"> <li>a. Copy the user consent code from the SUT screen to the VNC Viewer.</li> <li>b. Try using the keyboard and mouse to control the Host OS.</li> </ul> <p>26. Record the Host OS last boot time on the SUT (to verify successful suspend/resume).</p> <p>27. Suspend to S3/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>28. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</p> <p>29. Inform the test operator that "Due to OS behavior change, only user-initiated input can turn on display and request test operator to press the keyboard or mouse after console send Remote Power-Up to SUT".</p> <p>30. Perform a Remote Power-Up of the SUT via Intel® AMT. A user consent code will be displayed on the SUT screen.</p> <p>31. Wait until system resumes back to the Host OS.</p> <p>32. Verify the Host OS last boot time on the SUT <b>does</b> match the boot time recorded before the suspend.</p> <p>33. Request the test operator to:</p> <ul style="list-style-type: none"> <li>a. Enter the user consent code into the VNC Viewer on the management console.</li> <li>b. Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>c. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ul> <p>34. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>35. Close any VNC Viewer window, which may still be open.</p> <p>36. Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</p>
<p><b>Pass Criteria</b></p>	<p>The test passes, if all attempted KVM Redirection sessions are viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT. During system boot or resume, the Intel® MEBX hot-key (Ctrl+P or other keystroke) prompt is not displayed on the SUT. Additionally, no KVM redirection shall be permitted without first confirming the user consent code displayed on the SUT screen.</p>
<p><b>References</b></p>	<p>For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i>.</p>





## 10.8.7 KVM Redirection over Intel® AMT WLAN Network Interface with User Consent Enabled

ID	AMT_045			
Title	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT WLAN Network Interface with User Consent Enabled			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support, when the system is in Sx state and moves to S0 state.			
Objective	This test will check that, when the SUT moves from S3, S4 or S5 to S0 and KVM has been initiated, then the BIOS will halt and wait for the user to give consent for the KVM Redirection session, and the user consent opt-in option should be displayed on the platform under test. In all cases, the SUT's screen is visible in the Virtual Network Computing (VNC) Viewer on the management console.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
Procedure	1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC). 2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC). 3. Ensure the Host OS Wake on Wireless LAN is <b>disabled</b> . 4. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT. 5. Cancel any existing Intel® AMT user consent session which may be active on the SUT. 6. Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> on the SUT. 7. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT. 8. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.			
	The remaining steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped. 9. Inform the test operator that the SUT will soon be powered down and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to: a. Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during boot. b. Copy the user consent code from the SUT screen to the VNC Viewer. c. Try using the keyboard and mouse to control the Host OS. 10. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b> . 11. Verify that Intel® AMT is available via WLAN by requesting its version. 12. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console. 13. Perform a Remote Power-Up of the SUT via Intel® AMT. A user consent code will be displayed on the SUT screen. 14. Request the test operator to: a. Enter the user consent code into the VNC Viewer on the management console. b. Confirm that the redirected screen from the SUT appears in the VNC Viewer. c. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.			



ID	AMT_045
<b>Procedure</b> (continued) <b>S4→S0 Flow</b>	<ol style="list-style-type: none"><li>15. Close any open KVM Redirection session with the SUT via Intel® AMT.</li><li>16. Close any VNC Viewer window which may still be open.</li><li>17. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li><li>18. Attempt to bring the SUT to a base state via the following:<ol style="list-style-type: none"><li>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>b. Verify that the Host OS on the SUT is available.</li><li>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</li></ol>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.<ol style="list-style-type: none"><li>a. Bring the system to G3 and wait 10 seconds.</li><li>b. Set system power configuration to AC/DC and wait another 10 seconds.</li><li>c. Briefly press the Power Button on the SUT.</li></ol>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</li><li>19. Inform the test operator that the SUT will soon be sent into hibernation state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:<ol style="list-style-type: none"><li>a. Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during resume from hibernation.</li><li>b. Copy the user consent code from the SUT screen to the VNC Viewer.</li><li>c. Try using the keyboard and mouse to control the Host OS.</li></ol></li><li>20. Hibernate to S4/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li><li>21. Verify that Intel® AMT is available via WLAN by requesting its version.</li><li>22. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li><li>23. Perform a Remote Power-Up of the SUT via Intel® AMT. A user consent code will be displayed on the SUT screen.</li><li>24. Request the test operator to:<ol style="list-style-type: none"><li>a. Enter the user consent code into the VNC Viewer on the management console.</li><li>b. Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li><li>c. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li></ol></li></ol>



ID	AMT_045
<p><b>Procedure</b> (continued)</p> <p><b>S3→S0 Flow</b></p>	<p>25. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>26. Close any VNC Viewer window, which may still be open.</p> <p>27. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</p> <p>28. Attempt to bring the SUT to a base state via the following:</p> <ul style="list-style-type: none"> <li>a. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>b. Verify that the Host OS on the SUT is available.</li> <li>c. Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</li> </ul> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ul style="list-style-type: none"> <li>a. Bring the system to G3 and wait 10 seconds.</li> <li>b. Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>c. Briefly press the Power Button on the SUT.</li> </ul> <p>The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p><b>NOTE:</b> In the case the SUT is operating in Modern Standby or Microsoft* Windows InstantGo* mode, the test shall automatically end here, and the results thus far reported to the test operator as the final test results.</p> <p>29. Inform the test operator that the SUT will soon be sent into suspend state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:</p> <ul style="list-style-type: none"> <li>a. Copy the user consent code from the SUT screen to the VNC Viewer.</li> <li>b. Try using the keyboard and mouse to control the Host OS.</li> </ul> <p>30. Record the Host OS last boot time on the SUT (to verify successful suspend/resume).</p> <p>31. Suspend to S3/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>32. Verify that Intel® AMT is available via WLAN by requesting its version.</p> <p>33. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</p> <p>34. Inform the test operator that "Due to OS behavior change, only user-initiated input can turn on display and request test operator to press the keyboard or mouse after console send Remote Power-Up to SUT".</p> <p>35. Perform a Remote Power-Up of the SUT via Intel® AMT. A user consent code will be displayed on the SUT screen.</p> <p>36. Wait until system resumes back to the Host OS.</p> <p>37. Verify the Host OS last boot time on the SUT <b>does</b> match the boot time recorded before the suspend.</p> <p>38. Request the test operator to:</p> <ul style="list-style-type: none"> <li>a. Enter the user consent code into the VNC Viewer on the management console.</li> <li>b. Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>c. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ul> <p>39. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>40. Close any VNC Viewer window, which may still be open.</p> <p>41. Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</p>
<b>Pass Criteria</b>	<p>The test passes, if all attempted KVM Redirection sessions are viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT. During system boot or resume, the Intel® MEBX hot-key (Ctrl+P or other keystroke) prompt is not displayed on the SUT. Additionally, no KVM redirection shall be permitted without first confirming the user consent code displayed on the SUT screen.</p>
<b>References</b>	<p>For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i>.</p>



## 10.8.8 KVM Redirection During Warm Reset Over Intel® AMT LAN Network Interface

ID	AMT_046			
Title	Keyboard, Video, and Mouse (KVM) Redirection during Warm Reset over Intel® AMT LAN Network Interface			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support during warm reset.			
Objective	This test will check that when the SUT experiences a warm reset that an open KVM Redirection session remains connected throughout. Additionally, when a User Consent session is established, a new session is not requested as a result of the warm reset.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
Procedure	1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). 2. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT. 3. Cancel any existing Intel® AMT user consent session which may be active on the SUT. 4. Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> on the SUT. 5. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT. 6. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.			
	<p>The remaining steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> 7. Inform the test operator that the VNC Viewer window will open, and that when it does: a. Copy the user consent code from the SUT screen to the VNC Viewer. b. Try using the keyboard and mouse to control the Host OS. 8. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console. 9. Request the test operator to: a. Enter the user consent code into the VNC Viewer on the management console. b. Confirm that the redirected screen from the SUT appears in the VNC Viewer. c. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.			
S0→S0 Flow	<p>The steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> 10. Inform the test operator that the SUT will soon be restarted, and to try using the keyboard and mouse to control the Host OS afterwards. 11. Perform a Remote Reset of the SUT via Intel® AMT. 12. Wait until system reboots back to the Host OS. 13. Request the test operator to: a. Confirm that the SUT did not display a user consent code following the reset. b. Confirm that the VNC Viewer on the management console did not request a user consent code following the reset. c. Confirm that the redirected screen from the SUT appears in the VNC Viewer. d. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer. 14. Perform the following additional sub-steps for two (2) cycles each: a. Verify that the Host OS on the SUT is available. b. Record the Host OS last boot time on the SUT (to verify successful restart). c. Perform a graceful restart of the SUT via Host OS. d. Verify that the SUT is in S0/MeOn (CM0,CM0-PG). e. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.			



ID	AMT_046
<b>Procedure</b> (continued)	<p>15. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>LAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>16. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>17. Close any VNC Viewer window which may still be open.</p> <p>18. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</p>
<b>Pass Criteria</b>	<p>The test passes, if the KVM Redirection session remains up and the platform under test screen visible on the remote viewer, including BIOS screens, during the warm reset, and that when passcode is entered before the warm reset, the system does not display the user consent code.</p>
<b>References</b>	<p>For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i>.</p>



## 10.8.9 KVM Redirection During Warm Reset over Intel® AMT WLAN Network Interface

ID	AMT_047			
Title	Keyboard, Video, and Mouse (KVM) Redirection during Warm Reset over Intel® AMT WLAN Network Interface			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics			
System	<div>Form Factor</div> <div> <input checked="" type="checkbox"/> Desktop   <input checked="" type="checkbox"/> Workstation  <input checked="" type="checkbox"/> Mobile </div>	<div>System Power Model</div> <div> <input checked="" type="checkbox"/> Standard  <input checked="" type="checkbox"/> Modern Standby or InstantGo* </div>	<div>Intel® AMT Network Interface</div> <div> <input type="checkbox"/> LAN   <input type="checkbox"/> Either Used  <input checked="" type="checkbox"/> WLAN   <input type="checkbox"/> Not Used </div>	<div>LAN Type</div> <div> <input type="checkbox"/> Integrated LAN  <input type="checkbox"/> Discrete LAN  <input type="checkbox"/> TBT Dock LAN </div>
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support during warm reset.			
Objective	This test will check that when the SUT experiences a warm reset that an open KVM Redirection session remains connected throughout. Additionally, when a User Consent session is established, a new session is not requested as a result of the warm reset.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>			
	<p>The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the VNC Viewer window will open, and that when it does: <ol style="list-style-type: none"> <li>Copy the user consent code from the SUT screen to the VNC Viewer.</li> <li>Try using the keyboard and mouse to control the Host OS.</li> </ol> </li> <li>Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Request the test operator to: <ol style="list-style-type: none"> <li>Enter the user consent code into the VNC Viewer on the management console.</li> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> </ol> <p>The steps within this block shall be executed as, if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the SUT will soon be restarted, and to try using the keyboard and mouse to control the Host OS afterwards.</li> <li>Perform a Remote Reset of the SUT via Intel® AMT.</li> <li>Wait until system reboots back to the Host OS.</li> <li>Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>Request the test operator to: <ol style="list-style-type: none"> <li>Confirm that the SUT did not display a user consent code following the reset.</li> <li>Confirm that the VNC Viewer on the management console did not request a user consent code following the reset.</li> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> <li>Perform the following additional sub-steps for two (2) cycles each: <ol style="list-style-type: none"> <li>Verify that the Host OS on the SUT is available.</li> <li>Record the Host OS last boot time on the SUT (to verify successful restart).</li> <li>Perform a graceful restart of the SUT via Host OS.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before the restart.</li> </ol> </li> </ol>			



ID	AMT_047
<b>Procedure</b> (continued)	<p>18. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>19. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>20. Close any VNC Viewer window which may still be open.</p> <p>21. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</p>
<b>Pass Criteria</b>	<p>The test passes, if the KVM Redirection session remains up and the platform under test screen visible on the remote viewer, including BIOS screens, during the warm reset, and that when passcode is entered before the warm reset, the system does not display the user consent code.</p>
<b>References</b>	<p>For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i>.</p>



### 10.8.10 KVM Redirection with S0 Low Power Idle via Intel® AMT LAN Network Interface

ID	AMT_048			
Title	Keyboard, Video, and Mouse (KVM) Redirection with S0 Low Power Idle state, as with Modern Standby or Microsoft* Windows InstantGo* mode, via Intel® AMT LAN Network Interface			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics			
System	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support, when the system is in S0 Low Power Idle state and move to S0 state.			
Objective	This test will check that the SUT moves from S0 Low Power Idle state to S0, when KVM has been initiated.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics. The SUT must be configured to work in Modern Standby or Microsoft* Windows InstantGo* mode.			
Procedure	<ol style="list-style-type: none"><li>1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li><li>2. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li><li>3. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li><li>4. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li><li>5. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li><li>6. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li></ol> <p>The steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"><li>7. Inform the test operator that after SUT enters S0 Low Power Idle state, the VNC Viewer window will open. When the VNC Viewer window opens, request the test operator to try using the keyboard and mouse to Activate and control the Host OS on the SUT.</li><li>8. Request the test operator to manually place the SUT into S0 Low Power Idle state.</li><li>9. Verify that the SUT has moved into S0 Low Power Idle state.</li><li>10. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li><li>11. Request the test operator to:<ol style="list-style-type: none"><li>a. Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li><li>b. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li></ol></li><li>12. Close any open KVM Redirection session with the SUT via Intel® AMT.</li><li>13. Close any VNC Viewer window which may still be open.</li></ol>			
Pass Criteria	The test passes, if the KVM Redirection session can be viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT.			
References	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> .			

### 10.8.11 KVM Redirection with S0 Low Power Idle via Intel® AMT WLAN Network Interface

ID	AMT_049
Title	Keyboard, Video, and Mouse (KVM) Redirection with S0 Low Power Idle state, as with Modern Standby or Microsoft* Windows InstantGo* mode, via Intel® AMT WLAN Network Interface
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics





ID	AMT_049			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support, when the system is in S0 Low Power Idle state and move to S0 state.			
Objective	This test will check that the SUT moves from S0 Low Power Idle state to S0, when KVM has been initiated.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics. The SUT must be configured to work in Modern Standby or Microsoft® Windows InstantGo* mode.			
<b>Procedure</b>  <b>S0LP→S0 Flow</b>	1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0). 2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0). 3. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT. 4. Cancel any existing Intel® AMT user consent session which may be active on the SUT. 5. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT. 6. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT. 7. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.			
	The steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.			
	8. Inform the test operator that after SUT enters S0 Low Power Idle state, the VNC Viewer window will open. When the VNC Viewer window opens, request the test operator to try using the keyboard and mouse to Activate and control the Host OS on the SUT. 9. Request the test operator to manually place the SUT into S0 Low Power Idle state. 10. Verify that the SUT has moved into S0 Low Power Idle state. 11. Verify that Intel® AMT is available via WLAN by requesting its version. 12. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console. 13. Request the test operator to: a. Confirm that the redirected screen from the SUT appears in the VNC Viewer. b. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer. 14. Close any open KVM Redirection session with the SUT via Intel® AMT. 15. Close any VNC Viewer window which may still be open.			
Pass Criteria	The test passes, if the KVM Redirection session can be viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT.			
References	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> .			



### 10.8.12 KVM Redirection in Discrete Graphics Mode

ID	AMT_050				
Title	Keyboard, Video, and Mouse (KVM) Redirection in Discrete Graphics Mode				
Requirement	Mandatory - exempt for systems which <b>do not have</b> both internal and discrete graphics				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
LAN Type					
<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN					
Method	Automated by Intel® PETS with test operator interaction				
Description	This test checks SUT behavior when a KVM Redirection session is initiated, while the system is in discrete graphics mode.				
Objective	This test will ensure that the KVM Redirection session fails to start when the SUT is operating in discrete graphics mode.				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. The graphics configuration should be set to <b>discrete</b> graphics.				
Procedure	<ol style="list-style-type: none"><li>1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li><li>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0), if the WLAN network interface is used.</li><li>3. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li><li>4. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li><li>5. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li><li>6. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li><li>7. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li><li>8. Inform the test operator that the VNC Viewer will attempt to open. Request the test operator to wait at least 30 seconds to confirm the KVM Redirection session failed to start.</li><li>9. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li><li>10. Request the test operator to confirm that the KVM Redirection session did not start.</li></ol>				
Pass Criteria	The test passes, if the KVM Redirection session fails to start.				
References	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> .				

### 10.8.13 KVM Redirection and Switchable Graphics

ID	AMT_051				
Title	Keyboard, Video, and Mouse (KVM) Redirection and Switchable Graphics				
Requirement	Mandatory - exempt for systems which <b>do not have</b> both internal and discrete graphics				
System	Form Factor		System Power Model		Intel® AMT Network Interface
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Workstation	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
LAN Type					
<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN					
Method	Automated by Intel® PETS with test operator interaction				
Description	This test checks SUT behavior, when a KVM Redirection session is initiated, while the system is in integrated graphics mode and then switched to discrete graphics mode.				
Objective	This test will ensure that the Graphics Device Interface (GDI) alerts the Intel® ME, when it switches to discrete graphics mode. The Intel® ME should display the proper error, when this condition occurs. Switching may be done by means of the switchable graphics control application (not provided by Intel).				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. The graphics configuration should be set to <b>integrated</b> graphics.				



ID	AMT_051
Procedure	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0), if the WLAN network interface is used.</li> <li>3. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>4. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>5. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>6. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>7. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>
	<p>The steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>8. Inform the test operator that the VNC Viewer will soon open.</li> <li>9. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>10. Request the test operator to: <ol style="list-style-type: none"> <li>a. Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>b. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> <li>c. Change the SUT from integrated graphics mode to discrete graphics mode.</li> </ol> </li> </ol> <p><b>NOTE:</b> The KVM Redirection session should automatically disconnect.</p> <ol style="list-style-type: none"> <li>d. Wait atleast 30 seconds to confirm the KVM Redirection session closed.</li> <li>e. Change the SUT back to integrated graphics mode from discrete graphics mode.</li> </ol>
	<ol style="list-style-type: none"> <li>11. Close any open KVM Redirection session with the SUT via Intel® AMT.</li> <li>12. Close any VNC Viewer window which may still be open.</li> </ol>
Pass Criteria	The test passes, if KVM Redirection session is disconnected.
References	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.8.14 KVM with SOL and Storage Redirection

ID	AMT_052			
Title	Keyboard, Video, and Mouse (KVM) with Serial-Over-LAN (SOL) and Storage Redirection			
Requirement	Mandatory - Exempt for systems, which do not support KVM with internal graphics			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	This test checks that SOL and Storage Redirection can be activated during an open KVM Redirection session between a management console and the SUT.			
Objective	Verify that the BIOS detects, and executes, a request (by using boot options) to perform SOL Redirection and map an ISO OS image to a drive via Storage Redirection during an active KVM Redirection session.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM, SOL, and Storage Redirection are enabled in the Intel® MEBX. Also, ensure Windows* Boot Manager (WBM) is in the first boot priority. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.			
<b>Procedure</b>  <b>S0→S0 Flow</b>	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>			
	<p>The steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the VNC Viewer will soon open.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> <li>Use Intel® AMT to set the SUT boot options to use SOL Redirection on the next boot.</li> <li>Inform the test operator that a system reboot will be performed by Intel® PETS requesting that the BIOS boot with text output redirected via Serial-Over-LAN.</li> <li>Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>Open a Storage Redirection session with the SUT via Intel® AMT using an ISO OS image on the management console.</li> <li>Perform a graceful Restart via the Host OS.</li> <li>Wait until system reboots back to the Host OS.</li> <li>Verify the Intel® AMT SOL device on the SUT exists and is operating normally.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the Storage Redirected ISO OS image appears as a mapped drive in the Host OS.</li> <li>Confirm that the redirected screen from the SUT still appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can still control the Host OS via the management console via the VNC Viewer.</li> <li>Confirm that the redirected text from the BIOS boot flow was displayed in the Putty window.</li> </ol> </li> <li>Close any open KVM Redirection session with the SUT via Intel® AMT.</li> <li>Close any open Storage Redirection session with the SUT via Intel® AMT.</li> <li>Close any open SOL Redirection session with the SUT via Intel® AMT.</li> <li>Close any VNC Viewer window, which may still be open.</li> <li>Close any Putty terminal window, which may still be open.</li> </ol>			



<b>ID</b>	<b>AMT_052</b>
<b>Pass Criteria</b>	The test passes, if SOL and Storage Redirection sessions were successfully completed, while the KVM Redirection session was running, and the mapped Storage Redirection drive is accessible from the Host OS of the SUT.
<b>References</b>	For details on KVM, SOL and Storage Redirection, refer to the <i>Intel® ME BIOS Specification</i> .

### 10.8.15 KVM Redirection and USB Port Availability Check

<b>ID</b>	<b>AMT_053</b>			
<b>Title</b>	Keyboard, Video, and Mouse (KVM) Redirection and USB Port Availability Check			
<b>Requirement</b>	Mandatory - exempt for systems, which do not support KVM with internal graphics			
<b>System</b>	<b>Form Factor</b>	<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	<b>LAN Type</b>
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	This test checks that all USB ports of the SUT are working correctly during a KVM Redirection session.			
<b>Objective</b>	Verify that the BIOS properly enables USB ports other than those needed for KVM Redirection support during a KVM Redirection session.			
	This test shall be run once with the SUT configured to enable USB 2.0, and once more with the SUT configured to enable USB 3.0 where supported. If only one of those versions of USB is supported on the SUT, then this test shall be run once with the SUT configured to enable the supported USB version.			
<b>Setup</b>	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM Redirection is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.</p> <p>The USB Storage device (USB Key) used in the test may be either USB 2.0 or USB 3.0 compliant, depending on what the SUT can support. If the SUT can support both USB 2.0 and USB 3.0, the USB Storage device should be the lower of the two (USB 2.0).</p>			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0), if the WLAN network interface is used.</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>			
	<p>The steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Inform the test operator that the VNC Viewer will soon open.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> <li>Confirm that the USB keyboard and mouse on the SUT are both working.</li> <li>Confirm a USB Storage device (USB Key) can be connected to each USB port on the SUT and can be accessed via the Host OS thereon.</li> </ol> </li> </ol>			
	<ol style="list-style-type: none"> <li>Close any open KVM Redirection session with the SUT via Intel® AMT.</li> <li>Close any VNC Viewer window, which may still be open.</li> <li>Request the test operator to re-run the test, as needed, for each available USB version supported by the SUT.</li> </ol>			
<b>Pass Criteria</b>	This test passes, if all USB ports are working correctly during the KVM Redirection session for all supported USB versions on the SUT.			
<b>References</b>	For details on KVM Redirection and USB device support, refer to the <i>Intel® ME BIOS Specification</i> .			



## 10.8.16 KVM Redirection With Remote Screen Blank (RSB) Support

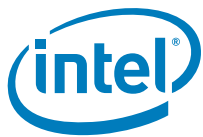
ID	AMT_054			
Title	Keyboard, Video, and Mouse (KVM) Redirection with Remote Screen Blank (RSB) Support			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	Remote screen blank is targeted at public unattended systems that require the capability to blank the screen display while IT personnel manages the system.			
Objective	Verify that remote screen blank works properly.			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM Redirection is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics. Ensure that remote screen blanking ('Firmware KVM Screen Blanking') is enabled in the firmware image on the SUT and that the display is connected to an Intel® Graphics port.			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> <li>Terminate any active remote screen blanking session on the SUT via Intel® AMT. The remaining steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</li> <li>Inform the test operator that the VNC Viewer will soon open.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> <li>Inform the test operator that remote screen blanking will be activated, whereby the screen on the SUT should become <b>blank</b>.</li> <li>Activate a remote screen blanking session on the SUT via Intel® AMT.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the display of the SUT is <b>blank</b>.</li> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> <li>Perform a graceful Restart via the Host OS.</li> <li>Wait until system reboots back to the Host OS.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the display of the SUT remains <b>blank</b>.</li> <li>Confirm that the redirected screen from the SUT remains in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can continue to control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> <li>Inform the test operator that remote screen blanking will be terminated, whereby the screen on the SUT should become <b>restored</b>.</li> <li>Terminate the remote screen blanking session on the SUT via Intel® AMT.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the display of the SUT is <b>restored</b>.</li> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> </ol>			



ID	AMT_054
<b>Procedure (continued)</b>	21. Terminate any active remote screen blanking session on the SUT via Intel® AMT. 22. Close any open KVM Redirection session with the SUT via Intel® AMT. 23. Close any VNC Viewer window, which may still be open.
<b>Pass Criteria</b>	The test passes, if the KVM Redirection session stays available during all test stages, while display blanks and turns back on according to the remote screen blank state.
<b>References</b>	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> . For details on Firmware KVM Screen Blanking configuration, refer to the <i>Intel® ME Firmware Bring Up Guide</i> .

### 10.8.17 KVM Redirection with S0 Low Power Idle and Intel® ME Power Gating

ID	AMT_055			
<b>Title</b>	Keyboard, Video, and Mouse (KVM) Redirection with S0 Low Power Idle state, as with Modern Standby or Microsoft* Windows InstantGo* mode, and Intel® ME Power Gating			
<b>Requirement</b>	Mandatory - exempt for systems, which do not support KVM with internal graphics			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	An Intel® AMT compliant system shall implement KVM redirection support, when the system is in S0 Low Power Idle state and move to S0 state.			
<b>Objective</b>	This test will check that the SUT moves from S0 Low Power Idle state to S0, when KVM has been initiated.			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics. The SUT must be configured to work in Modern Standby or Microsoft* Windows InstantGo* mode.			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 2 (Enabled in S0).</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>			
<b>S0LP→S0 Flow</b>	<p>The steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <ol style="list-style-type: none"> <li>Keep the host in S0 by performing host-only activity; allowing the Intel® ME to idle (approximately 2 to 3 seconds) and subsequently enter a power gated state.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>Inform the test operator that after SUT enters S0 Low Power Idle state, the VNC Viewer window will open. When the VNC Viewer window opens, request the test operator to try using the keyboard and mouse to Activate and control the Host OS on the SUT.</li> <li>Request the test operator to manually place the SUT into S0 Low Power Idle state.</li> <li>Verify that the SUT has moved into S0 Low Power Idle state.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> <li>Close any open KVM Redirection session with the SUT via Intel® AMT.</li> <li>Close any VNC Viewer window, which may still be open.</li> </ol>			
<b>Pass Criteria</b>	The test passes, if the Intel® ME enters power gated state and afterward the KVM Redirection session can be viewed via VNC Viewer on the management console. Keyboard/mouse functionality is redirected to the Host OS on the SUT during the KVM Redirection session.			



<b>ID</b>	<b>AMT_055</b>
<b>References</b>	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> .





## 10.8.18 KVM Redirection over Intel® AMT WLAN Network Interface for Systems Supporting Wake On Wireless LAN

ID	AMT_056			
Title	Keyboard, Video, and Mouse (KVM) Redirection over Intel® AMT WLAN Network Interface for Systems supporting Wake on Wireless LAN			
Requirement	Mandatory - exempt for systems which do not support KVM with internal graphics and Wake on Wireless LAN			
System	Form Factor	System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	An Intel® AMT compliant system shall implement KVM redirection support when the system is in S3 state and moves to S0 state.			
Objective	This test will check that when the SUT moves from S3 to S0, when KVM has been initiated, the BIOS will <b>not</b> halt and wait for the user to give consent for the KVM Redirection session, and the user consent opt-in option should <b>not</b> be displayed on the platform under test. The SUT's screen is visible in the Virtual Network Computing (VNC) Viewer on the management console.			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.</p> <p><b>NOTE:</b> In order to fully implement Wake on Wireless LAN (WoWLAN) in Sx states, the host BIOS must set HOST_WLAN_PP_EN. For more further details, refer to the PCH <i>External Design Specification (EDS)</i> and the PCH <i>Platform Design Guide (PDG)</i>. Failure to properly set the HOST_WLAN_PP_EN bit may result in failures for this test.</p>			
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC).</li> <li>Ensure the Host OS Wake on Wireless LAN is <b>enabled</b>.</li> <li>Verify that Intel® AMT is available via WLAN by requesting its version.</li> <li>Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> </ol>			
	<p>The steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p><b>S3→S0 Flow</b></p> <ol style="list-style-type: none"> <li>Inform the test operator that the SUT will soon be sent into suspend state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to try using the keyboard and mouse to control the Host OS.</li> <li>Suspend to S3/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>Wait for the SUT to return to S0/MeOn with the Host OS running.</li> <li>Request the test operator to:               <ol style="list-style-type: none"> <li>Press the ESC key or move the mouse in the VNC Viewer (necessary to activate the SUT screen on some systems).</li> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> <li>Close any open KVM Redirection session with the SUT via Intel® AMT.</li> <li>Close any VNC Viewer window which may still be open.</li> </ol>			
Pass Criteria	The test passes, if the attempted KVM Redirection session is viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT.			
References	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> as well as the <i>Intel® AMT and Wake On Wireless LAN Coexistence</i> feature overview.			



## 10.8.19 KVM Redirection on Headless Configurations

ID	AMT_059			
Title	Keyboard, Video, and Mouse (KVM) Redirection on Headless Configurations			
Requirement	Mandatory - Exempt for systems, which do not support KVM with internal graphics and not supporting headless configurations (refer below)			
System	<div>Form Factor</div> <div> <input checked="" type="checkbox"/> Desktop           <input checked="" type="checkbox"/> Workstation           <input checked="" type="checkbox"/> Mobile         </div>	<div>System Power Model</div> <div> <input checked="" type="checkbox"/> Standard           <input checked="" type="checkbox"/> Modern Standby or InstantGo*         </div>	<div>Intel® AMT Network Interface</div> <div> <input type="checkbox"/> LAN           <input checked="" type="checkbox"/> Either Used           <input type="checkbox"/> WLAN           <input type="checkbox"/> Not Used         </div>	<div>LAN Type</div> <div> <input checked="" type="checkbox"/> Integrated LAN           <input checked="" type="checkbox"/> Discrete LAN           <input type="checkbox"/> TBT Dock LAN         </div>
Method	Automated by Intel® PETS with test operator interaction			
Description	Headless configuration support is targeted at unattended, semi-attended (Example: Shared by multiple users), or unassigned systems that require KVM support even, when the system has no display device connected (either temporarily or permanently).			
Objective	Verify that KVM redirection works properly on a system with no physical display attached.			
Setup	<p>The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode. Before running this test, ensure that KVM Redirection is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.</p> <p>Important: VBIOS (Video BIOS) and Intel® Graphics drivers supporting KVM redirection on headless configurations must also be integrated/installed on the SUT. Refer to following steps for prepare BIOS image.</p> <ol style="list-style-type: none"> <li>1. Use the latest Intel® BMP tool to open VBIOS.</li> <li>2. Modify the setting "KVM Session/Fake DVI Display Support" to ENABLE.</li> <li>3. Build new BIOS to include the modified VBIOS.</li> </ol>			
<div>Procedure</div> <div>S5→S0 Flow</div>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>2. Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), if the WLAN network interface is used.</li> <li>3. Ensure the Host OS Wake on Wireless LAN is <b>disabled</b>.</li> <li>4. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>5. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>6. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>7. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>8. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> <li>9. Request the test operator to disconnect all display devices from the SUT. The remaining steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</li> <li>10. Inform the test operator that the SUT will soon be powered down and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:           <ol style="list-style-type: none"> <li>a. Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during boot.</li> <li>b. Verify that the BIOS boot screen (if any) is also visible via the VNC viewer.</li> <li>c. Try using the keyboard and mouse to control the Host OS.</li> </ol> </li> <li>11. Gracefully shutdown to S5/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</li> <li>12. Verify that Intel® AMT is available via WLAN by requesting its version, if the WLAN network interface is used.</li> <li>13. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>14. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>15. Request the test operator to:           <ol style="list-style-type: none"> <li>a. Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>b. Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol> </li> </ol>			



ID	AMT_059
<b>Procedure (continued)</b> <b>S4→S0 Flow</b>	<p>16. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>17. Close any VNC Viewer window, which may still be open.</p> <p>18. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface, if the WLAN network interface is used.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>The remaining steps within this block shall be executed, as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p>19. Inform the test operator that the SUT will soon be sent into hibernation state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to:</p> <ol style="list-style-type: none"> <li>Verify that the Ctrl+P (or equivalent keystroke) Intel® MEBX prompt does not appear on the SUT screen during resume from hibernation.</li> <li>Verify that the BIOS boot screen (if any) is also visible via the VNC viewer.</li> <li>Try using the keyboard and mouse to control the Host OS.</li> </ol> <p>20. Hibernate to S4/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>21. Verify that Intel® AMT is available via WLAN by requesting its version, if the WLAN network interface is used.</p> <p>22. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</p> <p>23. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>24. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol>
<b>Procedure (continued)</b> <b>S3→S0 Flow</b>	<p>25. Close any open KVM Redirection session with the SUT via Intel® AMT.</p> <p>26. Close any VNC Viewer window, which may still be open.</p> <p>27. Attempt to bring the SUT to a base state via the following:</p> <ol style="list-style-type: none"> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via the <b>WLAN</b> network interface, if the WLAN network interface is used.</li> </ol> <p>If any of base state verification steps above fail, perform the following as an attempt to recover the SUT before attempting the base state verification steps above one last time.</p> <ol style="list-style-type: none"> <li>Bring the system to G3 and wait 10 seconds.</li> <li>Set system power configuration to AC/DC and wait another 10 seconds.</li> <li>Briefly press the Power Button on the SUT.</li> </ol> <p>The remaining steps within this block shall be executed as if they are part of an independent sub-test. If a failure occurs at any point during the flow below, the remainder of the steps related to the sub-test, may be skipped.</p> <p><b>NOTE:</b> In the case the SUT is operating in Modern Standby or Microsoft* Windows InstantGo* mode, the test shall automatically end here, and the results thus far reported to the test operator as the final test results.</p> <p>28. Inform the test operator that the SUT will soon be sent into suspend state and the VNC Viewer window will open. When the VNC Viewer window opens and the SUT starts to boot, request the test operator to try using the keyboard and mouse to control the Host OS.</p> <p>29. Record the Host OS last boot time on the SUT (to verify successful suspend/resume).</p> <p>30. Suspend to S3/MeOn the SUT via the Host OS and then wait <b>10 seconds</b>.</p> <p>31. Verify that Intel® AMT is available via WLAN by requesting its version, if the WLAN network interface is used.</p> <p>32. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</p> <p>33. Perform a Remote Power-Up of the SUT via Intel® AMT.</p> <p>34. Wait until system resumes back to the Host OS.</p> <p>35. Verify the Host OS last boot time on the SUT <b>does</b> match the boot time recorded before the suspend.</p> <p>36. Request the test operator to:</p> <ol style="list-style-type: none"> <li>Confirm that the redirected screen from the SUT appears in the VNC Viewer.</li> <li>Confirm that the keyboard and mouse can control the Host OS via the management console via the VNC Viewer.</li> </ol>



ID	AMT_059
<b>Procedure</b> (continued)	37. Close any open KVM Redirection session with the SUT via Intel® AMT. 38. Close any VNC Viewer window which may still be open. 39. Request the test operator to re-connect any display devices to the SUT which had been disconnected earlier in the test.
<b>Pass Criteria</b>	The test passes, if all attempted KVM Redirection sessions are viewed via VNC Viewer on the management console, and keyboard/mouse functionality is redirected to the Host OS on the SUT. During system boot or resume, the Intel® MEBX hot-key (Ctrl+P or other keystroke) prompt is not displayed on the SUT.
<b>References</b>	For details on KVM Redirection, refer to the <i>Intel® ME BIOS Specification</i> . For details on Firmware KVM Screen Blanking configuration, refer to the <i>Intel® ME Firmware Bring Up Guide</i> .

## 10.9 Remote Access (Fast Call for Help)

The section serves as a checklist for the environment setup and covers integration testing of the Remote Access (Fast Call for Help) feature in Intel® AMT.

### 10.9.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with a DHCP assigned address configured. Static IP address configurations are not supported by the Environment Detection feature used in this section. The management console may be a laptop or a desktop with a version of Microsoft\* Windows supported by Intel® PETS, and the SUT should have a version of Microsoft\* Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables.

#### Tools for testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.

Where applicable, the wireless LAN interface on Intel® AMT must be on a different network/subnet than the wired LAN interface. For details on how to enter the network interface details into Intel® PETS, consult the Intel® PETS User Guide.

If the firmware image or the SUT configuration does not support some features, Intel® PETS will show those features as failing, when tested. Intel® PETS cannot determine in all cases, which features have been deactivated and should thus be skipped during testing.

#### 10.9.1.1 Environment Setup for Testing End-to-End Connectivity

For those wishing to run end-to-end test utilizing a Management Presence Server (MPS) via tests **following** AMT\_060, follow the instructions below in this section. Otherwise, continue with AMT\_060, where applicable; there is no need for additional test environment configuration.

##### 10.9.1.1.1 Device Roles

- System Under Test (SUT):
  - a. Initially participates on the Enterprise Network for configuration.

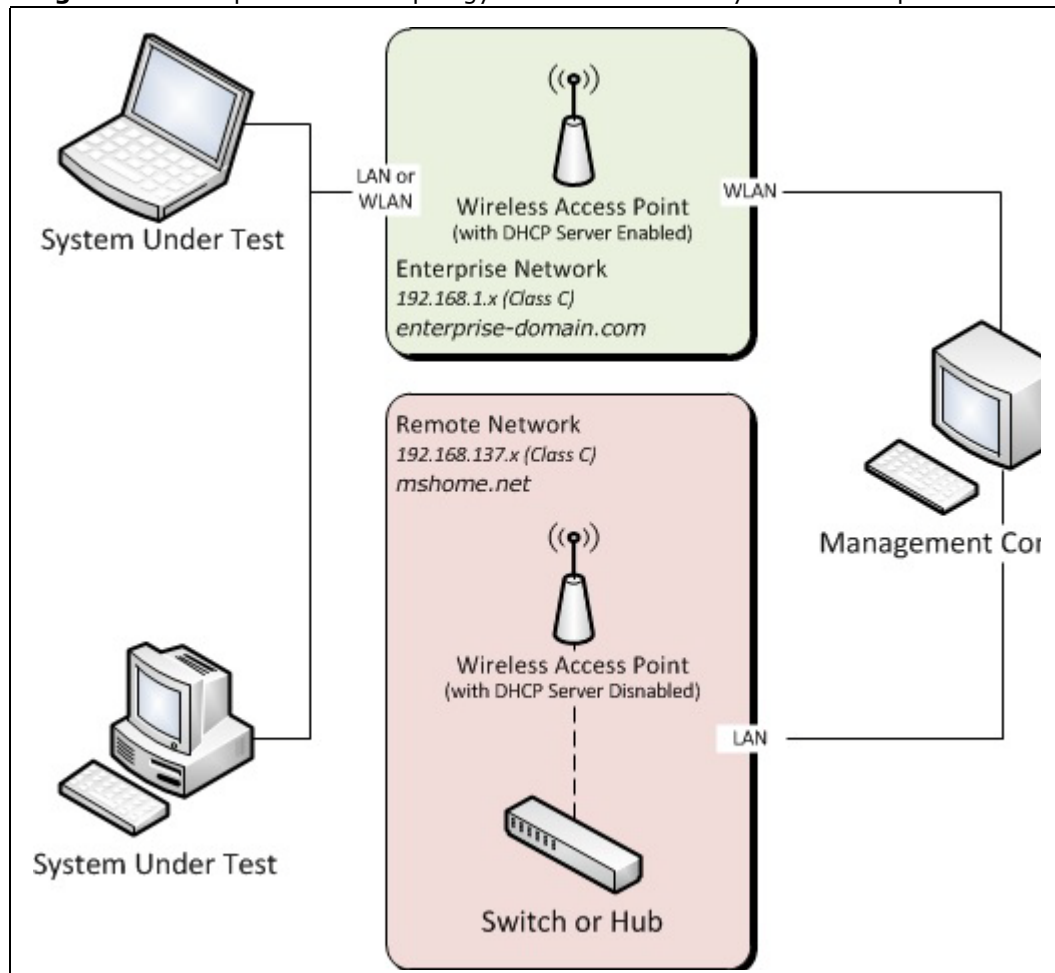


- b. Later is moved to the Remote Network for CIRA testing.
- Management Console:
  - a. Exists on the Enterprise Network (by means of a Wi-Fi connection) and configures the SUT.
  - b. Provides DHCP services for the Remote Network through Microsoft\* Windows Internet Connection Sharing (by means of a LAN connection).
  - c. Contains an MPS, a secure tunnel to communicate with the MPS through the Remote Network, and a HTTP Proxy to enable Web-based communication from the management console back to the SUT.
- Wireless Access Point (AP) for Enterprise Network:
  - a. Provides DHCP services to the Enterprise Network by means of wireless (to management console) and Intel wired/wireless ports (to SUT, when connected).
- Switch or Hub, and/or Wireless AP for Remote Network:
  - a. Exists on the Remote Network and provides a connection point for the SUT.
  - b. Provides continuous electrical signaling to the management console LAN PHY to enable Microsoft\* Windows Internet Connection Sharing configuration.

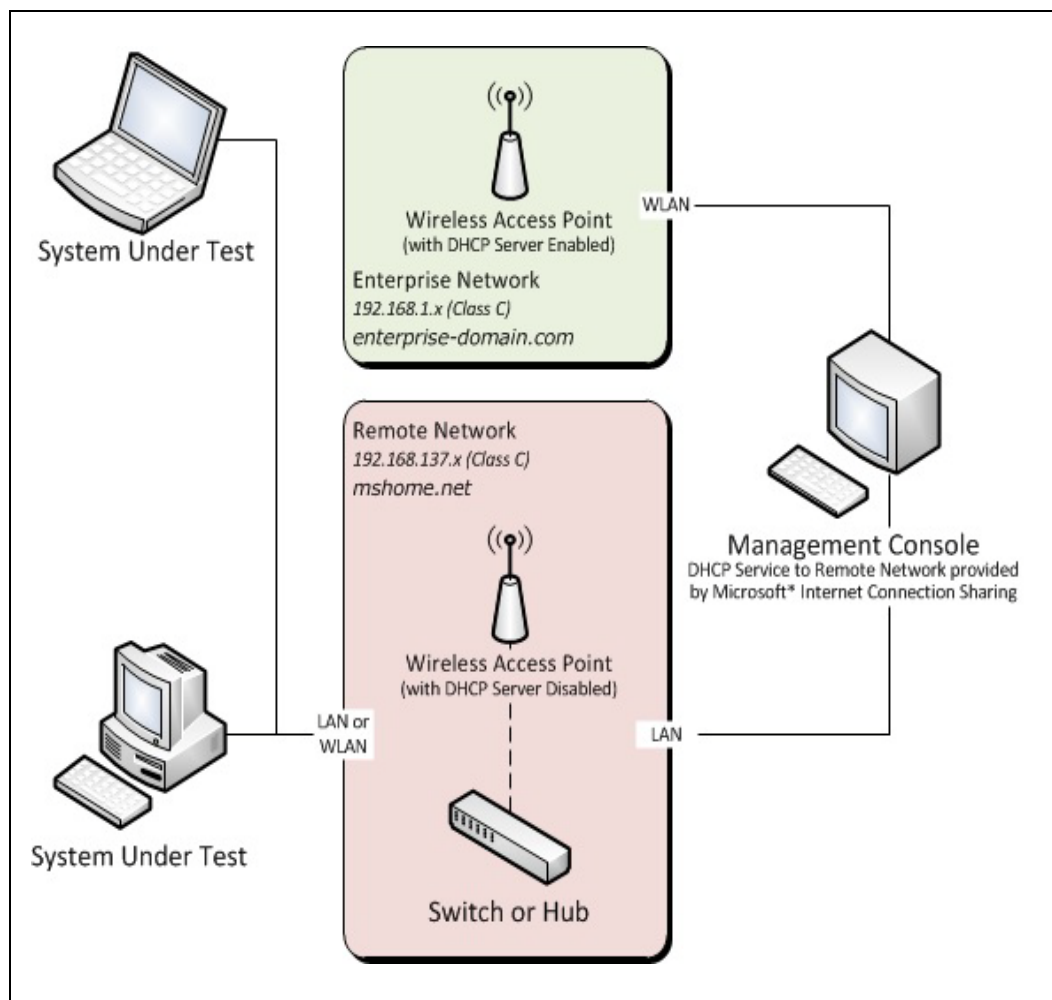
#### 10.9.1.1.2 Network Topology

- Enterprise Network (Refer to diagram #1)
  - a. **Address Range:** 192.168.1.x (Class C)
  - b. **Domain Name:** *enterprise-domain.com*
  - c. **DHCP Server:** Wireless AP
- Remote Network (Refer to diagram #2)
  - a. **Address Range:** 192.168.137.x (Class C)
  - b. **Domain Name:** *mshome.net*
  - c. **DHCP Server:** Microsoft\* Windows\* Internet Connection Sharing service running on the management console

**Diagram 1:** Example Network Topology for SUT Connectivity to the Enterprise Network



**Diagram 2:** Example Network Topology for SUT Connectivity to the Remote Network



**Note:** For the Remote Network configuration, a single Switch or Hub may be sufficient, if the tests are run using the Intel LAN network interface on the SUT; without the need for a Wireless AP. If the SUT is a WLAN-only configuration, then a Wireless AP will be required (and any available built-in DHCP server disabled).

#### 10.9.1.1.3 System Under Test Prerequisite

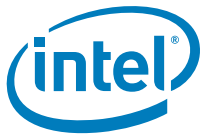
The System Under Test must be able to support TLS, although Intel® ME does not need to be configured to use TLS. Without TLS support, the SUT will not be able to communicate back through the stunnel to the MPS. Some boards may require rework to support TLS.

#### 10.9.1.1.4 Management Console Setup

##### **Network Setting Configuration**

Use the following configuration guidance for the Enterprise and Remote Network interface settings on the management console.





**Enterprise Network:** Connect the management console via Wireless LAN static IP to the Enterprise Network. The configuration used throughout [Section 10.9](#) assumes the static IP address of 192.168.1.20 as the IP address for the management console on the Enterprise Network.

**Warning:** Intel® PETS will use the static IP address of 192.168.1.20 by default, when configuring the MPS on the management console, as well as Intel® AMT on the SUT.

**Remote Network:** Connect the management console via Wired LAN to the Remote Network.

#### **Remote Network DHCP Services:**

The following configuration is required, if there is no other device or system available to provide DHCP services to the Remote Network. It may be possible to use other DHCP server configurations with the tests herein, but support for such configurations is out-of-scope of this document.

Visit official Microsoft\* website for instructions on how to configure Microsoft\* Windows Internet Connection Sharing. When using Microsoft\* Windows Internet Connection sharing, make sure to confirm the following:

- In some management console configurations, the DHCP services may not be available or are not enabled by default for the wireless adapter. To verify that the DHCP services are available and configured, open the *Properties* dialog for the wireless adapter, select the *Sharing* tab and click the *Settings* button in the *Internet Connection Sharing* section.
  - If available, verify that both DHCP Server (67) and DHCP Client (68) check boxes in the services list are selected.
  - If the DHCP service ports are not listed, add services for UDP Port 67 (Server) and UDP Port 68 (Client) manually. When entering the Name or IP address for the service, use the IP address of the MPS (Example: 192.168.1.20). For the DHCP service on Port 67, enter 67 for the **External Port** number and **Internal Port** number of the service. Repeat the same process for the DHCP service on Port 68 using the respective port value of 68 for the external and internal ports as well as the same IP address of the MPS.
- The management console wireless network interface should be *shared* from the device driver *Properties*. When this happens, the management console's LAN interface will automatically be set to 192.168.137.1 (ICS default value). The IP address received by the SUT should then be set within the 192.168.137.x subnet range.
- In cases, where the Intel LAN interface on the SUT is used for testing, ensure that the LAN NIC has a valid MAC address. (Example: **not** 88:88:88:88:87:88).
- The SUT's network interface should be operating in DHCP mode to receive an address from the Microsoft\* Windows Internet Connection Sharing service on the management console.

#### **MPS Configuration**

Intel® PETS will install and configure an MPS on the management console for use in testing. The MPS originates from the Intel® AMT SDK, and documentation related to MPS configuration and execution may be found therein.

The MPS certificates are generated before installation by means of External Security Scripts (also released as part of Intel® PETS). The following reference material is used to generate the scripts and may be used to generate certificates, if a domain name other than the default [enterprise-domain.com](#) is to be used during testing.





- a. The *checkes.bat* file in the `C:\<Intel® PETS directory>\Plugins\Me\Configuration\bin\CertGenerator\ExternalSecScripts\` directory is edited to replace all three instances of **intel.com** with **enterprise-domain.com**.
- b. From a DOS shell within the *checkes.bat* is then run.

The script will prompt to create a *Demo Trusted Root CA* and use it to sign client certificates. After entering **Y** and **<Enter>**, the scripts will create the MPS and Trusted Root certificates.

Intel® PETS configures the MPS sample application via the file `C:\<Intel® PETS directory>\Plugins\Me\MPS\conf\mps.config`. For reference, the following is a list of the changes to the Network section of default *mps.config* configuration file:

```
[Network]
AMTListenIP      = 192.168.1.20
AMTListenPort    = 20015
HttpListenIP     = 192.168.1.20
HttpListenPort   = 8080
SocksListenIP    = 192.168.1.20
SocksListenPort  = 4322
SOAPListenIP     = 192.168.1.20
SOAPListenPort   = 7793
```

Intel® PETS will also configure the MPS notification application via the file `C:\<Intel® PETS directory>\Plugins\Me\MPS\conf\NotificationList.config`. For reference, the following is a list of the changes to the of default *Notification List* configuration file:

```
Original:  http://195.168.1.1:9971
Modified:  http://192.168.1.20:9971
```

**Note:** If a different static IP address is used for the management console WLAN network interface, ensure to align the values above to match.

### Third Party Tools

The following table contains the best known configuration of software deployed herein:

Software	Version	Location
Stunnel	5.43	<a href="http://stunnel.mirt.net">http://stunnel.mirt.net</a>
Apache (win32-x86-no_ssl)	2.2.8	<a href="http://archive.apache.org/dist/httpd/binaries/win32">http://archive.apache.org/dist/httpd/binaries/win32</a>

**Note:** For the *stunnel* software, it may be necessary to locate an archived version available from one of the mirror repositories listed in the site above to find the exact version listed in this configuration. When selecting a package to download, use the Intel-compatible version with an Installer (Example: 'stunnel-5.43-win32-installer.exe').

### Apache Proxy Server Installation

Install the Apache web server into the `C:\AMT_06x\` directory on the management console:

- a. During setup, configure the *Server Information* wizard page, as such:
  - i. In the *Network Domain* field enter **enterprise-domain.com**.
  - ii. In the *Server Name* field enter **www.enterprise-domain.com**.
  - iii. In the *Administrator's Email Address* field enter **admin@enterprise-domain.com**.
  - iv. Select the install "only for the Current User, on Port 8080, when started Manually" radio button.



- v. Click *Next* to continue.

**Note:**

If a different domain name for the Enterprise Network is used for the management console WLAN network interface, ensure to align the values above to match.

- b. On the *Setup Type* wizard page, select the **Typical** radio button and click **Next** to continue.
- c. On the *Destination Folder* wizard page, click the **Change** button.
- d. In the *Change Current Destination Folder* dialog:
  - i. In the Folder name: field enter **C:\AMT\_06x\apache\**.
  - ii. Click **OK** to close the dialog.
- e. Click **Next** to continue.
- f. Click **Install** to start the installation.
- g. Click **Finish** to finalize the installation and exit the installer.
- h. Overwrite the following SOCKS5 proxy modules in the Apache installation with those from the MPS sample application directory:  
Source: C:\<Intel® PETS directory>\Plugins\Me\MPS\Apache\  
Destination: C:\AMT\_06x\apache\modules  
File(s): mod\_proxy.so, mod\_proxy\_connect.so

**Note:**

These modules originate from the Intel® AMT SDK. For more information about the supported directives, refer the Intel® AMT SDK for details.

- i. Copy the sample *httpd.conf* configuration file from the C:\<Intel® PETS directory>\Plugins\Me\MPS\Apache\ directory to the C:\AMT\_06x\apache\conf\ directory.

For reference, the following is a list of the changes to the default *httpd.conf* configuration file:

- a. The *ServerName* directive is un-commented and set to:  
ServerName www.enterprise-domain.com:8080

**Note:**

If a different domain name for the Enterprise Network is used for the management console WLAN network interface, ensure to align the value above to match.

- b. The following SOCKS5 proxy modules are enabled by un-commenting them:  
LoadModule proxy\_module modules/mod\_proxy.so  
LoadModule proxy\_connect\_module modules/mod\_proxy\_connect.so  
LoadModule proxy\_http\_module modules/mod\_proxy\_http.so
- c. The following proxy module settings are added to the end of the configuration file:  
AllowCONNECT 433 16992 16993 16994 16995 16996  
ProxyRequests On  
ProxyVia On  
ProxySocks On  
ProxySocksIp 192.168.1.20  
ProxySocksPort 4322  
ProxySocksDnsMode Remote  
ProxySocksAuth Off

**Note:**

If a different static IP address is used for the management console WLAN network interface, ensure to align the value above to match.



### ***Stunnel Installation***

Install the stunnel (TLS tunnel) application on the management console. After setup is complete, copy the sample *stunnel.conf* configuration file from the C:\<Intel® PETS directory>\Plugins\Me\MPS\stunnel\ directory to the C:\Program Files\stunnel\config\ directory.

For reference, the following is a list of the changes to the default *stunnel.conf* configuration file:

- a. Comment out each of the three lines for the pop3s, imaps, and smtp protocols are commented out.
- b. The following lines are added:  
[mps]  
accept = 192.168.1.20:2002  
connect = 192.168.1.20:20015

**Note:** If a different static IP address is used for the management console WLAN network interface, ensure to align the value above to match.

- c. The cert option is set to:  
cert = .\MPS\_cert.pem
- d. The key option is un-commented and set to:  
key = .\MPS\_key.pem
- e. The CAfile option is un-commented and set to:  
CAfile = .\trusted\_cert.pem
- f. The debug = 7 option may be un-commented and set, if more detailed debugging information is desired.

**Note:** Intel® PETS will automatically install the *trusted\_cert.cer* used by the stunnel configuration above into the Windows\* *Trusted Root Certification Authorities\Registry* store on the management console.



## 10.9.2 Fast Call for Help During System Boot

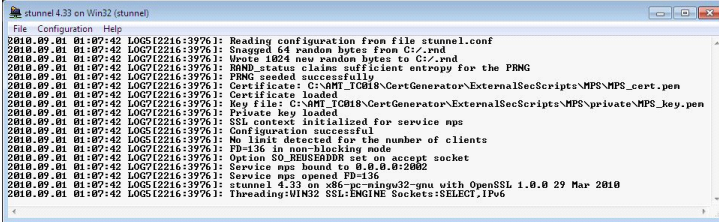
ID	AMT_060			
Title	Fast Call for Help During System Boot			
Requirement	Mandatory - Exempt for systems which do not support Fast Call for Help			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	<p>Fast Call for Help can be established by user from BIOS healing option, from Intel® MEBX or from Hardware button. Pending OEM implementation of Fast Call for Help feature, this test will verify that Fast Call for Help can be initiated by means of the interface implemented by the OEM.</p> <p>This is <b>NOT</b> an end to end test of Fast Call for Help feature. This test will check only that the session request is initiated from BIOS. In order to perform full end to end test, use ISV tools.</p>			
Objective	<p>This test will verify that BIOS is sending the request for Fast Call for Help session initiation once the session is initiated from BIOS/Intel® MEBX or Hardware button.</p> <p><b>NOTE:</b> Fast Call for Help connection is <b>not supposed</b> to succeed in this test. The test only verifies that the system is trying to initiate the connection.</p>			
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
Procedure	<ol style="list-style-type: none"> <li>1. Remove all Remote Access Policies on the SUT via Intel® AMT.</li> <li>2. Verify that the SUT is configured to use DHCP address configuration via Intel® AMT.</li> <li>3. Create a fictitious Management Presence Server (MPS) for the SUT via Intel® AMT, if not already registered.</li> <li>4. Create a user initiated trigger Remote Access Policy with a Tunnel Lifetime of 120 seconds associated to the fictitious MPS in the SUT via Intel® AMT.</li> <li>5. Set the BIOS as an acceptable interface to initiate a Remote Access connection on the SUT via Intel® AMT, if not already configured.</li> <li>6. Set the Environment Detection mechanism on the SUT via Intel® AMT to look for a fictitious network. This forces the SUT to immediately recognize the test network as being outside of the Enterprise.</li> <li>7. Inform the test operator that a system boot will be performed. Request the test operator to press Ctrl+Alt+F1 to initiate the <i>Fast Call for Help</i> process and to view the <i>Fast Call for Help</i> screens display the following.</li> </ol> <p><b>NOTE:</b> System implementations may use a different keyboard sequence to initiate the <i>Fast Call for Help</i> process.</p> <ol style="list-style-type: none"> <li>8. Gracefully restart the SUT via the Host OS.</li> </ol> <p>The next screen may be displayed (on some implementations it may not be visible):  <i>Intel(r) Remote Assistance mechanism is trying to get a network connection.  This may take a couple of minutes...  Press &lt;ESC&gt; to abort...</i></p> <p>The next screen should display the Remote Access connection attempt:  <i>Connecting to &lt;fictional server name&gt;...  Press &lt;ESC&gt; to abort</i></p> <p><b>NOTE:</b> It is expected that the connection attempt will fail.</p> <ol style="list-style-type: none"> <li>9. Request the test operator to confirm that the SUT attempted to connect the fictional MPS, but did not succeed.</li> <li>10. Clear the Environment Detection mechanism in the SUT via Intel® AMT, to clean up.</li> <li>11. Remove all Remote Access Policies on the SUT via Intel® AMT, to clean up.</li> </ol>			
Pass Criteria	The test passes, if the Fast Call For Help connection attempt screen is displayed. This means that the connection was initiated but no MPS was found (as expected).			
References	For details on Remote Access operations, refer to the <i>Intel® ME BIOS Specification</i> .			



### 10.9.3 Fast Call for Help from Outside the Enterprise

ID	AMT_061			
Title	Fast Call for Help from Outside the Enterprise			
Requirement	Optional			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	Fast Call for Help from outside the enterprise can be initiated by user from BIOS healing option, Intel® MEBX or Hardware button as well as OS application, such as Intel® MSS.			
Objective	<p>This test verifies that a Fast Call for Help session from outside the enterprise can be established between Intel® AMT and an MPS. This is <b>not</b> a mandatory test. The mandatory section of Fast Call for Help implementation is tested in AMT_060.</p> <p>This test may run twice, beginning-to-end, on systems with both LAN and WLAN Intel® AMT network interface support. Additionally, there is a Supplemental portion of this test during primary testing at the appropriate time, may run manually by the test operator in addition to the core Procedures outlined in this test.</p>			
Setup	<ol style="list-style-type: none"> <li>1. Request the test operator to confirm that the SUT and management console are operating in a network test environment aligned to what is described in "<a href="#">Environment Setup for Testing End-to-End Connectivity</a>" above, and confirm that the SUT is currently connected to the <i>Enterprise Network</i>.</li> <li>2. Warn the test operator that this test will unprovision the SUT during test setup and upon conclusion. If the test operator does not wish to have the SUT unprovisioned, they may select to abort the test in which case the test status will be reflected as Aborted.</li> <li>3. Bring the SUT to the base state of S0/MeOn.</li> <li>4. Terminate any existing Stunnel and Apache server processes running on the management console (Required to allow PETS to copy Stunnel and Apache server configuration files).</li> <li>5. Configure the MPS and MPS notification applications based on the settings found in "<a href="#">Environment Setup for Testing End-to-End Connectivity</a>" above.</li> <li>6. Verify and configure the Apache web server SOCK5 proxy modules and <code>http.conf</code> configuration based on the settings found in "<a href="#">Environment Setup for Testing End-to-End Connectivity</a>" above.</li> <li>7. Verify and configure the stunnel (TLS tunnel) certificates, keys, and configuration file based on the settings found in "<a href="#">Environment Setup for Testing End-to-End Connectivity</a>" above.</li> <li>8. If the SUT is in an <i>In-Provisioning</i> or <i>Post-Provisioning</i> state, fully unprovision the SUT and return it to a <i>Pre-Provisioning</i> state. This is intended to return the Intel® AMT configuration state to a clean baseline for testing.</li> <li>9. Verify the SUT is in <i>Pre-Provisioning</i> state.</li> <li>10. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>11. Prompt the test operator to provision the SUT via Intel® MEBX in order to proceed with testing.</li> </ol>			



ID	AMT_061
Procedure	<p>12. Run the stunnel service on the management console.</p> <p>13. Verify that there were no problems loading the MPS certificate and private key.</p>  <p>14. Prompt the test operator that the MPS sample application on the management console will be started and that Intel® PETS will stop the MPS sample application at the end of the test. Also indicate that, if the test operator experiences any issue with the application not closing automatically, then the MPS sample application may be closed by using Microsoft® Windows Task Manager to find and terminate the process. Control+C interrupts are <b>not</b> processed by the application.</p> <p>15. Start the MPS sample application on the management console.</p> <p><b>NOTE:</b> If the MPS application exits soon after startup, verify the network configuration of the management console again.</p> <p>16. Prompt the test operator that the MPS notification application on the management console will be started and that Intel® PETS will stop the MPS Notification application at the end of the test. If the test operator experiences any issue with the application not closing automatically, the MPS Notification application may be closed by pressing <i>Control+C</i>.</p> <p>17. Start the MPS notification application on the management console.</p> <p>18. Run the Apache server.</p>
	<p>19. Ensure that the SUT is configured to use DHCP address configuration via Intel® AMT.</p> <p>20. Ensure that Dynamic DNS update is disabled on the SUT via Intel® AMT.</p> <p>21. Ensure that the following fictitious network name is set in the SUT via Intel® AMT: FQDN: <b>sut.enterprise-domain.com</b></p> <p>22. Register a fictitious <i>external</i> MPS with the SUT via Intel® AMT based on the following settings: Server IP: <b>192.168.1.20</b> Port: <b>2002</b> Authentication Method <i>Username/Password Authentication</i> User: <b>admin</b> Password: <b>StrongPW123!</b> Certificate: <i>Created and installed by Intel® PETS</i> Common Name (CN): <b>mps.enterprise-domain.com</b> The Server IP and Common Name may change based on the management console's assigned <i>Enterprise Network</i> IP address and domain name.</p> <p>23. Create a user initiated trigger Remote Access Policy with a Tunnel Lifetime of 600 seconds associated to the fictitious MPS in the SUT via Intel® AMT.</p> <p>24. Set both the OS and BIOS acceptable interfaces from which to initiate a Remote Access connection on the SUT via Intel® AMT.</p> <p>25. Set the Environment Detection mechanism on the SUT via Intel® AMT to look for a fictitious network based on the following setting(s): Home Domain: <b>enterprise-domain.com</b> This forces the SUT to immediately recognize the test network as being outside of the enterprise, when connected to the <i>Remote Network</i> and inside the enterprise, when connected to the <i>Enterprise Network</i>.</p>



ID	AMT_061
<b>Procedure</b> (continued)	<p>26. Prompt the test operator to move the SUT network connection to the <i>Remote Network</i>. This may involve either physically moving the LAN cable on the SUT to change networks (LAN-only designs) or disconnecting from one Wireless Access Point and connecting to another (WLAN-only designs), or a combination both over a series of test executions each focusing on one of the two available LAN and WLAN network interfaces (LAN+WLAN designs).</p> <p>27. Wait for <b>1 minute</b>, while Intel® AMT Environment Detection is applied.</p> <p>28. Prompt the test operator to input the IP address of the SUT on the <i>Remote Network</i>. This will be used for the remainder of Intel® PETS' communications between the management consoles and the Intel® PETS Local Agent on the SUT.</p> <p>29. Using the SUT's <i>Remote Network</i> IP address, via Intel® PETS Local Agent on the SUT:</p> <ol style="list-style-type: none"> <li>Verify that the all available Intel® ME network IPv4 network interfaces have an IP address of <b>0.0.0.0</b>. This indicates that the Environment Detection feature of Intel® AMT has determined that the SUT is operating outside of the <i>Enterprise Network</i> and has configured the Intel® ME network interface to allow only communications through a TLS tunnel.</li> <li>Open a remote access User Initiated connection. This process may take up to 2 minutes.</li> <li>Verify the remote access connection status as <i>Connected</i>. If the SUT cannot connect through to the MPS and generate a notification to the MPS notification application: <ul style="list-style-type: none"> <li>Check the stunnel error log. There may an error indicating that a certificate has expired.</li> <li>If the Microsoft* Windows Firewall is running on the management console, it may also be necessary to open port 16993. Refer the documentation for the version of Microsoft* Windows on the management console for more details.</li> </ul> </li> <li>Inform the test operator that they may manually execute the Supplemental test steps listed in this test below to check Intel® ME WebUI access via Web Browser.</li> <li>Perform and log a WS-MAN request for the Intel® AMT version on the SUT via the Web proxy on the management console using the FQDN of the SUT (Example: <i>sut.enterprise-domain.com</i>) with the following proxy settings: <ul style="list-style-type: none"> <li>Proxy Address <b>192.168.1.20</b></li> <li>Proxy Port <b>8080</b></li> </ul> </li> <li>Close the remote access connection.</li> </ol> <p>30. Shut down the Apache server.</p> <p>31. Stop the MPS notification application.</p> <p>32. Stop the MPS sample application.</p> <p>33. Shut down the stunnel service on the management console</p> <p>34. Prompt the test operator to move the SUT back to the <i>Enterprise Network</i>.</p> <p>35. Prompt the user to input the IP address of the SUT on the enterprise network to allow PETS to communicate with the SUT.</p> <p>36. Clear the Environment Detection mechanism in the SUT via Intel® AMT, to clean up.</p> <p>37. Remove all Remote Access Policies on the SUT via Intel® AMT, to clean up.</p>
<b>Supplemental</b>	<p>A. In the Web Browser on the management console, visit official Microsoft* website for how to configure Microsoft* Internet Explorer's Proxy Settings. For Mozilla Firefox, refer to the instructions contained here: <a href="http://support.mozilla.com/en-US/kb/Options+window+-+Advanced+panel#Connection_Settings_Dialog">http://support.mozilla.com/en-US/kb/Options+window+-+Advanced+panel#Connection_Settings_Dialog</a></p> <ol style="list-style-type: none"> <li>Set the Address of the Proxy server to <b>192.168.1.20</b>.</li> <li>Set the Port of the Proxy server to <b>8080</b>.</li> <li>Apply the settings above for all protocols. (for example, HTTP, Secure, FTP, Socks)</li> </ol> <p>B. In the Web Browser on the management console connect to the SUT using its FQDN. (Example: <a href="http://sut.enterprise-domain.com:16992">http://sut.enterprise-domain.com:16992</a>) This step must be completed before the connection timeout expires and the SUT disconnects from the MPS.</p> <ul style="list-style-type: none"> <li>If connection occurs in the Web Browser on the management console and a login page from the SUT resembling that the Intel® CSME WebUI appears, the end-to-end configuration of Fast Call for Help support has been confirmed.</li> </ul> <p>C. In the Web Browser on the management console, reset the Proxy Settings back to their previous configuration before step A.</p>
<b>Pass Criteria</b>	<p>The test passes, if the Fast Call for Help connection was triggered, and Fast Call for Help session was established between the SUT and the MPS on a <i>Remote Network</i> configuration, and the SUT could be contacted by the management console via WS-MAN request.</p>

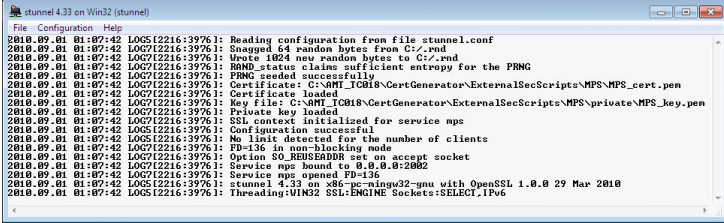


## 10.9.4 Fast Call for Help from Inside the Enterprise

ID	AMT_062			
Title	Fast Call for Help from Inside the Enterprise			
Requirement	Optional			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	Fast Call for Help from inside the enterprise can be initiated by user from BIOS healing option, Intel® MEBX or Hardware button as well as OS application, such as Intel® MSS.			
Objective	<p>This test will verify that a Fast Call for Help session from inside the enterprise can be established between Intel® AMT and an MPS. This is <b>not</b> a mandatory test. The mandatory section of Fast Call for Help implementation is tested in AMT_060.</p> <p>This test may be run twice, beginning-to-end, on systems with both LAN and WLAN Intel® AMT network interface support. Additionally, there is a Supplemental portion of this test which, during primary testing at the appropriate time, may be run manually by the test operator in addition to the core Procedures outlined in this test.</p>			
Setup	<ol style="list-style-type: none"> <li>1. Request the test operator to confirm that the SUT and management console are operating in a network test environment aligned to what is described in "Environment Setup for Testing End-to-End Connectivity" above, and confirm that the SUT is currently connected to the Enterprise Network.</li> <li>2. Warn the test operator that this test will unprovision the SUT during test setup and upon conclusion. If the test operator does not wish to have the SUT unprovisioned, they may select to abort the test in which case the test status will be reflected as Aborted.</li> <li>3. Bring the SUT to the base state of S0/MeOn.</li> <li>4. Terminate any existing Stunnel and Apache server processes running on the management console. (Required to allow PETS to copy Stunnel and Apache server configuration files)</li> <li>5. Configure the MPS and MPS notification applications based on the settings found in "Environment Setup for Testing End-to-End Connectivity" above.</li> <li>6. Verify and configure the Apache web server SOCK5 proxy modules and http.conf configuration based on the settings found in "Environment Setup for Testing End-to-End Connectivity" above.</li> <li>7. Verify and configure the stunnel (TLS tunnel) certificates, keys, and configuration file based on the settings found in "Environment Setup for Testing End-to-End Connectivity" above.</li> <li>8. If the SUT is in an <i>In-Provisioning</i> or <i>Post-Provisioning</i> state, fully unprovision the SUT and return it to a <i>Pre-Provisioning</i> state. This is intended to return the Intel® AMT configuration state to a clean baseline for testing.</li> <li>9. Verify the SUT is in <i>Pre-Provisioning</i> state.</li> <li>10. Shutdown the SUT, and confirm that Intel® ME is in the MeOff state.</li> <li>11. Prompt the test operator to provision the SUT via Intel® MEBX in order to proceed with testing.</li> </ol>			





ID	AMT_062
	<p>12. Run the stunnel service on the management console.</p> <p>13. Verify that there were no problems loading the MPS certificate and private key.</p>  <p>14. Prompt the test operator that the MPS sample application on the management console will be started and that Intel® PETS will stop the MPS sample application at the end of the test. Also indicate that if the test operator experiences any issue with the application not closing automatically, the MPS sample application may be closed by using Microsoft® Windows Task Manager to find and terminate the process. Control+C interrupts are <b>not</b> processed by the application.</p> <p>15. Start the MPS sample application on the management console. If the MPS application exits soon after startup, verify the network configuration of the management console again.</p> <p>16. Prompt the test operator that the MPS notification application on the management console will be started and that Intel® PETS will stop the MPS Notification application at the end of the test. If the test operator experiences any issue with the application not closing automatically, the MPS Notification application may be closed by pressing <i>Control+C</i>.</p> <p>17. Start the MPS notification application on the management console.</p> <p>18. Run the Apache server.</p>
Procedure	<p>19. Ensure that the SUT is configured to use DHCP address configuration via Intel® AMT.</p> <p>20. Ensure that Dynamic DNS update is disabled on the SUT via Intel® AMT.</p> <p>21. Ensure that the following fictitious network name is set in the SUT via Intel® AMT: FQDN: <b>sut.enterprise-domain.com</b></p> <p>22. Register a fictitious <i>internal</i> MPS with the SUT via Intel® AMT based on the following settings: Server IP: <b>192.168.1.20</b> Port: <b>2002</b> Authentication Method <i>Username/Password Authentication</i> User: <b>admin</b> Password: <b>StrongPW123!</b> Certificate: <i>Created and installed by Intel® PETS</i> Common Name (CN): <b>mps.enterprise-domain.com</b> The Server IP and Common Name may change based on the management console's assigned <i>Enterprise Network</i> IP address and domain name.</p> <p>23. Create a user initiated trigger Remote Access Policy with a Tunnel Lifetime of 600 seconds associated to the fictitious MPS in the SUT via Intel® AMT.</p> <p>24. Set both the OS and BIOS acceptable interfaces from which to initiate a Remote Access connection on the SUT via Intel® AMT.</p> <p>25. Set the Environment Detection mechanism on the SUT via Intel® AMT to look for a fictitious network based on the following setting(s): Home Domain: <b>enterprise-domain.com</b> This forces the SUT to immediately recognize the test network as being outside of the enterprise when connected to the <i>Remote Network</i> and inside the enterprise, when connected to the <i>Enterprise Network</i>.</p> <p>26. Wait for <b>1 minute</b> while Intel® AMT Environment Detection is applied.</p>



ID	AMT_062
Procedure (continued)	<p>27. Using the SUT's <i>Enterprise Network</i> IP address, via Intel® PETS Local Agent on the SUT:</p> <ol style="list-style-type: none"><li>Open a remote access User Initiated connection. This process may take up to 2 minutes.</li><li>Verify the remote access connection status as <i>Connected</i>. If the SUT cannot connect through to the MPS and generate a notification to the MPS notification application:<ul style="list-style-type: none"><li>Check the tunnel error log. There may an error indicating that a certificate has expired.</li><li>If the Microsoft* Windows Firewall is running on the management console, it may also be necessary to open port 16993. Refer the documentation for the version of Microsoft* Windows on the management console for more details.</li></ul></li><li>Inform the test operator that they may manually execute the Supplemental test steps listed in this test below to check Intel® ME WebUI access via Web Browser.</li><li>Perform and log a WS-MAN request for the Intel® AMT version on the SUT via the Web proxy on the management console using the FQDN of the SUT (Example: <i>sut.enterprise-domain.com</i>) with the following proxy settings:<ul style="list-style-type: none"><li>Proxy Address <b>192.168.1.20</b></li><li>Proxy Port <b>8080</b></li></ul></li><li>Close the remote access connection.</li></ol> <p>28. Shut down the Apache server. 29. Stop the MPS notification application. 30. Stop the MPS sample application. 31. Shut down the tunnel service on the management console. 32. Clear the Environment Detection mechanism in the SUT via Intel® AMT, to clean up. 33. Remove all Remote Access Policies on the SUT via Intel® AMT, to clean up.</p>
Supplemental	<p>A. In the Web Browser on the management console, visit official Microsoft* website for how to configure Microsoft* Internet Explorer's Proxy Settings.  For Mozilla Firefox, refer to the instructions contained here: <a href="http://support.mozilla.com/en-US/kb/Options+window+-+Advanced+panel#Connection_Settings_Dialog">http://support.mozilla.com/en-US/kb/Options+window+-+Advanced+panel#Connection_Settings_Dialog</a></p> <ol style="list-style-type: none"><li>Set the <i>Address</i> of the <i>Proxy server</i> to <b>192.168.1.20</b>.</li><li>Set the <i>Port</i> of the <i>Proxy server</i> to <b>8080</b>.</li><li>Apply the settings above for all protocols. (Example: HTTP, Secure, FTP, Socks)</li></ol> <p>B. In the Web Browser on the management console connect to the SUT using its FQDN. (Example: <a href="http://sut.enterprise-domain.com:16992">http://sut.enterprise-domain.com:16992</a>) This step must be completed before the connection timeout expires and the SUT disconnects from the MPS.<ul style="list-style-type: none"><li>If connection occurs in the Web Browser on the management console and a login page from the SUT resembling that of the Intel® CSME WebUI appears, the end-to-end configuration of Fast Call for Help support has been confirmed.</li></ul></p> <p>C. In the Web Browser on the management console, reset the Proxy Settings back to their previous configuration before step A.</p>
Pass Criteria	<p>The test passes, if the Fast Call for Help connection was triggered, and Fast Call for Help session was established between the SUT and the MPS on an <i>Enterprise Network</i> configuration, and the SUT could be contacted by the management console via WS-MAN request.</p>

## 10.10 Settings, Storage, and Security Configuration

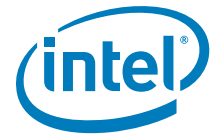
The section serves as a checklist for the environment setup and covers testing of the Settings, Storage, and Security Configuration features in Intel® AMT.

### 10.10.1 Test Environment

The System Under Test (SUT) is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows supported by Intel® PETS, and the SUT should have a version of Microsoft\* Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables.

#### Tools for testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.



- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.

Where applicable, the wireless LAN interface on Intel® AMT must be on a different network/subnet than the wired LAN interface. For details on how to enter the network interface details into Intel® PETS, consult the Intel® PETS User Guide.

If the firmware image or the SUT configuration does not support some features, Intel® PETS will show those features as failing, when tested. Intel® PETS cannot determine in all cases, which features have been deactivated and should thus be skipped during testing.



### 10.10.2 General Settings Information

ID	AMT_070				
Title	General Settings Information				
Requirement	Optional				
System	<div><div>Form Factor</div><div><input checked="" type="checkbox"/> Desktop   <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile</div></div>	<div><div>System Power Model</div><div><input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*</div></div>	<div><div>Intel® AMT Network Interface</div><div><input checked="" type="checkbox"/> LAN   <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN   <input type="checkbox"/> Not Used</div></div>	<div><div>LAN Type</div><div><input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN</div></div>	
Method	Automated by Intel® PETS				
Description	The Intel® AMT interface supports access to general settings information about the system.				
Objective	This test will use the Intel® AMT interface to extract the general settings information about the system and present it to the test operator.				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.				
Procedure	<div>1. Retrieve and display to the test operator general settings information, including:</div> <ul style="list-style-type: none"><li>• Configuration State</li><li>• Security Parameters<ul style="list-style-type: none"><li>— Administrator Control Mode (ACM) or Client Control Mode (CCM)</li><li>— Transport Layer Security (TLS) (enabled/disabled)</li><li>— Hardware Cryptography (enabled/disabled)</li><li>— Network Interface (enabled/disabled)</li></ul></li><li>• System BIOS Version Information</li><li>• Intel® ME Firmware Version Information</li><li>• Network Feature States<ul style="list-style-type: none"><li>— Web UI (enabled/disabled)</li><li>— Storage Redirection (enabled/disabled)</li><li>— Serial-Over-LAN (SOL) (enabled/disabled)</li><li>— Keyboard, Video and Mouse (KVM) (enabled/disabled)</li><li>— Redirection Ports (enabled/disabled)</li></ul></li><li>• Network Interface States<ul style="list-style-type: none"><li>— LAN IPv4 and IPv6 (when available)</li><li>— Wireless LAN IPv4 and IPv6 (when available)</li></ul></li><li>• IEEE 802.1x Profile Configuration</li></ul>				
Pass Criteria	The test passes, if the information is collected and displayed to the test operator.				

### 10.10.3 Security Administration Realm Interface

ID	AMT_071				
Title	Security Administration Realm Interface				
Requirement	Optional				
System	Form Factor	System Power Model	Intel® AMT Network Interface		LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input checked="" type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input type="checkbox"/> Either Used <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS				
Description	The Intel® AMT interface supports access to various functions via the Security Administration realm (ADMIN_SECURITY_ADMINISTRATION_REALM).				
Objective	This test will use the Intel® AMT interface with access rights within the Security Administration realm to toggle the active Intel® AMT Power Package.				
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.				



ID	AMT_071
<b>Procedure</b>	<ol style="list-style-type: none"> <li>With credentials in the Security Administration realm, use the Intel® AMT interface to: <ol style="list-style-type: none"> <li>Get the active power package.</li> <li>Set the power package to the opposite value (Example: If Power Package 1, select Power Package 2, or vice versa).</li> <li>Set the active power package back to the original value before the test started.</li> </ol> </li> </ol>
<b>Pass Criteria</b>	The test passes, if the active power package can be toggled using the Security Administration realm.

## 10.10.4 Transport Layer Security (TLS) Authentication

ID	AMT_073			
<b>Title</b>	Transport Layer Security (TLS) Authentication			
<b>Requirement</b>	Optional			
<b>System</b>	<b>Form Factor</b>	<b>System Power Model</b>	<b>Intel® AMT Network Interface</b>	<b>LAN Type</b>
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction			
<b>Description</b>	The Intel® AMT interface supports access to the system via Transport Layer Security (TLS) authentication.			
<b>Objective</b>	This test will configure the Intel® AMT to enable TLS authentication and then retrieve the Intel® AMT core version via the secured interface.			
<b>Setup</b>	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Configure the SUT to enable TLS (server side authentication) via Intel® AMT.</li> <li>Install a certificate on the SUT allowing TLS Server side connection.</li> <li>Connect to the SUT with a TLS connection, and request the Intel® AMT core version.</li> <li>Verify that the SUT responded over the TLS connection.</li> <li>Configure the SUT to disable TLS.</li> </ol>			
<b>Pass Criteria</b>	The test passes, if the Intel® AMT core version is collected via TLS connection.			



## 10.10.5 Wake By Means of an Alarm Clock

### 10.10.5.1 Alarm Wake from S5

ID	AMT_074
Title	Alarm Wake from S5
Requirement	Optional
Method	Automated by Intel® PETS
Form Factor	Desktop/Mobile
Description	Original Power State: S0/CM0; Power Policy - PP2, ACDC;
Objective	This test checks that the system wakes up by means of Alarm Clock from S5/M3 state.
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3.</li><li>2. Set the power source to AC + DC.</li><li>3. Boot the system to S0/CM0 and make sure OS is up.</li><li>4. Verify that Intel® CSME is on. This can be done by either checking SLP_A# signal, that should be de-asserted or running Intel® MEinfo tool indicating Intel® CSME is on.</li><li>5. Synchronize the Intel® CSME time with Universal Time Clock (UTC).</li><li>6. Set an alarm to another 5 minutes from now.</li><li>7. Move platform to S5.</li><li>8. Delay 6 minutes.</li><li>9. Verify platform is in S0.</li><li>10. Check HostBootReason (to confirm wake was caused by alarm).</li><li>11. Move to S5.</li><li>12. Delay 5 min.</li><li>13. Verify platform is in S0.</li><li>14. Check HostBootReason (to confirm wake was caused by alarm).</li><li>15. Delete alarm.</li></ol>
Test Pass/Fail Criteria	Host wakes up both times

### 10.10.5.2 Alarm Wake from S4

ID	AMT_075
Title	Alarm Wake from S4
Requirement	Optional
Method	Automated by Intel® PETS
Form Factor	Desktop/Mobile
Description	Original Power State: S0/CM0; Power Policy - PP2, ACDC;
Objective	This test checks that the system wakes up by means of Alarm Clock from S4/M3 state.



ID	AMT_075
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.
Procedure	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3.</li> <li>2. Set the power source to AC + DC.</li> <li>3. Boot the system to S0/CM0 and make sure OS is up.</li> <li>4. Verify that Intel® CSME is on. This can be done by either checking SLP_A# signal, that should be de-asserted or running Intel® MEinfo tool indicating Intel® CSME is on.</li> <li>5. Synchronize the Intel® CSME time with Universal Time Clock (UTC).</li> <li>6. Set an alarm to another 5 minutes from now.</li> <li>7. Move platform to S4.</li> <li>8. Delay 6 minutes.</li> <li>9. Verify platform is in S0.</li> <li>10. Check HostBootReason (to confirm wake was caused by alarm).</li> <li>11. Move to S4.</li> <li>12. Delay 5 minutes.</li> <li>13. Verify platform is in S0.</li> <li>14. Check HostBootReason (to confirm wake was caused by alarm).</li> <li>15. Delete alarm.</li> </ol>
Test Pass/ Fail Criteria	Host wakes up both times.



### 10.10.5.3 Alarm Wake from S3

ID	AMT_076
Title	Alarm Wake from S3
Requirement	Optional
Method	Automated by Intel® PETS
Form Factor	Desktop/Mobile
Description	Original Power State: S0/CM0; Power Policy - PP2, ACDC;
Objective	This test checks that the system wakes up by means of Alarm Clock from S3/M3 state.
Setup	The initial state of the SUT should be S0/MeOn with Host OS running. Intel® AMT should be provisioned via manual mode.
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. Set the power source to AC + DC</li><li>3. Boot the system to S0/CM0 and make sure OS is up</li><li>4. Verify that Intel® CSME is on. This can be done by either checking SLP_A# signal, that should be de-asserted or running Intel® MEInfo tool indicating Intel® CSME is on.</li><li>5. Synchronize the Intel® CSME time with Universal Time Clock (UTC).</li><li>6. Set an alarm to another 5 minutes from now.</li><li>7. Move platform to S3.</li><li>8. Delay 6 minutes.</li><li>9. Verify platform is in S0.</li><li>10. Check HostBootReason (to confirm wake was caused by alarm).</li><li>11. Move to S3.</li><li>12. Delay 5 minutes.</li><li>13. Verify platform is in S0.</li><li>14. Check HostBootReason (to confirm wake was caused by alarm).</li><li>15. Delete alarm.</li></ol>
Test Pass/ Fail Criteria	Host wakes up both times

## 10.11 Remote Secure Erase

The section serves as a checklist for the environment setup and covers integration testing of the BIOS Remote Secure Erase boot option in Intel® AMT. This feature allows an IT administrator to remotely erase the system drive in a secure fashion; enabling effective system waterfall without the need for direct access.

**Warning:** The testing conducted in this section is specifically designed to check conformity to the Remote Secure Erase feature implementation; which, if implemented properly, will **ERASE** or otherwise **RENDER LOST** the **FULL CONTENTS** of the system drive of the System Under Test (SUT). Read the following information carefully to properly complete testing of this feature.

The following type(s) of drives are supported under the tests in this section:

- SATA - Following the Serial ATA (AT Attachment) interface specification. For these drives, **both** User and Master password credentials **must** be set before Remote Secure Erase can start.
- NVMe\* - Following the Non-Volatile Memory Express\* host controller interface specification, and implemented as a PCI Express\* (PCIe\*)-based SSD. These drives do not support password security.

The following type(s) of drives and/or drive configurations are **not yet** supported under the tests in this section:





- Opal\* - Following the Trusted Computing Group™ Opal Security Subsystem Class (SSC) self-encrypting drive (SED) storage specification. These drives implement Opal Security Mode with associated Security ID (SID) support, when Opal is activated/provisioned.

**Important:** A drive, which supports Opal features, but has not yet been activated/provisioned, may still be eligible for text execution as long as, it adheres to the requirements listed above for supported drive types.

Support for each of the drive types above is dependent on the system BIOS and in some cases the SUT's hardware configuration. The BIOS must inform the Intel® ME through the SMBIOS Type 130 table, whether or not the Remote Secure Erase feature is supported as a capability of the BIOS (and system). This setting in the SMBIOS Type 130 table will determine how the capability is advertised from the Intel® AMT API to remote management consoles. For more information about the BIOS integration requirements, refer the *Intel® ME BIOS Specification*.

The tests conducted herein:

- **Do not** verify actual erasure of data from the target drive(s). Implementation of the drive data erasure protocols deployed by the different drive types covered in this section is in some cases, manufacturer dependent. Rather, the tests herein focus on confirming that proper integration of BIOS functionality with Intel® AMT to enable Remote Secure Erase feature support as follows:
  - Remote Secure Erase capability advertisement from Intel® AMT API per BIOS feature capability reporting in the SMBIOS Type 130 table.
  - Proper management within the Intel® ME of the Secure Erase boot option as set or cleared remotely by the management console.
  - Proper delivery of the Secure Erase boot option to the BIOS during the system boot process.
  - Proper management of the Secure Erase boot option by the BIOS upon completion of the actual drive erase activity.
  - Proper delivery of the drive password (where applicable), either via SOL/KVM redirection through Intel® AMT, or direct password input through Intel® AMT.
  - Proper implementation of BIOS last boot status after Secure Erase completion by the BIOS.
- **Assume** that the system has atleast one primary drive supporting RSE. Support for simultaneous multiple drive Remote Secure Erase is determined by BIOS implementation and system configuration.

*Tip:* The ability to configure the drive password or authentication access procedures is also BIOS dependent (and in the case of Opal\* may require third-party ISV software support to deactivate/unprovision before attempting Remote Secure Erase). Ensure to carefully review available third-party documentation regarding drive password and/or authentication configuration measures for the target drive before beginning testing. These topics are out-of-scope for this document, and Intel cannot provide support for them.

### 10.11.1 Test Environment

The tests in this section are based on the expectation that two kinds of drives have been prepared for testing, and during testing the drives may be interchanged:

- **System Validation Drive** is used for primary system validation for tests in this section, as well as others found in this document and beyond. Only one drive should be prepared for testing; and may be the same drive as had been used in other sections of this chapter.



- **Remote Secure Erase Drive** is intended for tests in this section. One drive per supported drive type should be prepared. These drives may be fully erased multiple times, may not contain a valid Host OS to boot to, and do not contain any critical information necessary for system validation work.

The SUT is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows supported by Intel® PETS, and the **System Validation Drive** used with the SUT should have a version of Microsoft\* Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables.

#### Tools for testing:

- Intel® PETS: The latest version of the tool from the Intel® CSME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- SUT: Should be connected to Intel® APS 3. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the **System Validation Drive** of the SUT.

In order for Intel® PETS to work properly, ensure the following:

- The SUT has a valid System UUID. This can be checked by confirming a non-zero value is reported by the Intel® MEInfo tool.
- The firmware image is configured to **not** require user consent on redirection. This can be done by checking the following value of the SPI image via the Intel® FIT tool in the 'Intel(R) AMT' tab: 'Redirection Configuration' | 'Redirection Privacy / Security Level' set to "Default".

Where applicable, the wireless LAN interface on Intel® AMT must be on a different network/subnet than the wired LAN interface. For details on how to enter the network interface details into Intel® PETS, consult the Intel® PETS User Guide.

If the firmware image or the SUT configuration does not support some features, Intel® PETS will show those features as failing, when tested. Intel® PETS cannot determine in all cases, which features have been deactivated and should thus be skipped during testing.

#### 10.11.1.1 Common Issues and Troubleshooting

**Warning:** If there is a failure during testing, **DO NOT** reconnect the **System Validation Drive** with the SUT, as the Secure Erase boot option may still be set in firmware (even after G3). In this case, first use test AMT\_080 to safely clear the Secure Erase boot option before proceeding with any further testing or corrective action.

The following is a list of common issues that can occur during Remote Secure Erase testing and associated recommendations on how to check test environment and system configuration.

1. Remote Secure Erase did not start.
  - Verify that the BIOS and system support the feature. Check the SMBIOS Type 130 table, which the BIOS provides to the Intel® ME firmware to confirm that the capability is indeed enabled.
  - Verify that the **Remote Secure Erase Drive** is properly attached to the system and that the BIOS can properly identify it. Depending on BIOS implementation, there may be considerations regarding boot list ordering, and therefore may require drive relocation to the first position in the boot list in



order to be identified by the BIOS as a device for use with Remote Secure Erase. Confirm with the system BIOS design for implementation specific details related to **Remote Secure Erase Drive** detection. Refer to the *Intel® ME BIOS Specification* for further information boot order and Secure Erase command execution order.

2. Remote Secure Erase did not complete successfully for an unlocked drive, which **does not require** authentication (password or user authentication).

When this occurs, the SUT should shutdown and the Secure Erase boot option remain set. In this case, on the following boot, the BIOS will detect the Secure Erase boot option and attempt the erase operation again.

IT administrators, who set the Secure Erase boot option and initiate system boot can check the boot option setting as well as the Intel® AMT API to verify, if the boot options had been cleared upon successful erasure.

Failure to properly execute secure erase and clear the Secure Erase boot option may occur for several reasons. Verify the following, when a failure occurs:

- Erase feature is not supported by the BIOS or system for the target drive.
- Target drive is not properly installed or connected.
- BIOS feature support not completely implemented.
- Target drive failure to perform selected erase action.

3. Remote Secure Erase did not complete successfully for a locked drive, which **require** authentication (password or user authentication).

When this occurs, it may be necessary to connect to the SUT via Serial-Over-LAN (SOL) or Keyboard, Video, and Mouse (KVM) to view and respond to the authentication prompt displayed on the SUT screen, if the drive password was **not** already provided directly via Intel® AMT for use during the Remote Secure Erase procedure.

In the case, where User Consent is required to establish a SOL or KVM session, a timeout may occur, where the User Consent display expires without confirmation from the management console. In this case, a drive authentication timeout will occur.

As such, verify the following, when a failure occurs:

- Failure to input the correct password or to properly authenticate with the target drive.
- A User Consent code timeout did not occur during KVM or SOL session activation.

**Note:**

All tests in this section, other than test AMT\_080, require that Intel® AMT power package be set to Power Package 2 (Intel® ME on in S0, wake in Sx/AC) on the SUT. If the WLAN network interface is used, the Intel® AMT WLAN link policy will also be set to Link Policy 3 (Enabled in S0, Sx/AC) on the SUT. The intention is to allow the Secure Erase state to be cleared via test AMT\_080 in the case, where there is a failure during boot and the BIOS shuts down the system to S5.

## 10.11.2 Clear Secure Erase Boot Option

ID	AMT_080
Title	Clear Secure Erase Boot Option
Requirement	Mandatory - exempt for systems which do not support the Secure Erase boot option



ID	AMT_080			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	This test attempts to clear the Remote Secure Erase boot option.			
Objective	Verify that the BIOS properly advertises the Secure Erase boot option as a capability via the SMBIOS Type 130 table. If the capability is properly configured, the Intel® AMT API will indicate feature support. The test will then check the boot option setting, and attempt to clear it.			
Setup	<p>The initial state of the SUT may be in either S0 or S3/S4/S5 with either Power Package 1 (Intel® ME on in S0) or Power Package 2 (Intel® ME on in S0, wake in Sx/AC) applied to Intel® AMT respectively. Similarly, if the WLAN network interface is used, the Intel® AMT WLAN link policy on the SUT must be set to either Link Policy 2 (Enabled in S0), when the system is in S0, or Link Policy 3 (Enabled in S0, Sx/AC), when the system is in S5.</p> <p>The test will not pass, if the system is in G3 or Deep Sx, or if the WLAN network interface is used but not configured in the appropriate Link Policy 2 or Link Policy 3 for the SUT Sx state.</p> <p>The test will not apply power to a SUT, if found in G3. Doing so, with the risk that the Secure Erase boot option is set in firmware, may lead to the system booting from S5 and starting the erasure process on an attached drive.</p>			
Procedure	<ol style="list-style-type: none"> <li>Request the test operator to perform the following steps:  Steps 1 through 3, if the <b>Remote Secure Erase Drive</b> has <b>NOT</b> already been installed. <ol style="list-style-type: none"> <li>Shut down the SUT gracefully to G3 (if needed).</li> <li>Install the <b>Remote Secure Erase Drive</b> for testing.</li> <li>Attach AC power.</li> </ol> <p>---</p> <ol style="list-style-type: none"> <li>Boot the SUT, with the <b>Remote Secure Erase Drive</b>, to the Intel® MEBX menu.  <b>NOTE:</b> It may be necessary to enter a drive password.</li> </ol> </li> <li>Wait for <b>3 minutes</b>, when <b>only</b> the WLAN network interface is available. This is to allow network connectivity stabilization with the active WLAN profile.</li> <li>Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), when <b>only</b> the WLAN network interface is available.</li> <li>Verify that Intel® AMT is available by requesting its version.</li> <li>Check that the SUT supports booting to Secure Erase by querying the Intel® AMT and checking the boot capabilities. <ol style="list-style-type: none"> <li>If supported, continue to the next step.</li> <li>If not supported, end the test and request the test operator to confirm the BIOS support of 'Secure Erase' OEMCapabilities3 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>Clear the Secure Erase boot option on the SUT via Intel® AMT.</li> <li>Perform a Remote Power-Down of the SUT via Intel® AMT.</li> <li>Verify that the SUT is in S5.</li> </ol>			
Pass Criteria	This test passes, if the system was in a supported state at the beginning of testing, and Intel® AMT could be used to confirm the Secure Erase boot option capability, check its status, and clear the setting if set.			
References	For details on the Secure Erase boot option, refer to the <i>Intel® ME BIOS Specification</i> .			



### 10.11.3 Remote Secure Erase without Drive Authentication

ID	AMT_081			
Title	Remote Secure Erase without Drive Authentication			
Requirement	Mandatory - exempt for systems, which: <ul style="list-style-type: none"> <li>Do not support the Secure Erase boot option, or</li> <li>Support only configurations requiring drive authentication</li> </ul>			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	This test attempts to initiate the Remote Secure Erase boot option and verify that the BIOS has completed execution of the erase operation on a drive which does not require authentication.			
Objective	Verify that the BIOS properly advertises and implements the Secure Erase boot option on system configurations which do not require drive authentication.  This test is intended for systems, which support NVMe* drives that do not require password configuration or systems, which support SATA drives and do not require end-user drive password configuration (as may be provided via supplemental BIOS feature support).			
Setup	The initial state of the SUT should be either G3 or S5 with the <b>Remote Secure Erase Drive</b> attached after executing AMT_080. Intel® AMT should be provisioned via manual mode with Power Package 2 (Intel® ME on in S0, wake in Sx/AC) and Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), when <b>only</b> the WLAN network interface is available.			
Procedure	<ol style="list-style-type: none"> <li>Prompt the test operator exit this test and run <b>AMT_080</b> with the target <b>Remote Secure Erase Drive</b>, if they have not done so already.</li> <li>Request the test operator to perform the following steps: Steps 1 through 4, if the BIOS settings have <b>NOT</b> already been confirmed.               <ol style="list-style-type: none"> <li>Boot the SUT to the BIOS menu.</li> <li>Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>Ensure the drive password(s) have been <b>cleared</b> for applicable drives as needed.</li> <li>Save any BIOS settings changes.</li> </ol> </li> <li>Shutdown the SUT to S5. <b>NOTE:</b> It may be necessary to enter a drive password during these steps.</li> <li>Verify that the SUT is in S5.</li> <li>Prompt the test operator to acknowledge that operations past this point may <b>ERASE</b> or otherwise <b>RENDER LOST</b> the <b>FULL CONTENTS</b> of the system drive. The test operator may cancel the test at this time via the prompt or via Intel® PETS test controls.</li> <li>Check that the SUT supports booting to Secure Erase by querying the Intel® AMT and checking the boot capabilities.               <ol style="list-style-type: none"> <li>If supported, continue to the next step.</li> <li>If not supported, end the test and request the test operator to confirm the BIOS support of 'Secure Erase' OEMCapabilities3 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>Set the Secure Erase boot option on the SUT via Intel® AMT.</li> <li>Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure.</li> <li>Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li> <li>Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li> <li>Verify that the BIOS last boot status reports success via Intel® AMT.</li> <li>Verify that the value of Secure Erase boot option setting retrieved at step 11 was cleared by the BIOS.</li> <li>Set the SUT to G3 via Intel® APS.</li> <li>Verify that the SUT is in G3.</li> </ol> If there was a failure during the test, consider running AMT_080 to safely clear the Secure Erase boot option before returning the <b>System Validation Drive</b> to the SUT.			



<b>ID</b>	<b>AMT_081</b>
<b>Pass Criteria</b>	This test passes, if the <b>Remote Secure Erase Drive</b> supported by the SUT can be erased remotely using the Secure Erase boot option, and the BIOS successfully clears the boot options at the end of the operation.
<b>References</b>	For details on the Secure Erase boot option, refer to the <i>Intel® ME BIOS Specification</i> .



### 10.11.4 Remote Secure Erase with Drive Authentication via SOL Redirection

ID	AMT_082			
Title	Remote Secure Erase with Drive Authentication via Serial-Over-LAN (SOL) Redirection			
Requirement	Mandatory - exempt for systems, which: <ul style="list-style-type: none"> <li>Do not support the Secure Erase boot option, or</li> <li>Support only NVMe* configurations not requiring drive authentication</li> </ul>			
System	Form Factor	System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input type="checkbox"/> WLAN	<input checked="" type="checkbox"/> Either Used <input type="checkbox"/> Not Used
Method	Automated by Intel® PETS with test operator interaction			
Description	This test attempts to initiate the Remote Secure Erase boot option and verify that the BIOS has completed execution of the erase operation on a drive, which requires authentication via Serial-Over-LAN (SOL).			
Objective	<p>Verify that the BIOS properly advertises and implements the Secure Erase boot option for drives, which require authentication via Serial-Over-LAN (SOL). Proper User Consent verification is also confirmed.</p> <p>This test should be run once per each drive type supported on the SUT (which have been prepared via one sample each in the set of Remote Secure Erase Drives described in the beginning of this section).</p>			
Setup	<p>The initial state of the SUT should be either G3 or S5 with the <b>Remote Secure Erase Drive</b> attached after executing AMT_080. Intel® AMT should be provisioned via manual mode with Power Package 2 (Intel® ME on in S0, wake in Sx/AC) and Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), when <b>only</b> the WLAN network interface is available.</p> <p>Before running this test, ensure that SOL is enabled in the Intel® MEBX.</p> <p>The default number of rows shown in the Putty terminal window may differ from the number of rows displayed by the BIOS. When this occurs, the Putty terminal display will incur line wrapping problems. To avoid this problem, change the settings of the Putty application to align with the BIOS via the following steps:</p> <ol style="list-style-type: none"> <li>Open the ".\Intel(R) Platform Enablement Test Suite\Plugins\Me\Redirection\bin\" directory.</li> <li>Start putty.exe, and in the Category section: <ol style="list-style-type: none"> <li>Select Window, and change the Rows value to the required number of rows.</li> <li>Select Session, then select <i>Default Settings</i>, and finally click the Save button.</li> </ol> </li> <li>Close the Putty Configuration window.</li> <li>To confirm, start putty.exe again, and make sure Row number is set to the new value.</li> </ol>			
Procedure	<ol style="list-style-type: none"> <li>Prompt the test operator exit this test and run <b>AMT_080</b> with the target <b>Remote Secure Erase Drive</b> if they have not done so already.</li> <li>Request the test operator to perform the following steps: <ol style="list-style-type: none"> <li>Steps 1 through 4, if the BIOS settings have <b>NOT</b> already been confirmed.</li> <li>Boot the SUT to the BIOS menu.</li> <li>Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>Ensure the drive password(s) have been <b>set</b>.</li> <li>Save any BIOS settings changes.</li> <li>---</li> <li>Shutdown the SUT to S5.</li> </ol> </li> <li>It may be necessary to enter a drive password during these steps.</li> <li>Verify that the SUT is in S5.</li> </ol>			



ID	AMT_082
<p><b>Procedure</b> (continued)</p>	<ol style="list-style-type: none"> <li>4. Prompt the test operator to acknowledge that operations past this point may <b>ERASE</b> or otherwise <b>RENDER LOST</b> the <b>FULL CONTENTS</b> of the system drive. The test operator may cancel the test at this time via the prompt or via Intel® PETS test controls.</li> <li>5. Check that the SUT supports booting to Secure Erase by querying the Intel® AMT and checking the boot capabilities.             <ol style="list-style-type: none"> <li>a. If supported, continue to the next step.</li> <li>b. If not supported, end the test and request the test operator to confirm the BIOS support of 'Secure Erase' OEMCapabilities3 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>6. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>7. Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>8. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>9. Prompt the test operator to input the drive password via the Putty terminal program on the management console. For SATA drives, the Master password should be used.</li> <li>10. Use Intel® AMT to set the SUT boot options to use SOL Redirection and activate Secure Erase on the next boot.</li> <li>11. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>12. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>13. Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure, but stop at a drive authentication prompt.</li> <li>14. Close the SOL Redirection session with the SUT via Intel® AMT.</li> <li>15. Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li> <li>16. Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>17. Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li> <li>18. Verify that the BIOS last boot status reports success via Intel® AMT.</li> <li>19. Verify that the value of Secure Erase boot option setting retrieved at step 15 was cleared by the BIOS.</li> </ol> <ol style="list-style-type: none"> <li>20. Request the test operator to perform the following steps: Steps a through b, if the BIOS settings have <b>NOT</b> already been confirmed.             <ol style="list-style-type: none"> <li>a. Boot the SUT to the BIOS menu.</li> <li>b. Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>c. Ensure the drive password(s) have been <b>set</b>.</li> <li>d. Save any BIOS settings changes.</li> </ol> <p>---</p> <ol style="list-style-type: none"> <li>e. Boot the SUT to S0.</li> </ol> <p>It may be necessary to enter a drive password.</p> </li> <li>21. Verify that the SUT is in S0.</li> <li>22. Wait for <b>3 minutes</b>, when <b>only</b> the WLAN network interface is available. This is to allow network connectivity stabilization with the active WLAN profile.</li> <li>23. Wait until Intel® AMT responds to WS-MAN call.</li> <li>24. Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> for boot options (ALL) on the SUT.</li> <li>25. Initiate a user consent session with Intel® AMT.</li> <li>26. Perform a Remote Power-Down of the SUT via Intel® AMT.</li> <li>27. Verify that the SUT is in S5.</li> <li>28. Prompt the test operator to input the drive password via the Putty terminal program on the management console. Note: For SATA drives, the Master password should be used.</li> <li>29. Use Intel® AMT to set the SUT boot options to use SOL Redirection and activate Secure Erase on the next boot.</li> <li>30. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>31. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>32. Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure, but stop at a drive authentication prompt.</li> <li>33. Close the SOL Redirection session with the SUT via Intel® AMT.</li> <li>34. Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li> <li>35. Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>36. Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li> <li>37. Verify that the BIOS last boot status reports success via Intel® AMT.</li> <li>38. Verify that the value of Secure Erase boot option setting retrieved at step 35 was cleared by the BIOS.</li> </ol>





ID	AMT_082
<b>Procedure</b> (continued)	<p>39. Set the SUT to G3 via Intel® APS.</p> <p>40. Verify that the SUT is in G3.</p> <p>41. Request the test operator to repeat the test for each remaining representative type of <b>Remote Secure Erase Drive</b> supported by the SUT. Otherwise, return the <b>System Validation Drive</b> to the SUT.</p> <p>If there was a failure during the test, consider running AMT_080 to safely clear the Secure Erase boot option before returning the <b>System Validation Drive</b> to the SUT.</p>
<b>Pass Criteria</b>	<p>This test passes, if each of the representative sample types of <b>Remote Secure Erase Drive</b> supported by the SUT can each be erased remotely using the Secure Erase boot option with drive authentication via SOL (also under User Consent control), and the BIOS successfully clears the boot options at the end of each operation.</p>
<b>References</b>	<p>For details on the Secure Erase boot option, refer to the <i>Intel® ME BIOS Specification</i>.</p>



## 10.11.5 Remote Secure Erase with Drive Authentication via KVM Redirection

ID	AMT_083			
Title	Remote Secure Erase with Drive Authentication via Keyboard, Video and Mouse (KVM) Redirection			
Requirement	Mandatory - exempt for systems, which: <ul style="list-style-type: none"> <li>Do not support the Secure Erase boot option, or</li> <li>Support only NVMe* configurations not requiring drive authentication, or</li> <li>Do not support KVM with internal graphics</li> </ul>			
System	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	This test attempts to initiate the Remote Secure Erase boot option and verify that the BIOS has completed execution of the erase operation on a drive which requires authentication via Keyboard, Video and Mouse (KVM).			
Objective	<p>Verify that the BIOS properly advertises and implements the Secure Erase boot option for drives which require authentication via Keyboard, Video and Mouse (KVM). Proper User Consent verification is also confirmed.</p> <p>This test should be run once per each drive type supported on the SUT (which have been prepared via one sample each in the set of Remote Secure Erase Drives described in the beginning of this section).</p>			
Setup	<p>The initial state of the SUT should be either G3 or S5 with the <b>Remote Secure Erase Drive</b> attached after executing AMT_080. Intel® AMT should be provisioned via manual mode with Power Package 2 (Intel® ME on in S0, wake in Sx/AC) and Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), when <b>only</b> the WLAN network interface is available.</p> <p>Before running this test, ensure that KVM is enabled in the Intel® MEBX. If the SUT supports switchable graphics, graphics configuration should be set to <b>integrated</b> graphics.</p>			
Procedure	<ol style="list-style-type: none"> <li>Prompt the test operator exit this test and run <b>AMT_080</b> with the target <b>Remote Secure Erase Drive</b> if they have not done so already.</li> <li>Request the test operator to perform the following steps: <ol style="list-style-type: none"> <li>Steps 1 through 4, if the BIOS settings have <b>NOT</b> already been confirmed.</li> <li>1. Boot the SUT to the BIOS menu.</li> <li>2. Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>3. Ensure the drive password(s) have been <b>set</b>.</li> <li>4. Save any BIOS settings changes.</li> <li>---</li> <li>5. Shutdown the SUT to S5.</li> </ol> <p>It may be necessary to enter a drive password during these steps.</p> </li> <li>3. Verify that the SUT is in S5.</li> </ol>			



ID	AMT_083
<p><b>Procedure</b> (continued)</p>	<ol style="list-style-type: none"> <li>4. Prompt the test operator to acknowledge that operations past this point may <b>ERASE</b> or otherwise <b>RENDER LOST</b> the <b>FULL CONTENTS</b> of the system drive. The test operator may cancel the test at this time via the prompt or via Intel® PETS test controls.</li> <li>5. Check that the SUT supports booting to Secure Erase by querying the Intel® AMT and checking the boot capabilities.             <ol style="list-style-type: none"> <li>a. If supported, continue to the next step.</li> <li>b. If not supported, end the test and request the test operator to confirm the BIOS support of 'Secure Erase' OEMCapabilities3 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>6. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>7. Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li> <li>8. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>9. Prompt the test operator to input the drive password via the VNC Viewer program on the management console. For SATA drives, the Master password should be used.</li> <li>10. Set the KVM password to 'Admin!98' on the SUT via Intel® AMT.</li> <li>11. Ensure that the VNC port 5900 is enabled on the SUT via Intel® AMT.</li> <li>12. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>13. Set the Secure Erase boot option on the SUT via Intel® AMT.</li> <li>14. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>15. Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure, but stop at a drive authentication prompt.</li> <li>16. Close the KVM Redirection session with the SUT via Intel® AMT.</li> <li>17. Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li> <li>18. Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>19. Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li> <li>20. Verify that the BIOS last boot status reports success via Intel® AMT.</li> <li>21. Verify that the value of Secure Erase boot option setting retrieved at Step 17 was cleared by the BIOS.</li> </ol> <ol style="list-style-type: none"> <li>22. Request the test operator to perform the following steps: Steps 1 through 4, if the BIOS settings have <b>NOT</b> already been confirmed.             <ol style="list-style-type: none"> <li>1. Boot the SUT to the BIOS menu.</li> <li>2. Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>3. Ensure the drive password(s) have been <b>set</b>.</li> <li>4. Save any BIOS settings changes.</li> </ol> <p>---</p> <li>5. Shutdown the SUT to S5. It may be necessary to enter a drive password during these steps.</li> </li></ol> <li>23. Verify that the SUT is in S5.</li> <li>24. Prompt the test operator to input the drive password via the VNC Viewer on the management console. Note: For SATA drives, the Master password should be used.</li> <li>25. Ensure the Intel® AMT user consent opt-in setting is <b>enabled</b> for KVM on the SUT.</li> <li>26. Open a KVM Redirection session with the SUT via Intel® AMT using the VNC Viewer on the management console.</li> <li>27. Set the Secure Erase boot option on the SUT via Intel® AMT.</li> <li>28. Perform a Remote Power-Up of the SUT via Intel® AMT. A user consent code will be displayed on the SUT screen.</li> <li>29. Request the test operator to enter the user consent code into the VNC Viewer on the management console.</li> <li>30. Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure, but stop at a drive authentication prompt.</li> <li>31. Close the KVM Redirection session with the SUT via Intel® AMT.</li> <li>32. Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li> <li>33. Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>34. Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li> <li>35. Verify that the BIOS last boot status reports success via Intel® AMT.</li> <li>36. Verify that the value of Secure Erase boot option setting retrieved at step 33 was cleared by the BIOS.</li>



ID	AMT_083
Procedure (continued)	<p>37. Set the SUT to G3 via Intel® APS.</p> <p>38. Verify that the SUT is in G3.</p> <p>39. Request the test operator to repeat the test for each remaining representative type of <b>Remote Secure Erase Drive</b> supported by the SUT. Otherwise, return the <b>System Validation Drive</b> to the SUT.</p> <p>If there was a failure during the test, consider running AMT_080 to safely clear the Secure Erase boot option before returning the <b>System Validation Drive</b> to the SUT.</p>
Pass Criteria	<p>This test passes, if each of the representative sample types of <b>Remote Secure Erase Drive</b> supported by the SUT can each be erased remotely using the Secure Erase boot option with drive authentication via KVM (also under User Consent control), and the BIOS successfully clears the boot options at the end of each operation.</p>
References	<p>For details on the Secure Erase boot option, refer to the <i>Intel® ME BIOS Specification</i>.</p>



## 10.11.6 Remote Secure Erase with Drive Authentication via Direct Password Input

ID	AMT_084			
Title	Remote Secure Erase with Drive Authentication via Direct Password Input			
Requirement	Mandatory - exempt for systems which: <ul style="list-style-type: none"> <li>Do not support the Secure Erase boot option, or</li> <li>Support only NVMe* configurations not requiring drive authentication</li> </ul>			
System	Form Factor	System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	This test attempts to initiate the Remote Secure Erase boot option and verify that the BIOS has completed execution of the erase operation on a drive which requires authentication via direct password input from the management console.			
Objective	Verify that the BIOS properly advertises and implements the Secure Erase boot option for drives which require authentication via direct password input from the management console.  This test should be run once per each drive type supported on the SUT (which have been prepared via one sample each in the set of Remote Secure Erase Drives described in the beginning of this section).			
Setup	The initial state of the SUT should be either G3 or S5 with the <b>Remote Secure Erase Drive</b> attached after executing AMT_080. Intel® AMT should be provisioned via manual mode with Power Package 2 (Intel® ME on in S0, wake in Sx/AC) and Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), when <b>only</b> the WLAN network interface is available.			
Procedure	<ol style="list-style-type: none"> <li>Prompt the test operator exit this test and run <b>AMT_080</b> with the target <b>Remote Secure Erase Drive</b> if they have not done so already.</li> <li>Request the test operator to perform the following steps: Steps 1 through 4, if the BIOS settings have <b>NOT</b> already been confirmed. <ol style="list-style-type: none"> <li>Boot the SUT to the BIOS menu.</li> <li>Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>Ensure the drive password(s) have been <b>set</b>.</li> <li>Save any BIOS settings changes.</li> </ol> </li> <li>Shutdown the SUT to S5. It may be necessary to enter a drive password during these steps.</li> <li>Verify that the SUT is in S5.</li> </ol>			



ID	AMT_084
Procedure (continued)	<ol style="list-style-type: none"><li>4. Prompt the test operator to acknowledge that operations past this point may <b>ERASE</b> or otherwise <b>RENDER LOST</b> the <b>FULL CONTENTS</b> of the system drive. The test operator may cancel the test at this time via the prompt or via Intel® PETS test controls.</li><li>5. Check that the SUT supports booting to Secure Erase by querying the Intel® AMT and checking the boot capabilities.<ol style="list-style-type: none"><li>a. If supported, continue to the next step.</li><li>b. If not supported, end the test and request the test operator to confirm the BIOS support of 'Secure Erase' OEMCapabilities3 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li></ol></li><li>6. Cancel any existing Intel® AMT user consent session, which may be active on the SUT.</li><li>7. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li><li>8. Prompt the test operator to input the drive password via Intel® PETS on the management console. For SATA drives, the Master password should be used.</li><li>9. Set the Secure Erase boot option and the drive password on the SUT via Intel® AMT.</li><li>10. Perform a Remote Power-Up of the SUT via Intel® AMT.</li><li>11. Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure using the drive password, which was provided through Intel® PETS from the management console.</li><li>12. Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li><li>13. Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li><li>14. Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li><li>15. Verify that the BIOS last boot status reports success via Intel® AMT.</li><li>16. Verify that the value of Secure Erase boot option setting retrieved at step 12 was cleared by the BIOS.</li></ol> <ol style="list-style-type: none"><li>17. Set the SUT to G3 via Intel® APS.</li><li>18. Verify that the SUT is in G3.</li><li>19. Request the test operator to repeat the test for each remaining representative type of <b>Remote Secure Erase Drive</b> supported by the SUT. Otherwise, return the <b>System Validation Drive</b> to the SUT.</li></ol> <p>If there was a failure during the test, consider running AMT_080 to safely clear the Secure Erase boot option before returning the <b>System Validation Drive</b> to the SUT.</p>
Pass Criteria	This test passes, if each of the representative sample types of <b>Remote Secure Erase Drive</b> supported by the SUT can each be erased remotely using the Secure Erase boot option with drive authentication via direct password input from the management console, and the BIOS successfully clears the boot options at the end of each operation.
References	For details on the Secure Erase boot option, refer to the <i>Intel® ME BIOS Specification</i> .



## 10.11.7 Remote Secure Erase with Drive Authentication Failure via SOL Redirection

ID	AMT_085			
Title	Remote Secure Erase with Drive Authentication Failure via Serial-Over-LAN (SOL) Redirection			
Requirement	Mandatory - exempt for systems, which: <ul style="list-style-type: none"> <li>Do not support the Secure Erase boot option, or</li> <li>Support only NVMe* configurations not requiring drive authentication</li> </ul>			
System	Form Factor	System Power Model	Intel® AMT Network Interface	LAN Type
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	This test attempts to initiate the Remote Secure Erase boot option and verify that the BIOS has implemented proper error handling of the erase operation on a drive, which requires authentication via Serial-Over-LAN (SOL).			
Objective	<p>Verify that the BIOS properly advertises and implements error handling with the Secure Erase boot option for drives which require authentication via Serial-Over-LAN (SOL) but were not authenticated during the erasure process.</p> <p>This test should be run once per each drive type supported on the SUT (which have been prepared via one sample each in the set of Remote Secure Erase Drives described in the beginning of this section).</p>			
Setup	<p>The initial state of the SUT should be either G3 or S5 with the <b>Remote Secure Erase Drive</b> attached after executing AMT_080. Intel® AMT should be provisioned via manual mode with Power Package 2 (Intel® ME on in S0, wake in Sx/AC) and Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), when <b>only</b> the WLAN network interface is available.</p> <p>Before running this test, ensure that SOL is enabled in the Intel® MEBX.</p> <p>The default number of rows shown in the Putty terminal window may differ from the number of rows displayed by the BIOS. When this occurs, the Putty terminal display will incur line wrapping problems. To avoid this problem, change the settings of the Putty application to align with the BIOS via the following steps:</p> <ol style="list-style-type: none"> <li>Open the "..\Intel(R) Platform Enablement Test Suite\Plugins\Me\Redirection\bin\" directory.</li> <li>Start putty.exe, and in the Category section: <ol style="list-style-type: none"> <li>Select Window, and change the <u>R</u>ows value to the required number of rows.</li> <li>Select Session, then select <i>Default Settings</i>, and finally click the <u>S</u>ave button.</li> </ol> </li> <li>Close the Putty Configuration window.</li> <li>To confirm, start putty.exe again, and make sure Row number is set to the new value.</li> </ol>			
Procedure	<ol style="list-style-type: none"> <li>Prompt the test operator exit this test and run <b>AMT_080</b> with the target <b>Remote Secure Erase Drive</b>, if they have not done so already.</li> <li>Request the test operator to perform the following steps: <ol style="list-style-type: none"> <li>Steps 1 through 4, if the BIOS settings have <b>NOT</b> already been confirmed. <ol style="list-style-type: none"> <li>Boot the SUT to the BIOS menu.</li> <li>Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>Ensure the drive password(s) have been <b>set</b>.</li> <li>Save any BIOS settings changes.</li> </ol> </li> <li>---</li> <li>Shutdown the SUT to S5.</li> </ol> <p>It may be necessary to enter a drive password during these steps.</p> </li> <li>Verify that the SUT is in S5.</li> </ol>			



ID	AMT_085
Procedure (continued)	<ol style="list-style-type: none"> <li>4. Prompt the test operator to acknowledge that operations past this point may <b>ERASE</b> or otherwise <b>RENDER LOST</b> the <b>FULL CONTENTS</b> of the system drive. The test operator may cancel the test at this time via the prompt or via Intel® PETS test controls.</li> <li>5. Check that the SUT supports booting to Secure Erase by querying the Intel® AMT and checking the boot capabilities. <ol style="list-style-type: none"> <li>a. If supported, continue to the next step.</li> <li>b. If not supported, end the test and request the test operator to confirm the BIOS support of 'Secure Erase' OEMCapabilities3 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>6. Ensure the Intel® AMT redirection ports are <b>enabled</b> on the SUT.</li> <li>7. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>8. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>9. Prompt the test operator to input <b>an invalid</b> drive password via the Putty terminal program on the management console as many times as needed for authentication failure to occur.</li> <li>10. Use Intel® AMT to set the SUT boot options to use SOL Redirection and activate Secure Erase on the next boot.</li> <li>11. Open a SOL Redirection session with the SUT via Intel® AMT using the Putty terminal program on the management console.</li> <li>12. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>13. Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure, but stop at a drive authentication prompt.</li> <li>14. Close the SOL Redirection session with the SUT via Intel® AMT.</li> <li>15. Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li> <li>16. Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>17. Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li> <li>18. Verify that the BIOS last boot status reports <b>authentication failure</b> via Intel® AMT.</li> <li>19. Verify that the value of Secure Erase boot option setting retrieved at step 15 was <b>not</b> cleared by the BIOS.</li> </ol>
	<ol style="list-style-type: none"> <li>20. Set the SUT to G3 via Intel® APS.</li> <li>21. Verify that the SUT is in G3.</li> <li>22. Request the test operator to repeat the test for each remaining representative type of <b>Remote Secure Erase Drive</b> supported by the SUT. Otherwise, return the <b>System Validation Drive</b> to the SUT.</li> </ol> <p>If there was a failure during the test, consider running AMT_080 to safely clear the Secure Erase boot option before returning the <b>System Validation Drive</b> to the SUT.</p>
Pass Criteria	This test passes, if each of the representative sample types of <b>Remote Secure Erase Drive</b> supported by the SUT <b>are not</b> erased remotely using the Secure Erase boot option with drive authentication <b>failure</b> via SOL (also under User Consent control), and the BIOS <b>does not</b> clear the boot options at the end of each operation.
References	For details on the Secure Erase boot option, refer to the <i>Intel® ME BIOS Specification</i> .





### 10.11.8 Remote Secure Erase with Drive Authentication Failure via Direct Password Input

ID	AMT_086			
Title	Remote Secure Erase with Drive Authentication Failure via Direct Password Input			
Requirement	Mandatory - exempt for systems, which: <ul style="list-style-type: none"> <li>Do not support the Secure Erase boot option, or</li> <li>Support only NVMe* configurations not requiring drive authentication</li> </ul>			
System	Form Factor	System Power Model	Intel® AMT Network Interface	
	<input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<input type="checkbox"/> LAN <input checked="" type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
Method	Automated by Intel® PETS with test operator interaction			
Description	This test attempts to initiate the Remote Secure Erase boot option and verify that the BIOS has implemented proper error handling of the erase operation on a drive, which requires authentication via direct password input from the management console.			
Objective	<p>Verify that the BIOS properly advertises and implements error handling with the Secure Erase boot option for drives, which require authentication via direct password input from the management console but were not authenticated during the erasure process.</p> <p>This test should run once per each drive type supported on the SUT (which have been prepared via one sample each in the set of Remote Secure Erase Drives described in the beginning of this section).</p>			
Setup	The initial state of the SUT should be either G3 or S5 with the <b>Remote Secure Erase Drive</b> attached after executing AMT_080. Intel® AMT should be provisioned via manual mode with Power Package 2 (Intel® ME on in S0, wake in Sx/AC) and Intel® AMT WLAN link policy on the SUT to Link Policy 3 (Enabled in S0, Sx/AC), when <b>only</b> the WLAN network interface is available.			
Procedure	<ol style="list-style-type: none"> <li>Prompt the test operator exit this test and run <b>AMT_080</b> with the target <b>Remote Secure Erase Drive</b> if they have not done so already.</li> <li>Request the test operator to perform the following steps: Steps 1 through 4, if the BIOS settings have <b>NOT</b> already been confirmed. <ol style="list-style-type: none"> <li>Boot the SUT to the BIOS menu.</li> <li>Verify device boot order to ensure BIOS' <b>Remote Secure Erase Drive</b> detection.</li> <li>Ensure the drive password(s) have been <b>set</b>.</li> <li>Save any BIOS settings changes.</li> <li>---</li> <li>Shutdown the SUT to S5.</li> </ol> It may be necessary to enter a drive password during these steps. </li> <li>Verify that the SUT is in S5.</li> </ol>			



ID	AMT_086
Procedure (continued)	<ol style="list-style-type: none"> <li>4. Prompt the test operator to acknowledge that operations past this point may <b>ERASE</b> or otherwise <b>RENDER LOST</b> the <b>FULL CONTENTS</b> of the system drive. The test operator may cancel the test at this time via the prompt or via Intel® PETS test controls.</li> <li>5. Check that the SUT supports booting to Secure Erase by querying the Intel® AMT and checking the boot capabilities.               <ol style="list-style-type: none"> <li>a. If supported, continue to the next step.</li> <li>b. If not supported, end the test and request the test operator to confirm the BIOS support of 'Secure Erase' OEMCapabilities3 setting provided to the Intel® ME via the SMBIOS Type 130 table.</li> </ol> </li> <li>6. Cancel any existing Intel® AMT user consent session which may be active on the SUT.</li> <li>7. Ensure the Intel® AMT user consent opt-in setting is <b>disabled</b> on the SUT.</li> <li>8. Prompt the test operator to input <b>an invalid</b> drive password via Intel® PETS on the management console.</li> <li>9. Set the Secure Erase boot option and the drive password on the SUT via Intel® AMT.</li> <li>10. Perform a Remote Power-Up of the SUT via Intel® AMT.</li> <li>11. Wait for the SUT to return to S0/MeOn. At this point, the BIOS should receive the Secure Erase boot option and begin drive erasure using the drive password which was provided through Intel® PETS from the management console.</li> <li>12. Poll the system for S5 for <b>10 minutes</b> (maximum wait) for drive erasure completion. The test operator shall be able to configure the polling duration to control the maximum duration for drives that take longer to complete erasure.</li> <li>13. Get the Secure Erase boot option setting on the SUT via Intel® AMT and log it.</li> <li>14. Clear the Secure Erase boot option on the SUT via Intel® AMT (safety precaution).</li> <li>15. Verify that the BIOS last boot status reports <b>authentication failure</b> via Intel® AMT.</li> <li>16. Verify that the value of Secure Erase boot option setting retrieved at step 12 was <b>not</b> cleared by the BIOS.</li> </ol> <ol style="list-style-type: none"> <li>17. Set the SUT to G3 via Intel® APS.</li> <li>18. Verify that the SUT is in G3.</li> <li>19. Request the test operator to repeat the test for each remaining representative type of <b>Remote Secure Erase Drive</b> supported by the SUT. Otherwise, return the <b>System Validation Drive</b> to the SUT.</li> </ol> <p>If there was a failure during the test, consider running AMT_080 to safely clear the Secure Erase boot option before returning the <b>System Validation Drive</b> to the SUT.</p>
Pass Criteria	This test passes, if each of the representative sample types of <b>Remote Secure Erase Drive</b> supported by the SUT <b>are not</b> erased remotely using the Secure Erase boot option with drive authentication <b>failure</b> via direct password input from the management console, and the BIOS <b>does not</b> clear the boot options at the end of each operation.
References	For details on the Secure Erase boot option, refer to the <i>Intel® ME BIOS Specification</i> .

## 10.12 Basic Wired and wireless Connectivity Checks

### 10.12.1 Wired Connectivity Check in S0

ID	AMT_090				
Title	Wired connectivity check in S0.				
Requirement	Mandatory.				
System	<div>Form Factor</div> <div> <input checked="" type="checkbox"/> Desktop   <input checked="" type="checkbox"/> Workstation  <input checked="" type="checkbox"/> Mobile               </div>	<div>System Power Model</div> <div> <input checked="" type="checkbox"/> Standard  <input checked="" type="checkbox"/> Modern Standby or InstantGo*               </div>	<div>Intel® AMT Network Interface</div> <div> <input checked="" type="checkbox"/> LAN   <input type="checkbox"/> Either Used  <input type="checkbox"/> WLAN   <input type="checkbox"/> Not Used               </div>	<div>LAN Type</div> <div> <input type="checkbox"/> Integrated LAN  <input checked="" type="checkbox"/> Discrete LAN  <input checked="" type="checkbox"/> TBT Dock LAN               </div>	
Method	Automated by Intel® PETS.				
Description	This test checks the LAN connectivity and active BUS during S0.				
Objective	Verify vPro system wired connection in <b>S0</b> state.				



<b>ID</b>	<b>AMT_090</b>
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. Query SUT wired IP.</li> <li>5. Verify Ethernet cable is connected to SUT.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Connect to SUT IP and port 16992 from Management console.</li> <li>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>3. Verify SUT is in <b>S0</b> state.</li> <li>4. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> <li>5. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>PCIe</b> BUS is active by checking if value matches to "<b>PCIe</b>".</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

## 10.12.2 Wired and Wireless Connectivity Check in S0

<b>ID</b>	<b>AMT_091</b>			
<b>Title</b>	Wired and wireless connectivities check in S0.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS.			
<b>Description</b>	This test checks the wireless and LAN connectivities in parallel during S0.			
<b>Objective</b>	Verify vPro system wired and wireless connection in <b>S0</b> state.			
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. Query SUT wired and wireless IP.</li> <li>5. Verify Ethernet cable is connected to SUT.</li> <li>6. Refer to AMT_21 setup section for wireless AMT preparation.</li> </ol>			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Run <b>AMT_090 test</b>.</li> <li>2. Connect to SUT <b>wireless</b> IP and port 16992 from Management console. <b>NOTE:</b> This step is in parallel to active wire connection.</li> <li>3. Query Intel ME firmware version using WSMAN command or using wireless WebUI, "System Status", Intel AMT FW version in lower panel. <b>NOTE:</b> This step indicates successful connectivity using wireless connectivity in SUT.</li> </ol>			
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.			
<b>References</b>	N/A			

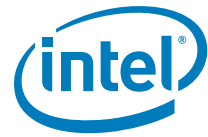


### 10.12.3 Wired Connectivity Check in S3

<b>ID</b>	<b>AMT_092</b>			
<b>Title</b>	Wired connectivity check in S3.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS.			
<b>Description</b>	This test checks the LAN connectivity and active BUS during S3 while dock is connected or not.			
<b>Objective</b>	Verify vPro system wired connection in <b>S3</b> state.			
<b>Setup</b>	<ol style="list-style-type: none"><li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li><li>2. Intel® AMT should be provisioned via manual mode.</li><li>3. SUT power port should be connected to power supply.</li><li>4. Query SUT wired IP.</li><li>5. Verify Ethernet cable is connected to SUT.</li></ol>			
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in Sx).</li><li>2. Select Windows-&gt;Power-&gt;<b>Sleep</b>.</li><li>3. Verify SUT is in <b>S3</b> state.</li><li>4. Connect to SUT IP and port 16992 from Management console.</li><li>5. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>6. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li><li>7. From WebUI or using RCO command, return to S0 state.</li><li>8. Verify machine is up in S0 state.</li><li>9. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li></ol>			
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.			
<b>References</b>	N/A			

### 10.12.4 Wired Connectivity Check in S4

<b>ID</b>	<b>AMT_093</b>			
<b>Title</b>	Wired connectivity check in S4.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS.			
<b>Description</b>	This test checks the LAN connectivity and active BUS during S4.			
<b>Objective</b>	Verify vPro system wired connection in <b>S4</b> state.			
<b>Setup</b>	<ol style="list-style-type: none"><li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li><li>2. Intel® AMT should be provisioned via manual mode.</li><li>3. SUT power port should be connected to power supply.</li><li>4. Query SUT wired IP.</li><li>5. Verify Ethernet cable is connected to SUT.</li></ol>			



<b>ID</b>	<b>AMT_093</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in Sx).</li> <li>2. Select Windows-&gt;Power-&gt;<b>Hibernate</b>.</li> <li>3. Verify SUT is in <b>S4</b> state.</li> <li>4. Connect to SUT IP and port 16992 from Management console.</li> <li>5. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> <li>6. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li> <li>7. From WebUI or using RCO command, power up machine.</li> <li>8. Verify machine is up in S0 state.</li> <li>9. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

### 10.12.5 Wired Connectivity Check in S5

<b>ID</b>	<b>AMT_094</b>			
<b>Title</b>	Wired connectivity check in S5.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS.			
<b>Description</b>	This test checks the LAN connectivity and active BUS during S5.			
<b>Objective</b>	Verify vPro system wired connection in <b>S5</b> state.			
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. Query SUT wired IP.</li> <li>5. Verify Ethernet cable is connected to SUT.</li> </ol>			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in Sx).</li> <li>2. Select Windows-&gt;Power-&gt;<b>Shutdown</b>.</li> <li>3. Verify SUT is in <b>S5</b> state.</li> <li>4. Connect to SUT IP and port 16992 from Management console.</li> <li>5. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> <li>6. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li> <li>7. From WebUI or using RCO command, power up machine.</li> <li>8. Verify machine is up in S0 state.</li> <li>9. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> </ol>			
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.			
<b>References</b>	N/A			



## 10.12.6 Wired Remote Power Control Transition Check

<b>ID</b>	<b>AMT_095</b>			
<b>Title</b>	Wired Remote Power Control Transition Check.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS.			
<b>Description</b>	This test preform remote power control transitions.			
<b>Objective</b>	Verify vPro system wired connection in different power transitions.			
<b>Setup</b>	1. The initial state of the SUT should be S0/MeOn with host OS running. 2. Intel® AMT should be provisioned via manual mode. 3. SUT power port should be connected to power supply. 4. Query wired SUT IP. 5. Verify Ethernet cable is connected to SUT.			
<b>Procedure</b>	1. Connect to SUT IP and port 16992 from Management console 2. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC). 3. in S0 state, query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel 4. Select Windows->Power-> <b>Sleep</b> . 5. Verify SUT is in <b>S3</b> state. 6. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. 7. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to " <b>SMBUS</b> ". 8. From WebUI or using RCO command, power up machine to S0. 9. Select Windows->Power-> <b>Hibernate</b> . 10. Verify SUT is in <b>S4</b> state. 11. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. 12. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to " <b>SMBUS</b> ". <b>NOTE:</b> This step is relevant to PETS only while using a platform connected to TBT dock or platform with discrete LAN. 13. Return to S0 state using RCO command from WebUI. 14. Select Windows->Power-> <b>Shutdown</b> . 15. Verify SUT is in <b>S5</b> state. 16. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. 17. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to " <b>SMBUS</b> ". <b>NOTE:</b> This step is relevant to PETS only while using a platform connected to TBT dock or platform with discrete LAN. 18. From WebUI or using RCO command, return to S0 state.			
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.			
<b>References</b>	N/A			



## 10.12.7 Wired Connection Check Using IPV6

<b>ID</b>	<b>AMT_096</b>			
<b>Title</b>	Wired Connection Check Using IPV6.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input checked="" type="checkbox"/> Desktop <input checked="" type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Manual.			
<b>Description</b>	This test preform remote power control transitions.			
<b>Objective</b>	Verify vPro system wired connection while using IPV6.			
<b>Setup</b>	1. The initial state of the SUT should be S0/MeOn with host OS running. 2. Intel® AMT should be provisioned via manual mode. 3. SUT power port should be connected to power supply. 4. Query wired SUT IP. 5. Verify Ethernet cable is connected to SUT. 6. Enable IPV6 in DHCP server and make sure IPV6 is functional. 7. Enable IPV6 in local WebUI <b>IPV6 Network Setting</b> screen. 8. Verify <b>IPV6 Network Setting contains</b> 2 or 3 IPV6 addresses. 9. Run IPConfig to check IPV6 is configure properly. 10. Run ping command to check IPV6 ping response.  <b>NOTE:</b> This indicates IPV6 address was allocated from DHCP server			
<b>Procedure</b>	1. Verify SUT is in <b>S0</b> state. 2. Connect to SUT Wired <b>IPV6</b> IP and port 16992 from Management console. 3. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT. 4. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>PCIe</b> BUS is active by checking if value matches to " <b>PCIe</b> ".			
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.			
<b>References</b>	N/A			

## 10.13 Intel® AMT Over Thunderbolt™ Dock

The section serves as a checklist for the environment setup and covers integration testing of the AMT over TBT Dock. This feature allow to do AMT wired connectivity with TBT dock.

**Note:** A special IFWI image should be created with discrete LAN enable, refer to "Check Intel® AMT Connectivity using TBT dock station and SUT Discrete\Integrated LAN" test for additional info.



## 10.13.1 Intel® AMT Over Thunderbolt™ Dock with SUT Integrated LAN

### 10.13.1.1 Wired Connectivity Check in S0 with Different TBT Dock States

ID	AMT_100				
Title	Wired connectivity check in S0 with different TBT dock states.				
Requirement	Mandatory.				
System	<div>Form Factor</div> <div><input type="checkbox"/> Desktop   <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile</div>	<div>System Power Model</div> <div><input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*</div>	<div>Intel® AMT Network Interface</div> <div><input checked="" type="checkbox"/> LAN   <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN   <input type="checkbox"/> Not Used</div>	<div>LAN Type</div> <div><input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN</div>	
Method	Automated by Intel® PETS with test operator interaction.				
Description	This test checks the LAN connectivity and active BUS during S0 while dock is connected or not.				
Objective	Verify vPro system wire connection availability with or without TBT dock in S0 state.				
Setup	<div>1. The initial state of the SUT should be S0/MeOn with host OS running.</div> <div>2. Intel® AMT should be provisioned via manual mode.</div> <div>3. SUT power port should be connected to power supply.</div> <div>4. TBT dock should not be connected to SUT.</div> <div>5. Query SUT IP and TBT dock IP.</div> <div>6. Verify Ethernet cables are connected to SUT and TBT dock.</div>				
Procedure	<div>1. Connect to SUT IP and port 16992 from Management console.</div> <div>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</div> <div>3. Verify SUT is in <b>S0</b> state.</div> <div>4. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT.</div> <div>5. Disconnect Ethernet cable from SUT.</div> <div>6. Connect the dock to SUT using TypeC TBT cable.</div> <div>7. Connect to dock IP and port 16992 from Management Console.</div> <div>8. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using FXVL LAN in TBT dock.</div> <div>9. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>PCIe</b> BUS is active by checking if value matches to "<b>PCIe</b>".</div> <div>10. Disconnect dock from SUT.</div> <div>11. Connect Ethernet cable to SUT.</div> <div>12. Connect to SUT IP and port 16992 from Management console.</div> <div>13. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</div>				
Pass Criteria	This test passes if each of the step above passed successfully.				
References	N/A				

### 10.13.1.2 Wired Connectivity Check in S3 with Different TBT Dock States

<b>ID</b>	<b>AMT_101</b>				
<b>Title</b>	Wired connectivity check in S3 with different TBT dock states.				
<b>Requirement</b>	Mandatory.				
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN	





<b>ID</b>	<b>AMT_101</b>
<b>Method</b>	Automated by Intel® PETS with test operator interaction.
<b>Description</b>	This test checks the LAN connectivity and active BUS during S3 while dock is connected or not.
<b>Objective</b>	Verify vPro system wire connection availability with or without TBT dock in S3 state.
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. TBT dock should not be connected to SUT.</li> <li>5. Query SUT IP and TBT dock IP.</li> <li>6. Verify Ethernet cables are connected to SUT and TBT dock.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>2. Select Windows-&gt;Power-&gt;Sleep.</li> <li>3. Verify SUT is in <b>S3</b> state.</li> <li>4. Connect to SUT IP and port 16992 from Management console.</li> <li>5. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT.</li> <li>6. Disconnect Ethernet cable from SUT.</li> <li>7. Connect the dock to SUT using TypeC TBT cable.</li> <li>8. Connect to dock IP and port 16992 from Management Console.</li> <li>9. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using FXVL LAN in TBT dock.</li> <li>10. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li> <li>11. Disconnect dock from SUT.</li> <li>12. Connect Ethernet cable to SUT.</li> <li>13. Connect to SUT IP and port 16992 from Management console.</li> <li>14. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> <li>15. From WebUI or using RCO command, return to S0 state.</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

### 10.13.1.3 Wired Connectivity Check in S4 with different TBT Dock States

<b>ID</b>	<b>AMT_102</b>			
<b>Title</b>	Wired connectivity check in S4 with different TBT dock states.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction.			
<b>Description</b>	This test checks the LAN connectivity and active BUS during S4 while dock is connected or not.			
<b>Objective</b>	Verify vPro system wire connection availability with or without TBT dock in S4 state.			
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. TBT dock should not be connected to SUT.</li> <li>5. Query SUT IP and TBT dock IP.</li> <li>6. Verify Ethernet cables are connected to SUT and TBT dock.</li> </ol>			



<b>ID</b>	<b>AMT_102</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>2. Select Windows-&gt;Power-&gt;Hibernate.</li> <li>3. Verify SUT is in <b>S4</b> state.</li> <li>4. Connect to SUT IP and port 16992 from Management console.</li> <li>5. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT.</li> <li>6. Disconnect Ethernet cable from SUT.</li> <li>7. Connect the dock to SUT using TypeC TBT cable.</li> <li>8. Connect to dock IP and port 16992 from Management Console.</li> <li>9. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using FXVL LAN in TBT dock.</li> <li>10. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li> <li>11. Disconnect dock from SUT.</li> <li>12. Connect Ethernet cable to SUT.</li> <li>13. Connect to SUT IP and port 16992 from Management console.</li> <li>14. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> <li>15. Return to S0 state using RCO command from WebUI.</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

#### 10.13.1.4 Wired Connectivity Check in S5 with Different TBT Dock States

<b>ID</b>	<b>AMT_103</b>			
<b>Title</b>	Wired connectivity check in S5 with different TBT dock states.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction.			
<b>Description</b>	This test checks the LAN connectivity and active BUS during S5 while dock is connected or not.			
<b>Objective</b>	Verify vPro system wire connection availability with or without TBT dock in S5 state.			
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. TBT dock should not be connected to SUT.</li> <li>5. Query SUT IP and TBT dock IP.</li> <li>6. Verify Ethernet cables are connected to SUT and TBT dock.</li> </ol>			



<b>ID</b>	<b>AMT_103</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li> <li>2. Select Windows-&gt;Power-&gt;Shutdown.</li> <li>3. Verify SUT is in <b>S5</b> state.</li> <li>4. Connect to SUT IP and port 16992 from Management console.</li> <li>5. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT.</li> <li>6. Disconnect Ethernet cable from SUT.</li> <li>7. Connect the dock to SUT using TypeC TBT cable.</li> <li>8. Connect to dock IP and port 16992 from Management Console.</li> <li>9. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using FXVL LAN in TBT dock.</li> <li>10. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li> <li>11. Disconnect dock from SUT.</li> <li>12. Connect Ethernet cable to SUT.</li> <li>13. Connect to SUT IP and port 16992 from Management console.</li> <li>14. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> <li>15. Power up machine using RCO command or from WebUI.</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

### 10.13.1.5 Wired Remote Power Control Transition Check with Different TBT Dock States

<b>ID</b>	<b>AMT_104</b>			
<b>Title</b>	Wired Remote Power Control Transition Check with different TBT dock states.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction.			
<b>Description</b>	This test preform remote power control transitions while the dock is connected and disconnected.			
<b>Objective</b>	Verify vPro system wire connection availability in different power transitions with or without TBT dock.			
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. TBT dock should not be connected to SUT.</li> <li>5. Query SUT IP and TBT dock IP.</li> <li>6. Verify Ethernet cables are connected to SUT and TBT dock.</li> </ol>			



<b>ID</b>	<b>AMT_104</b>
<b>Procedure</b>	<p><b>Test Power transitions with platform LAN:</b></p> <ol style="list-style-type: none"><li>1. Connect to SUT IP and port 16992 from Management console</li><li>2. Set the active power package on the SUT to Power Package 2 (Intel® ME on in S0, wake in Sx/AC).</li><li>3. In S0, query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>4. Select Windows-&gt;Power-&gt;<b>Sleep</b>.</li><li>5. Verify SUT is in <b>S3</b> state.</li><li>6. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>7. Return to S0 state.</li><li>8. Select Windows-&gt;Power-&gt;<b>Hibernate</b>.</li><li>9. Verify SUT is in <b>S4</b> state.</li><li>10. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>11. Return to S0 state by RCO command from WebUI.</li><li>12. Select Windows-&gt;Power-&gt;<b>Shutdown</b>.</li><li>13. Verify SUT is in <b>S5</b> state.</li><li>14. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>15. Return to S0 state by RCO command using WebUI.</li><li>16. Disconnect Ethernet cable from SUT.</li></ol> <p><b>Test Power transitions with TBT Dock (TBT Dock event):</b></p> <ol style="list-style-type: none"><li>17. Connect the dock to SUT using TypeC TBT cable.</li><li>18. Connect to dock IP and port 16992 from Management Console.</li><li>19. In S0, query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>20. Select Windows-&gt;Power-&gt;<b>Sleep</b>.</li><li>21. Verify SUT is in <b>S3</b> state.</li><li>22. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>23. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li><li>24. From WebUI or using RCO command, return to S0 state.</li><li>25. Select Windows-&gt;Power-&gt;<b>Hibernate</b>.</li><li>26. Verify SUT is in <b>S4</b> state.</li><li>27. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>28. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li><li>29. Return to S0 state by RCO command from WebUI.</li><li>30. Select Windows-&gt;Power-&gt;<b>Shutdown</b>.</li><li>31. Verify SUT is in <b>S5</b> state.</li><li>32. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li><li>33. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>SMBUS</b> BUS is active by checking if value matches to "<b>SMBUS</b>".</li><li>34. Return to S0 state by RCO command using WebUI</li></ol> <p><b>Test Power transitions with platform LAN (Un-dock event)</b></p> <ol style="list-style-type: none"><li>35. Disconnect dock from SUT.</li><li>36. Connect Ethernet cable to SUT.</li><li>37. Repeat steps 1-18.</li></ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

### 10.13.1.6 Placeholder



### 10.13.1.7 Wireless Connectivity Check with Connected TBT Dock

<b>ID</b>	<b>AMT_106</b>			
<b>Title</b>	Wireless connectivity check with connected TBT dock event.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction.			
<b>Description</b>	This test checks the LAN and Wireless connectivity and while dock is connected.			
<b>Objective</b>	Verify vPro system wire and wireless connection availability with TBT dock.			
<b>Setup</b>	1. The initial state of the SUT should be S0/MeOn with host OS running. 2. Intel® AMT should be provisioned via manual mode. 3. SUT power port should be connected to power supply. 4. TBT dock should not be connected to SUT. 5. Query SUT IP and TBT dock IP. 6. Verify Ethernet cable is disconnected from SUT and connected to TBT dock. 7. Refer to AMT_21 for additional AMT wireless setup steps.			
<b>Procedure</b>	1. Disconnect Ethernet cable from SUT 2. Connect the dock to SUT using TypeC TBT cable. 3. Connect to dock IP and port 16992 from Management Console. 4. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using discrete LAN in TBT dock. 5. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>PCIe</b> BUS is active by checking if value matches to " <b>PCIe</b> ". 6. Enable wireless in SUT and connect to wireless IP and port 16992 from Management Console while dock is connected.  <b>NOTE:</b> This is a new session in parallel to dock wired session. 7. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using wireless connectivity.			
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.			
<b>References</b>	N/A			

### 10.13.1.8 Wired IPV6 Connectivity Check in S0 with Different TBT Dock States

<b>ID</b>	<b>AMT_107</b>			
<b>Title</b>	Wired <b>IPV6</b> connectivity check in S0 with different TBT dock states.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> Either Used <input type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Manual.			
<b>Description</b>	This test checks the LAN connectivity using IPV6 and active BUS during S0 while dock is connected or not.			
<b>Objective</b>	Verify vPro system wire connection availability with or without TBT dock in S0 state.			



<b>ID</b>	<b>AMT_107</b>
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. TBT dock should not be connected to SUT.</li> <li>5. Verify Ethernet cables are connected to SUT and TBT dock.</li> <li>6. Enable IPV6 in DHCP server or router and make sure IPV6 is functional.</li> <li>7. Enable IPV6 in local WebUI <b>IPV6 Network Setting</b> screen.</li> <li>8. Verify <b>IPV6 Network Setting</b> contains 2 or 3 IPV6 addresses. Note: This indicates IPV6 address was allocated from DHCP server</li> <li>9. Run IPConfig to check IPV6 is configure properly.</li> <li>10. Run ping command to check IPV6 ping response.</li> <li>11. Query SUT IPV6 and TBT dock IP.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Connect to SUT IP (IPV6) and port 16992 from Management console.</li> <li>2. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>3. Verify SUT is in <b>S0</b> state.</li> <li>4. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT and IPV6 interface.</li> <li>5. Disconnect Ethernet cable to SUT.</li> <li>6. Connect the dock to SUT using TypeC TBT cable.</li> <li>7. Connect to dock IP (IPV6) and port 16992 from Management Console.</li> <li>8. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using FXVL LAN in TBT dock.</li> <li>9. Send WSMAN command to query CSME active bus interface and verify response contains indication of <b>PCIe</b> BUS is active by checking if value matches to <b>"PCIe"</b>.</li> <li>10. Disconnect dock from SUT.</li> <li>11. Connect Ethernet cable to SUT.</li> <li>12. Connect to SUT IP (IPV6) and port 16992 from Management console.</li> <li>13. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

### 10.13.1.9 Integrated/Discrete LAN Connectivity Check While Dock is Connected

<b>ID</b>	<b>AMT_108</b>			
<b>Title</b>	Integrated\Discrete LAN connectivity check while dock is connected.			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input checked="" type="checkbox"/> LAN <input type="checkbox"/> WLAN <input type="checkbox"/> Either Used <input type="checkbox"/> Not Used	<b>LAN Type</b> <input checked="" type="checkbox"/> Integrated LAN <input checked="" type="checkbox"/> Discrete LAN <input checked="" type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction.			
<b>Description</b>	This is negative test to verify platform LAN is not active while dock is connected.			
<b>Objective</b>	Verify vPro system wire connection is available only using the dock which it's connected.			
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. TBT dock should not be connected to SUT.</li> <li>5. Verify Ethernet cables are connected to SUT and TBT dock.</li> <li>6. Define DHCP server to allocate separate IP for SUT and dock.</li> <li>7. Query SUT IP and TBT dock IP.</li> </ol>			



<b>ID</b>	<b>AMT_108</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>2. Verify SUT is in <b>S0</b> state.</li> <li>3. Connect to SUT IP and port 16992 from Management console.</li> <li>4. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel.</li> </ol> <p><b>NOTE:</b> This step indicates successful connectivity using platform LAN in SUT.</p> <ol style="list-style-type: none"> <li>5. Connect the dock to SUT using TypeC TBT cable.</li> <li>6. Verify existing AMT session with platform LAN is no longer exist.</li> </ol> <p><b>NOTE:</b> In case dock and SUT has same IP, AMT connectivity should remains active.</p> <ol style="list-style-type: none"> <li>7. Try to connect to <b>SUT IP</b> and port 16992 from Management console.</li> <li>8. Verify connection failed.</li> </ol>
<b>Pass Criteria</b>	This test passes if each of the step above passed successfully.
<b>References</b>	N/A

### 10.13.1.10 Wireless Connectivity Check with Standard TBT Dock (Non vPro Support)

<b>ID</b>	<b>AMT_109</b>			
<b>Title</b>	Wireless connectivity check with TBT dock which doesn't support vPro			
<b>Requirement</b>	Mandatory.			
<b>System</b>	<b>Form Factor</b> <input type="checkbox"/> Desktop <input type="checkbox"/> Workstation <input checked="" type="checkbox"/> Mobile	<b>System Power Model</b> <input checked="" type="checkbox"/> Standard <input checked="" type="checkbox"/> Modern Standby or InstantGo*	<b>Intel® AMT Network Interface</b> <input type="checkbox"/> LAN <input type="checkbox"/> Either Used <input checked="" type="checkbox"/> WLAN <input type="checkbox"/> Not Used	<b>LAN Type</b> <input type="checkbox"/> Integrated LAN <input type="checkbox"/> Discrete LAN <input type="checkbox"/> TBT Dock LAN
<b>Method</b>	Automated by Intel® PETS with test operator interaction.			
<b>Description</b>	This is negative test to verify integrated LAN is not active while dock is connected.			
<b>Objective</b>	Verify vPro system wire connection is available only using the dock which it's connected.			
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. The initial state of the SUT should be S0/MeOn with host OS running.</li> <li>2. Intel® AMT should be provisioned via manual mode.</li> <li>3. SUT power port should be connected to power supply.</li> <li>4. <b>Regular TBT dock (non vPro support)</b> should not be connected to SUT.</li> <li>5. Verify Ethernet cables are connected to SUT and TBT dock.</li> <li>6. Query SUT IP and TBT dock IP.</li> <li>7. Enable AMT wireless, refer to AMT_21 setup section for details steps.</li> </ol>			
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to Power Package 1 (Intel® ME on in S0).</li> <li>2. Verify SUT is in <b>S0</b> state.</li> <li>3. Connect to SUT IP and port 16992 from Management console.</li> <li>4. Query Intel ME firmware version using WSMAN command or using WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT.</li> <li>5. Connect the <b>Regular TBT dock (non vPro support)</b> to SUT using TypeC TBT cable.</li> <li>6. Disconnect Ethernet cable from SUT.</li> <li>7. Enable AMT wireless connectivity</li> <li>8. Connect to wireless IP and port 16992 from Management console while dock is connected.</li> <li>9. Query Intel ME firmware version using WSMAN command or using wireless WebUI, "System Status", Intel AMT FW version in lower panel. Note: This step indicates successful connectivity using integrated LAN in SUT.</li> <li>10. Disconnect TBT Dock from SUT.</li> <li>11. Connect Ethernet cable to SUT.</li> <li>12. Connect to SUT IP and port 16992 from Management console.</li> <li>13. Query Intel ME firmware version using WSMAN command or using wired WebUI, "System Status", Intel AMT FW version in lower panel.</li> </ol> <p><b>NOTE:</b> This step indicates successful connectivity using integrated LAN in SUT.</p>			



ID	AMT_109
Pass Criteria	This test passes if each of the step above passed successfully.
References	N/A

### 10.13.2 Intel® AMT Over Thunderbolt™ Dock with Discrete SUT LAN

Refer to AMT Over Thunderbolt™ Dock with SUT Integrated LAN paragraph for test list to run.

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# 11 Intel® CSME Power Management for Corporate Designs

This chapter covers system power flow transitions, which involve the Intel® ME firmware (and/or software). Test coverage for Intel® Active Management Technology (Intel® AMT), as an application within in the Intel® ME firmware, related configurations and flows found in Corporate designs are also included herein.

## 11.1 System Power States

The following section describes power states that exist beyond the standard ACPI System Level Sx (S0, S3, S4, and S5) system S-states.

### 11.1.1 Deep S4/S5 Support

To minimize power consumption in S4/S5, the PCH supports a lower power version of these power states known as Deep S4/S5. In these states, Deep S4 and Deep S5, the suspend well is powered off, while the Deep S4/S5 Well (DSW) remains powered. A limited set of wake events are supported by the logic located in the DSW. The Deep S4/S5 capability and the SUSPWRDNACK pin functionality are mutually exclusive.

Deep S4/S5 feature can be enabled/disabled by means of the Intel® FIT. Beyond this, a combination of conditions is required for entry into Deep S4/S5. All of the following must be met: Intel® ME must be in CM-Off AND either a OR b as defined below:

- ((DPS4\_EN\_AC AND S4) OR (DPS5\_EN\_AC AND S5)) (desktop only)
- ((AC\_PRESENT = 0) AND ((DPS4\_EN\_DC AND S4) OR (DPS5\_EN\_DC AND S5)))

How to enable DSX in softstrap - **Deep SX Enable = true** in PCHSTRP10

**Table 11-1. Supported Deep S4/S5 Policy Configurations**

Configuration	DPS4_EN_DC	DPS4_EN_AC	DPS5_EN_DC	DPS5_EN_AC
Enabled in S5 when on Battery (ACPRESENT = 0)	0	0	1	0
Enabled in S5 (ACPRESENT not considered) (Desktop only)	0	0	1	1
Enabled in S4 and S5 when on Battery (ACPRESENT = 0)	1	0	1	0
Enabled in S4 and S5 (ACPRESENT not considered) (Desktop only)	1	1	1	1
Deep S4/S5 disabled	0	0	0	0



The PCH initiates DeepSx entry in Sx/CM-Off state upon sensing that all of the above conditions are satisfied. The PCH asserts SUSWARN# as notification that it is about to enter Deep S4/S5. Before the PCH proceeds and asserts SLP\_SUS#, the PCH waits for SUSACK# to assert.

**Note:** CNVI does not support wake on WLAN/BT\* during deep system sleep states (DSx).

#### 11.1.1.1 Exit from Deep S4/S5

While in Deep S4/S5, the PCH monitors and responds to a limited set of wake events (RTC Alarm, Power Button, and GPIO27). Upon sensing an enabled Deep S4/S5 wake event, the PCH brings up the Suspend well by de-asserting SLP\_SUS#.

#### 11.1.2 Intel® ME Power Gating

Intel® ME firmware enters power gated state (CM0-PG), when the firmware is idle and system state is either S0 or S0ix. Intel® ME firmware exits CM0-PG state to process power management events on the system and when host applications require Intel® ME firmware services. When the Intel® ME is in CM3 state, after Intel® AMT idle timeout, Intel® ME will enter CM3-PG state.

Intel® ME Power Gating feature is available only, when the following conditions are satisfied:

- Intel® ME Power Gating feature supported, when the platform is in S0 state. In this case, Intel® ME may enter power gated state (CM0-PG), when the firmware reaches idle state.
- Intel® ME Power Gating feature supported, when the platform is in Sx state. In this case, Intel® ME is in CM3 state, after Intel® AMT idle timeout expiration, Intel® ME will enter CM3-PG state.

**Table 11-2. Supporting Intel® ME Power Gating with AMT, LAN**

Intel® ME Power Gating is supported	AMT Provisioned	AMT Unprovisioned
LAN connected	Supported	Supported
LAN disconnected	Supported	Supported

**Note:** If the machine is configured to operate in Modern Standby or Microsoft\* Windows InstantGo, all S3 tests are not relevant, and should be replaced with the CM0-PG tests.

## 11.2 Test Environment and System Configuration

Each test in this chapter contains a section outlining the test configuration.

Unless where stated otherwise, Intel® AMT should be provisioned.

The Intel® AMT networking interface used by the test, if any, is documented in the test configuration section as well. 'LAN' and 'WLAN' indicate that the test is explicitly using the respective LAN and/or wireless LAN (WLAN) interface. Some tests may have a combination of targeted network configurations. Example: WLAN-only and/or LAN+WLAN.

The test should be run on the SUT only in the case, where a matching network configuration is described.



**Note:** Not all Workstation and Intel® AMT Server designs may have Intel® AMT wireless LAN interface support.

Other details about the configuration of the SUT are described on a per-test basis. Refer the test contents for details.

### 11.2.1 Test Parameters

Each test in this chapter contains a table describing the system configuration to which the test is applicable. Below are some example test parameters blocks:

**Example 1: Two-state with Single Trigger**

<b>System Power Source</b>		AC+DC or AC-only
<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
	<b>Final</b>	S0/MeOn (CM0, CM0-PG)
	<b>Trigger</b>	Remote Power Cycle
<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
	<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available

**Example 2: Three-state with Double Trigger**

<b>System Power Source</b>		AC+DC or AC-only
<b>Power States</b>	<b>Initial</b>	S5/MeOn (CM3)
	<b>Middle</b>	G3/MeOff (CM-Off)
	<b>Final</b>	S5/MeOn (CM3)
	<b>Trigger</b>	Power loss → Power attach
<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
	<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available

**System Power Source:** Describes the initial power source configuration of the system. Can be one of 'AC-only', 'DC-only', 'AC+DC', 'AC+DC,AC-only' (AC+DC or AC-only). The system may transition to different power source configurations during the test.

**Power States:** Describes the 'Initial', 'Middle' (where applicable), and 'Final' power states of the SUT. The description is provided in terms of basic ACPI Sx states (S0, S3, S4, S5, G3) as well as Intel® ME availability ('MeOn' or 'MeOff'). Exact detail of system power states, including Deep Sx and/or Intel® ME power gating availability, is provided in each test. Included is also the 'Trigger' used to initiate the power flow transition. Many tests are limited one trigger, but some tests have two.

**Intel® AMT:** Describes the 'Power Package' and 'WLAN Link Policy' (where available and applicable) that apply to the test. The Power Package controls, when manageability is available on the SUT and what power states the SUT and particularly the Intel® ME may transition to and from. The WLAN Link Policy describes, relative to Wireless LAN support, when manageability is available via Intel® AMT Wireless Networking support.

### 11.2.2 Tools for Testing

The following tools, as provided by Intel, may be used to execute automated tests listed herein:

- Intel® PETS: The latest version of the tool from the Intel® ME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.



- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.

### 11.2.3 Test Environment Setup

The SUT is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft® Windows supported by Intel® PETS, and the SUT should have a version of Microsoft® Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one HDD.

While completing tests within this chapter, especially those which send the system to a specific S-state (S3, S4, S5, Deep Sx, and so forth), it is important to ensure that the network wake events are properly configured for each applicable device (LAN and/or WLAN).

If not properly configured, the system may wake from a given S-state unexpectedly during test execution as a result of various network traffic within the test environment, and cause the test to result in a *false failure*.

The following Host OS LAN/WLAN driver settings allow the network device to process specific network frames **without** waking the system, where supported.

- Address Resolution Protocol (ARP) offload should be **enabled**.
- Neighbor Solicitation (NS) offload should be **enabled**.

The following Host OS LAN/WLAN driver settings allow the network device to wake the system, where supported, when specific network frames are received.

- Wake on Magic Packet should be **disabled**.
- Wake on Pattern Match should be **disabled**.
- Wake on Magic Packet from power off state should be **disabled**.

**Note:**

The word used for the Host OS driver settings above may vary, and in some cases may not be available depending on driver support or system configuration.

Beyond the guidance in this section, refer individual test setup information for details on specifically, when to enable relevant wake functionality in the network device, as applicable to the test. In all other cases, the above settings should be applied by default.

The following additional checkpoints are recommended before Intel® ME firmware Power Management testing:

- Install all platform drivers (Chipset, Graphics, LAN, WLAN, Intel® MEI, LMS\_SOL).
- Client platform OS can be Windows® 10.
- For wired LAN network use a hub/switch and network cables.
- Wireless setup:
  - Wireless card should be installed.
  - Setup an active wireless profile.
- LAN and WLAN interfaces should be setup on different subnets.
- For Global reset tests to pass (ME\_PM\_18), the SUT should be in manufacturing mode.



**Note:** Intel® ME FWSTS values are updated except for test cases, which have Power Gating (PG) validation and Deep Sx enabled.

Following test step has been added to Power Flows, which ends at S0 state resuming back from S4 Hibernation. This helps to ensure System resumed from S4 state only and no other Sx state.

Verify that Windows\* booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10|where-Object {\$\_.message -like "The Boot type\*"}

## 11.2.4 Test Step Execution and Verification

The tests described in this chapter contain test steps, which are executed by Intel® PETS. While, Intel® PETS brings a certain level of convenience and speed to the testing process, there are times where manual verification of steps are critical toward issue triage and debug.

The following is a list of non-trivial test steps and a description of how they may be manually executed. The list assumes that the test operator has access to information available in the PCH External Design Specification (EDS), and the Intel® AMT SDK.

1. Set the active power package on the SUT to **Power Package 1** (Intel® ME in S0).

- a. Log into the WebUI via the SUT at [http://<ip\\_address>:16992/](http://<ip_address>:16992/) to view and manually change the Power Policy therein.
- b. To configure the Intel® AMT power package to PP1, run the following command from the Management Console:

Mobile

```
$> PowerPackage.exe -applyguid djmXEQtWUEOIcJgS85G1YA== -host <ip_address> -user <user> -pass <password>
```

Desktop

```
$> PowerPackage.exe -applyguid IE+DEvsQT9yWjh4jKwyQZQ== -host <ip_address> -user <user> -pass <password>
```

Upon successful execution, the Intel® AMT firmware active power package will be returned. The PowerPackage application is located in the Intel® AMT SDK.

2. Set the active power package on the SUT to **Power Package 2** (Intel® ME in S0, wake in Sx/AC).

- a. Log into the WebUI via the SUT at [http://<ip\\_address>:16992/](http://<ip_address>:16992/) to view and manually change the Power Policy therein.
- b. To configure the Intel® AMT power package to PP2, run the following command from the Management Console:

Mobile

```
$> PowerPackage.exe -applyguid MIAN7gnAeEOvKHhootu+Og== -host <ip_address> -user <user> -pass <password>
```

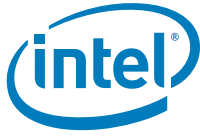
Desktop

```
$> PowerPackage.exe -applyguid cyJzRiPcQy+pihPTeYLYVQ== -host <ip_address> -user <user> -pass <password>
```

Upon successful execution, the Intel® AMT firmware active power package will be returned. The PowerPackage application is located in the Intel® AMT SDK.

3. Set the Intel® AMT WLAN link policy on the SUT to Link Policy [1,2,3].

- a. Log into the WebUI via the SUT at [http://<ip\\_address>:16992/](http://<ip_address>:16992/) and manually change the Link Policy via the Wireless Settings screen therein.



4. Send three magic packets, at **2 second** intervals, by means of the [active,LAN] network interface.
  - a. Sending magic packets is supported by various tools and utilities available on the Internet.
5. Ensure the Intel® AMT idle timeout on the SUT is set to **1 minute**.
  - a. The following command may be used to set the Intel® AMT idle timeout on the SUT from the Management Console:  

```
$> PowerPackage.exe -setidletimeout 1 -host <ip_address> -user <user> -pass <password>
```

Upon successful execution, the Intel® AMT idle timeout will be set. The `getidletimeout` command line option may be used to confirm the setting. The PowerPackage application is located in the Intel® AMT SDK.
6. Ensure that CF9h Global Reset (CF9GR) is [set,cleared].
  - a. CF9GR bit is located at 0xFE001048 (BIT20) in PMC PWRM space on TGL. Confirm that CF9 Global Reset (CF9GR) bit 20 is set to 1b (set) or 0b (clear). Information describing how to access this value may be found in the PCH EDS.

The following is a list of commonly used test steps and a description of how they may be manually verified. The list assumes that the test operator has access to information available in the PCH External Design Specification (EDS), Platform Design Guide (PDG), PCH BIOS Specification, the Intel® AMT SDK, as well as power management related signals (as described by the Intel® APS header found in the PDG) on the SUT.



1. Confirm that the BIOS has **not set** the CF9 Lockdown.
  - a. CF9GR bit is located at 0xFE001048 (BIT20) in PMC PWRM space on TGL and confirm that CF9 Lockdown (CF9LOCK) bit 31 is set to **0b**. Information describing how to access this value may be found in the PCH EDS.
2. Verify that Intel® AMT on the SUT responds to version query via the [LAN,WLAN,active,any] network interface.
  - a. For a given network interface for which Intel® AMT should be responsive, the following command may be used to confirm connectivity from the Management Console:  

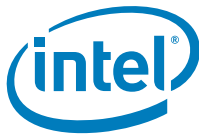
```
$> GeneralInfo.exe -host <ip_address> -user <user> -pass <password> -CoreVersion
```

 Upon successful execution, the Intel® AMT firmware core version will be returned. The GeneralInfo application is located in the Intel® AMT SDK.
3. Verify that the SUT is in S0.
  - a. Confirm that signals SLP\_S3#, SLP\_S4#, and SLP\_S5# are all de-asserted (high) for at least 5 seconds.
4. Verify that the SUT is in Sx[,Deep Sx]/Me[On/Off] (CMx[-PG]).
  - a. Confirm that signals and power rails are asserted (low)/de-asserted (high) or powered/off respectively for the associated SUT state for at least **5 seconds**:

State	SLP_S3#	SLP_S4#	SLP_S5#	SLP_A#	VccSUS3_3	VccDSW3_3
<b>S0</b>	1	1	1	N/A	Powered	Powered
<b>S3</b>	0	1	1	N/A	Powered	Powered
<b>S4</b>	0	0	1	N/A	Powered	Powered
<b>S5</b>	0	0	0	N/A	Powered	Powered
<b>MeOn</b>	N/A	N/A	N/A	1	Powered	Powered
<b>MeOff</b>	N/A	N/A	N/A	0	Powered	Powered
<b>Deep S4</b>	0	0	1	0	Off	Powered
<b>Deep S5</b>	0	0	0	0	Off	Powered
<b>G3</b>	0	0	0	0	Off	Off

**Note:** VccSUS3\_3 is also referred to as VCCPRIM\_3p3 in the PCH EDS and PDG. Similarly, VccDSW3\_3 is also referred to as VCCDSW\_3p3 as well. The labels VccSUS3\_3 and VccDSW3\_3 are listed in the table above to assist test operators identification of the corresponding signals (as silk-screened) on their Intel® APS adapter (refer the PDG for details).

- b. In S0, the CM0-PG and CM0 Intel® ME 'MeOn' states will appear the same in the table above. Follow the procedure below via the Host OS on the SUT to confirm, if the Intel® ME is Power Gated (CM0-PG):
  - i. Get the Intel® CSME PG value by reading PPFEAR0 (n=0,1). Information describing how to access this value may be found in either the PCH EDS or the PCH BIOS Specification.
  - ii. Read 8 bytes at 0xfe001d93 and 0xfe001d94 and verify these bits 15:0 equal FFh.
    - The above fields include non-CSME IP status, BIT25,26 are not part of CSME PG values. So, if user finds 0xF9 at 0xFE001D93, then it is acceptable as per PG test case.
- c. In S3, S4, or S5, the CM3-PG and CM-Off Intel® ME 'MeOff' states will appear the same in the table above. The Intel® ME may enter CM3-PG (supporting wake) upon Intel® AMT idle timeout, when the Intel® AMT Power Policy configuration is set to PP2 (Intel® ME on in S0, wake in Sx/AC).



**Caution:** When using Intel® PETS to verify the power state of the SUT, it is critical to ensure that the Advanced Power Settings configuration in the SUT profile is correctly set. Failure to set the correct policy configuration supported by the SUT may lead to false test results or incomplete evaluation. Refer the Intel® PETS User Guide for further details.

5. Verify that the SUT is in G3/MeOff (CM-Off).
  - a. Confirm that signals SLP\_S3#, SLP\_S4#, SLP\_S5#, and SLP\_A# are asserted low. Additionally, VccSus3\_3 (and VccDSW3\_3 for systems supporting Deep Sx) should be powered off.
  - b. The signal and power rail state should remain stable for at least **5 seconds**. Furthermore, measurements should not be taken for at least **10 seconds** after state transition to allow full electric dissipation from the system.
6. Verify that the Host OS on the SUT is available.
  - a. A connection test with the Intel® PETS Local Agent service on the SUT can be used to confirm that the Host OS is available remotely from the Management Console:  

```
$> PsService.exe \\<ip_address> -u <user> -pass <password> query PeTSLocalAgent
```

Upon successful execution, the Intel® PETS Local Agent status should be displayed. The PsService tools is available from Microsoft\* Windows Sysinternals website.
7. Verify that the Intel® ME on the SUT is on.
  - a. Confirm that the SLP\_A# signal is de-asserted (high) for at least **5 seconds**.
8. Verify that the Intel® ME on the SUT is off.
  - a. Confirm that the SLP\_A# signal is asserted (low) for at least **5 seconds**.
9. Verify that the Intel® ME is configured in manufacturing mode.
  - a. The manufacturing mode status is available by querying the Intel® ME firmware status bits via the MEInfo tool on the SUT. The following example shows tool usage in a UEFI shell:  

```
$> MEInfo.efi -fwsts
```

Upon successful execution, the Intel® ME Manufacturing Mode status should read "Enabled". The MEInfo tool is available from Intel via the Intel® ME firmware kit.
10. Verify that a DC battery is connected to the SUT, and that it is charged.
  - a. The battery information on SUT can be queried via the Microsoft\* Windows Management Instrumentation Command (WMIC) tool.  

```
$> WMIC PATH Win32_Battery Get EstimatedChargeRemaining
```
  - b. It is recommended that tests in this chapter can run not less than **30%** battery charge. More information about the WMIC is available from Microsoft\*, including how to connect remotely and perform queries via various command-line switches.

## 11.2.5 Setup Environment Tests

The following tests are defined as Setup Environment Test (SET) tests. These are intended to confirm basic test environment configuration and should run before any other automated test described in this chapter.





Because Intel® AMT is provisioned in many of the tests in this chapter, it is strongly recommended to run the Setup Environment Tests for that technology as well before running any test in this chapter.

ID	Check S3		
<b>Title</b>	S0/CM0 to S3/CM3 to S0/CM0 via Host OS suspend cycle (AC-only/PP2)		
<b>Requirement</b>	Optional	<b>Non-Support</b>	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM3 to S0/CM0 via Host OS suspend cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode.		
<b>Parameters</b>	<b>System Power Source</b>		AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Middle</b>	S3/MeOn (CM3)
		<b>Final</b>	S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b>	Host OS suspend ➡ Power Button press
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	[Not applicable.]
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves to S3 and then to S0, and the Intel® ME is in MeOn (CM0, CM0-PG).		

ID	Check S4		
<b>Title</b>	S0/CM0 to S4/CM3 to S0/CM0 via Host OS hibernate cycle (AC-only/PP2)		
<b>Requirement</b>	Optional		
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM3 to S0/CM0 via Host OS hibernate cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode.		
<b>Parameters</b>	<b>System Power Source</b>		AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Middle</b>	S4,S5/MeOn (CM3)
		<b>Final</b>	S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b>	Host OS hibernate ➡ Power Button press
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	[Not applicable.]



ID	Check S4
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>4. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Hibernate the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>3. Briefly press the Power Button on the SUT.</li> <li>4. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> </ol>
<b>Pass Criteria</b>	The test passes, if the SUT moves to S4 and then to S0, and the Intel® ME is in MeOn (CM0, CM0-PG).

ID	Check S5		
<b>Title</b>	S0/CM0 to S5/CM3 to S0/CM0 via Host OS shutdown cycle (AC-only/PP2)		
<b>Requirement</b>	Optional		
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S5/CM3 to S0/CM0 via Host OS shutdown cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode.		
<b>Parameters</b>	<b>System Power Source</b>		AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Middle</b>	S5/MeOn (CM3)
		<b>Final</b>	S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b>	Host OS shutdown ➡ Power Button press
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	[Not applicable.]
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>4. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Shutdown the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S5/MeOn (CM3).</li> <li>3. Briefly press the Power Button on the SUT.</li> <li>4. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves to S5 and then to S0, and the Intel® ME is in MeOn (CM0, CM0-PG).		
ID	Check Deep S4		
<b>Title</b>	S0/CM0 to S4/CM-Off to S0/CM0 via Host OS hibernate cycle (AC, DC)		
<b>Requirement</b>	Optional <b>Non-Support</b>   <input checked="" type="checkbox"/> Systems not supporting Deep S4		
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via Host OS hibernate cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. If Deep S4 is supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>• The SUT and/or BIOS are properly configured to permit Deep S4 entry.</li> <li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul>		



ID	Check Deep S4		
Parameters	System Power Source		AC, DC
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Middle	Deep S4/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Host OS hibernate ➡ Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	[Not applicable.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source based on <b>Deep Sx policy</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Request the test operator to confirm the SUT is properly configured to enter Deep S4 upon Host OS hibernate.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in Deep S4/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to Deep S4 and then to S0, and the Intel® ME is in MeOn (CM0, CM0-PG).		

ID	Check Deep S5		
Title	S0/CM0 to S5/CM-Off to S0/CM0 via Host OS shutdown cycle (AC, DC)		
Requirement	Optional	Non-Support	☑ Systems not supporting Deep S5
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via Host OS shutdown cycle with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S5 is supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul>		
Parameters	System Power Source		AC, DC
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Middle	Deep S5/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Host OS shutdown ➡ Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	[Not applicable.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source based on <b>Deep Sx policy</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Request the test operator to confirm the SUT is properly configured to enter Deep S5 upon Host OS shutdown.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in Deep S5/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to Deep S5 and then to S0, and the Intel® ME is in MeOn (CM0, CM0-PG).		



ID	Check Intel® ME		
<b>Title</b>	S0/CM0 to S5/CM-Off to S0/CM0 via Host OS shutdown cycle (AC-only/PP1)		
<b>Requirement</b>	Optional		
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S5/CM3 to S0/CM0 via Host OS shutdown cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul>		
<b>Parameters</b>	<b>System Power Source</b>		AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Middle</b>	S5/MeOn (CM3)
		<b>Final</b>	S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b>	Host OS shutdown → Power Button press
	<b>Intel® AMT</b>	<b>Power Package</b>	PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b>	[Not applicable.]
<b>Setup</b>	1. Set the SUT power source to <b>AC-only</b> . 2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available. 3. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0). 4. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.		
<b>Procedure</b>	1. Shutdown the SUT via the Host OS. 2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off). 3. Briefly press the Power Button on the SUT. 4. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).		
<b>Pass Criteria</b>	The test passes, if the SUT moves to S5 (or Deep S5 or G3) and then to S0, and the Intel® ME is in MeOff (CM-Off) when the SUT is in S5 (or Deep S5 or G3).		

ID	Check DC Power		
<b>Title</b>	Check DC power connectivity to the SUT (AC+DC)		
<b>Requirement</b>	Optional <b>Non-Support</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems		
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from AC+DC to DC-only with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b>	AC-detach
	<b>Intel® AMT</b>	<b>Power Package</b>	[Not applicable.]
		<b>WLAN Link Policy</b>	[Not applicable.]
<b>Setup</b>	1. Set the SUT power source to <b>AC+DC</b> . 2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.		
<b>Procedure</b>	1. Set the SUT power source to <b>DC-only</b> . 2. Wait <b>5 seconds</b> before proceeding to allow the test environment to stabilize. 3. Verify that the SUT is operating on DC-only power.		
<b>Pass Criteria</b>	The test passes, if the SUT moves from AC+DC power to DC-only power.		



ID	Check AC Power		
<b>Title</b>	Check AC power connectivity to the SUT (AC+DC, AC-only)		
<b>Requirement</b>	Optional		
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from AC+DC to AC-only with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b>	DC-detach where available
	<b>Intel® AMT</b>	<b>Power Package</b>	[Not applicable.]
		<b>WLAN Link Policy</b>	[Not applicable.]
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC-only</b>.</li> <li>Wait <b>5 seconds</b> before proceeding to allow the test environment to stabilize.</li> <li>Verify that the SUT is operating on AC-only power.</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves from AC+DC power to AC-only power.		

ID	Check G3 State		
<b>Title</b>	S0/CM0 to G3/CM-Off via Power loss (AC+DC, AC-only/PP1)		
<b>Requirement</b>	Optional		
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to G3/CM-Off via Power loss with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul>		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	G3/MeOff (CM-Off)
		<b>Trigger</b>	Power loss
	<b>Intel® AMT</b>	<b>Power Package</b>	PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b>	[Not applicable.]
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves to G3, and the Intel® ME moves to MeOff (CM-Off).		



## 11.3 Intel® ME Power Management Test Coverage Summary

### Test Requirements:

In general, all **applicable** tests are considered Mandatory in this section except for those specifically described as Optional or those, which meet an Exemption. Refer the test Requirement section for details on test applicability.

### Form Factor:

Mobile designs are most broadly covered by the tests in this chapter, Desktop, All-in-One, and Workstation designs are Exempted, where classified as Non-Mobile (AC-only) systems. Refer the test Requirement section for Exemption details.

### System Power Model:

Tests which involve S3 flows will not support Modern Standby or Microsoft\* Windows InstantGo. Refer the test Requirement section for Exemption details.

### Network Configuration:

In general, all tests may be run on systems with any combination of LAN and/or WLAN network interface support. For tests that work with a subset of configurations, like LAN-only or LAN+WLAN, refer the test Configuration section for details.

Test ID	Test Case Title	Test Method
ME_PM_1	S0/CM0 to S3/CM-Off	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_2	S0/CM0 to S3/CM-Off	Intel® PETS Package: Compliance_Power_G3-S5.xml Compliance_Power_Network_Wake.xml
ME_PM_3	S0/CM0 to S3/CM3	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_4	S3/CM3 to S0/CM0	Intel® PETS Package: Compliance_Power_G3-S5.xml Compliance_Power_Network_Wake.xml
ME_PM_5	S3/CM3 to S3/CM-Off (without Intel® ME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_6	S3/CM3 to S3/CM-Off (with Intel® CSME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_7	S3/CM-Off to S3/CM3	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_8	S0/CM0 to S3/CM-Off	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_9	G3 or S4-S5/CM-Off (Suspend Well Off) to S0/CM0	Intel® PETS Package: Compliance_Power_G3-S0.xml
ME_PM_10	S4/CM-Off (Suspend Well On) to S0/CM0	Intel® PETS Package: Compliance_Power_G3-S5.xml Compliance_Power_Network_Wake.xml
ME_PM_11	S0/CM0 to S4,S5/CM3	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_12	S4-S5/CM3 to S0/CM0	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_13	S4-S5/CM3 to S4-S5/CM-Off (without Intel® CSME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_14	S4-S5/CM3 to S4-S5/CM-Off (with Intel® CSME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_15	G3 or S4-S5/CM-Off (Suspend Well Off) to S4-S5/CM3	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_16	S4-S5/CM-Off (Suspend Well On) to S4-S5/CM3	Intel® PETS Package: Compliance_Power_G3-S5.xml



Test ID	Test Case Title	Test Method
ME_PM_17	Cold Reset	Intel® PETS Package: Compliance_Power_RST.xml
ME_PM_18	Global Reset	Intel® PETS Package: Compliance_Power_RST.xml
ME_PM_19	Straight-to-S5, Intel® ME Power Policy is S0 Only	Intel® PETS Package: Compliance_Power_G3-S5.xml Compliance_Power_RST.xml
ME_PM_20	Straight-to-S5 via Power Button Override	Intel® PETS Package: Compliance_Power_G3-S5.xml Compliance_Power_RST.xml
ME_PM_21	S3/CM-Off (w/ Intel® CSME Wake) to S3/CM-Off (w/o Intel® CSME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_22	S3/CM3-PG (w/ Intel® CSME Wake) to S3/CM-Off (w/o Intel® CSME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_23	G3 or S4-S5/CM-Off (w/o Intel® CSME Wake) to S4-S5/CM-Off (w/ Intel® CSME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_24	S4-S5/CM-Off (w/ Intel® CSME Wake) to S4-S5/CM-Off (w/o Intel® CSME Wake)	Intel® PETS Package: Compliance_Power_G3-S5.xml
ME_PM_25	S4-S5/CM-Off (Suspend Well Off) to S4-S5/CM-Off (w/ Host WoL) to S0/CM0 via Host WoL/WoWLAN	Intel® PETS Package: Compliance_Power_Network_Wake.xml
ME_PM_26	Warm Reset	Intel® PETS Package: Compliance_Power_G3-S5.xml Compliance_Power_RST.xml
ME_PM_27	S0/CM0 or Sx/Mx to G3	Intel® PETS Package: Compliance_Power_RST.xml
ME_PM_44	S0/CM0-PG, CM0 to S4-S5/CM-Off	Intel® PETS Package: Compliance_ME_Power_Gating.xml
ME_PM_45	G3 or S4-S5/CM-Off to S0/CM0_PG, CM0	Intel® PETS Package: Compliance_ME_Power_Gating.xml Compliance_ME_Power_Gating_Network_Wake.xml
ME_PM_46	S0/CM0-PG, CM0 to S0/CM0-PG, CM0	Intel® PETS Package: Compliance_ME_Power_Gating.xml Compliance_Power_RST.xml
ME_PM_50	S0/CM0 to Sx (Cm3 or CM-Off) to S0/CM0 via AC Attach	Intel (R) PETS Package: Compliance_Power_G3-S5.xml Compliance_Power_G3-S5_UnProvision.xml
ME_PM_51	S0/CM0 to Sx/CM-Off to S0/CM0 via AC Detach in Sx State	Intel (R) PETS Package: Compliance_Power_G3-S5.xml

**Notes:**

- All the tests, which use wake on LAN (WOL) as a trigger require SUSPEND well (SUS well) to be powered up. Hence platforms, which implement and support DeepSx cannot run WOL tests. PETS will include all the WOL tests under a single package named Compliance\_Power\_WOL.xml.
- Some tests defined in this chapter perform a non-graceful system shutdown or restart. In cases, where the Host OS used on the SUT during the test is Microsoft\* Windows, the test may cause the Host OS to enter into recovery mode due to non-graceful power state transition. **Test operators should be aware of the Host OS boot state during these tests to avoid impact to the Host OS on the SUT or invalid test result collection.** The following is a list of tests, which may have impact on subsequent Host OS boot: ME\_PM\_17.6, ME\_PM\_18.1 through ME\_PM\_18.4, ME\_PM\_19.1/2, ME\_PM\_20.1/2, ME\_PM\_20.21, ME\_PM\_26.5 through ME\_PM\_26.8, ME\_PM\_26.13, ME\_PM\_27.1/2, and ME\_PM\_46.3 through ME\_PM\_46.6.

## 11.4 ME\_PM\_1 - S0/CM0 to S3/CM-Off

ID	ME_PM_1.1
Title	S0/CM0 to S3/CM-Off via Host OS suspend (DC-only/PP1/LP3)



ID	ME_PM_1.1		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM-Off via Host OS suspend with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S3/MeOff (CM-Off)
		Trigger	Host OS suspend
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</div> <div>8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div>		
Procedure	<div>1. Suspend the SUT via the Host OS.</div> <div>2. Verify that the SUT is in S3/MeOff (CM-Off).</div>		
Pass Criteria	The test passes, if the SUT moves to S3 and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_1.2		
Title	S0/CM0 to S3/CM-Off via Host OS suspend (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM-Off via Host OS suspend with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S3/MeOff (CM-Off)
		Trigger	Host OS suspend
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available





ID	ME_PM_1.2
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> </ol>
<b>Pass Criteria</b>	The test passes, if the SUT moves to S3 and the Intel® ME moves to MeOff (CM-Off).

ID	ME_PM_1.3		
Title	S0/CM0 to S3/CM3-PG with AC Wake via Host OS suspend (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM3-PGwith AC Wake via Host OS suspend with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S3/CM3-PG
		Trigger	Host OS suspend
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</div> <div>8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div>		
Procedure	<div>1. Suspend the SUT via the Host OS.</div> <div>2. Verify that the SUT is in S3/(CM3-PG)</div>		
Pass Criteria	The test passes, if the SUT moves to S3 and the Intel® ME moves to CM3-PG.		



## 11.5 ME\_PM\_2 - S3/CM-Off to S0/CM0

ID	ME_PM_2.1		
Title	S3/CM-Off to S0/CM0 via magic packet (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM-Off to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li><li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>Ensure that, where available, <b>only</b> the Host OS Wake on LAN and/or Wake on Wireless LAN driver setting(s) are <b>enabled</b> on the SUT. All other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to help prevent unexpected host wake events.</li><li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager</li></ol>		
Procedure	<ol style="list-style-type: none"><li>Suspend the SUT via the Host OS.</li><li>Verify that the SUT is in S3/MeOff (CM-Off).</li><li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li><li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>Verify that the Host OS on the SUT is available.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li><li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager</li></ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"><li>The SUT moves from S3 to S0.</li><li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li><li>Intel® AMT responds to version queries via all available network interfaces.</li><li>The Host OS last boot time has not changed.</li></ul>		

ID	ME_PM_2.2
Title	S3/CM-Off to S0/CM0 via Power Button press (DC-only/PP1/LP3)



ID	ME_PM_2.2		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
			<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM-Off to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</div> <div>8. Record the Host OS last boot time on the SUT (to verify successful return from S3).</div> <div>9. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>10. Ensure yellow bang is not seen on Drivers in Device Manager</div> <div>11. Suspend the SUT via the Host OS.</div> <div>12. Verify that the SUT is in S3/MeOff (CM-Off).</div>		
Procedure	<div>1. Briefly press the Power Button on the SUT.</div> <div>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div> <div>3. Verify that the Host OS on the SUT is available.</div> <div>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>5. Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</div> <div>6. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</div> <div>7. Ensure yellow bang is not seen on Drivers in Device Manager</div>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"><li>The SUT moves from S3 to S0.</li><li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li><li>Intel® AMT responds to version queries via all available network interfaces.</li><li>The Host OS last boot time has not changed.</li></ul>		

ID	ME_PM_2.3		
Title	S3/CM-Off to S0/CM0 via Power Button press (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM-Off to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		



ID	ME_PM_2.3		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>		

ID	ME_PM_2.4		
Title	S3/CM3-PG to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support</div> <div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM-Off to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/CM3-PG
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_2.4
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that, where available, <b>only</b> the Host OS Wake on LAN and/or Wake on Wireless LAN driver setting(s) are <b>enabled</b> on the SUT. All other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to help prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>

ID	ME_PM_2.5		
Title	S3/CM3-PG with AC Wake to S0/CM0 via Power Button press (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG with AC Wake to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/CM3-PG with AC Wake
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_2.5
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/CM3-PG with AC Wake</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>

ID	ME_PM_2.6		
Title	S3/CM3-PG to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/CM3-PG
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_2.6
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>

ID	ME_PM_2.7		
Title	S3/CM-Off with AC Wake to S0/CM0 via magic packet (DC-only/PP1/LP3)		
Requirement	Optional	Non-Support	<div><div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div><div><input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support</div><div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div></div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG with AC Wake to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/CM3-PG with AC Wake
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	



ID	ME_PM_2.7
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that, where available, <b>only</b> the Host OS Wake on LAN and/or Wake on Wireless LAN driver setting(s) are <b>enabled</b> on the SUT. All other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to help prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/CM3-PG with AC Wake.</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>

ID	ME_PM_2.8		
Title	S3/CM3-PG with AC Wake to S0/CM0 via magic packet (DC-only/PP2/LP3)		
Requirement	Optional	Non-Support	<div><div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div><div><input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support</div><div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div></div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG with AC Wake to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/CM3-PG with AC Wake
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	





ID	ME_PM_2.8
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that, where available, <b>only</b> the Host OS Wake on LAN and/or Wake on Wireless LAN driver setting(s) are <b>enabled</b> on the SUT. All other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to help prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.with AC Wake.</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>

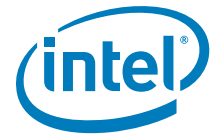
## 11.6 ME\_PM\_3 - S0/CM0 to S3/CM3

ID	ME_PM_3.1		
Title	S0/CM0 to S3/CM3 via Host OS suspend (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM3 via Host OS suspend with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S3/MeOn (CM3)
		Trigger	Host OS suspend
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_3.1
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Pass Criteria</b>	The test passes, if the SUT moves to S3, and the Intel® ME is in MeOn (CM3).

ID	ME_PM_3.21		
<b>Title</b>	S0/CM0 to S3/CM3 via Host OS suspend (AC+DC, AC-only/PP2/LP2)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems <input checked="" type="checkbox"/> Systems with a LAN-only network interface
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM3 via Host OS suspend with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	S3/MeOn (CM3)
		<b>Trigger</b>	Host OS suspend
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP2 (Enabled in S0)
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		



ID	ME_PM_3.21
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"><li>• The SUT moves to S3.</li><li>• The Intel® ME is in MeOn (CM3).</li><li>• When in S3:<ul style="list-style-type: none"><li>— Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li><li>— Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li></ul></li></ul>



## 11.7 ME\_PM\_4 - S3/CM3 to S0/CM0

ID	ME_PM_4.1		
Title	S3/CM3 to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that, where available, <b>only</b> the Host OS Wake on LAN and/or Wake on Wireless LAN driver setting(s) are <b>enabled</b> on the SUT. All other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to help prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>		



ID	ME_PM_4.2		
<b>Title</b>	S3/CM3 to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S3/CM3 to S0/CM0 via Power Button press with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S3/MeOn (CM3)
		<b>Final</b>	S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b>	Power Button press
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
<b>Pass Criteria</b>	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>		

ID	ME_PM_4.21		
<b>Title</b>	S3/CM3 to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP2)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
<b>Method</b>	Automated by Intel® PETS		



ID	ME_PM_4.21		
Objective	This test checks the SUT power flow from S3/CM3 to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0), if the WLAN network interface is available.</li> <li>Ensure that, where available, <b>only</b> the Host OS Wake on LAN and/or Wake on Wireless LAN driver setting(s) are <b>enabled</b> on the SUT. All other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to help prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>		

ID	ME_PM_4.22		
Title	S3/CM3 to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S0/CM0 via Power Button press with the parameters outlined below.		



ID	ME_PM_4.22		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S3 to S0.</li> <li>The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time has not changed.</li> </ul>		



## 11.8 ME\_PM\_5 - S3/CM3 to S3/CM-Off (Without Intel® CSME Wake)

ID	ME_PM_5.1		
Title	S3/CM3 to S3/CM3-PG with AC wake via AC-detach (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S3/CM3-PG with AC Wake via AC-detach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC
	Power States	Initial	S3/MeOn (CM3)
		Final	S3/CM3-PG with AC Wake
		Trigger	AC-detach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to <b>AC+DC</b>.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Verify that a DC battery is connected to the SUT, and that it is charged.</li><li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li><li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Suspend the SUT via the Host OS.</li><li>Verify that the SUT is in S3/MeOn (CM3).</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li></ol>		
Procedure	<ol style="list-style-type: none"><li>Set the SUT power source to DC-only.</li><li>Verify that the SUT is in S3/(CM3-PG) with AC Wake.</li></ol>		
Pass Criteria	The test passes, if the SUT remains in S3 and the Intel® ME moves to CM3-PG.		

ID	ME_PM_5.2		
Title	S3/CM3 to S3/CM-Off via Intel® AMT Power Package change (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S3/CM-Off via Intel® AMT Power Package change with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		





ID	ME_PM_5.2		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S3/MeOff (CM-Off)
		Trigger	Set Intel® AMT PP1 (Intel® ME on in S0)
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> </ol>		
Pass Criteria	The test passes, if the SUT remains in S3 and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_5.21		
Title	S3/CM3 to S3/CM3-PG with AC Wake via AC-detach (AC+DC/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
			<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
			<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S3/CM3-PG with AC Wake via AC-detach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC
	Power States	Initial	S3/MeOn (CM3)
		Final	S3/CM3-PG with Ac Wake
		Trigger	AC-detach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_5.21
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to DC-only.</li> <li>Verify that the SUT is in S3/(CM3-PG)with AC Wake.</li> </ol>
Pass Criteria	The test passes, if the SUT remains in S3 and the Intel® ME moves to CM3-PG with AC Wake.

ID	ME_PM_5.22		
Title	S3/CM3 to S3/CM-Off via Intel® AMT Power Package change (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div> <div><input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S3/CM-Off via Intel® AMT Power Package change with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S3/CM3-PG
		Trigger	Set Intel® AMT PP1 (Intel® ME on in S0)
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP2 (Enabled in S0)	
Setup	<div><div>1.</div><div>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</div></div> <div><div>2.</div><div>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</div></div> <div><div>3.</div><div>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div></div> <div><div>4.</div><div>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</div></div> <div><div>5.</div><div>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</div></div> <div><div>6.</div><div>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div></div> <div><div>7.</div><div>Suspend the SUT via the Host OS.</div></div> <div><div>8.</div><div>Verify that the SUT is in S3/MeOn (CM3).</div></div> <div><div>9.</div><div>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</div></div> <div><div>10.</div><div>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</div></div>		
Procedure	<div><div>1.</div><div>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div></div> <div><div>2.</div><div>Verify that the SUT is in S3/MeOff (CM-Off).</div></div>		
Pass Criteria	The test passes, if the SUT remains in S3 and the Intel® ME moves to MeOff (CM-Off).		



## 11.9 ME\_PM\_6 - S3/CM3 to S3/CM-Off (with Intel® CSME Wake)

ID	ME_PM_6.1	
<b>Title</b>	S3/CM3 to S3/CM3-PG via Intel® AMT idle timeout (AC+DC, AC-only/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S3/CM3 to S3/CM-Off via Intel® AMT idle timeout with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
<b>Parameters</b>	<b>System Power Source</b>	AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b> S3/MeOn (CM3)
		<b>Final</b> S3/CM3-PG
		<b>Trigger</b> Intel® AMT idle timeout
	<b>Intel® AMT</b>	<b>Power Package</b> PP2 (Intel® ME on in S0, wake in Sx/AC) <b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S3/CM3-PG.</li> </ol>	
<b>Pass Criteria</b>	The test passes, if the SUT remains in S3, and the Intel® ME moves to CM3-PG.	

ID	ME_PM_6.21	
<b>Title</b>	S3/CM3 to S3/CM3-PG via Intel® AMT idle timeout (AC+DC, AC-only/PP2/LP2)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems <input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S3/CM3 to S3/CM-Off via Intel® AMT idle timeout with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that both LAN and WLAN network interfaces are available on the SUT.	



ID	ME_PM_6.21		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S3/CM3-PG
		Trigger	Intel® AMT idle timeout
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S3/CM3-PG.</li> </ol>		
Pass Criteria	The test passes, if the SUT remains in S3, and the Intel® ME moves to CM3-PG.		

## 11.10 ME\_PM\_7 - S3/CM-Off to S3/CM3

ID	ME_PM_7.1		
Title	S3/CM3-PG to S3/CM3 via Intel® AMT network access (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG to S3/CM3 via Intel® AMT network access with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/CM3-PG
		Final	S3/MeOn (CM3)
		Trigger	Intel® AMT network access
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_7.1
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> <li>Verify that Intel® AMT on the SUT responds to version query by means of the active network interface.</li> <li>Verify that the Intel® ME on the SUT is on.</li> </ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The SUT remains in S3.</li> <li>The Intel® ME moves to MeOn (CM3).</li> </ul>

ID	ME_PM_7.2		
Title	S3/CM3-PG with AC Wake to S3/CM3 via AC-attach (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG with Ac Wake to S3/CM3 via AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/CM3-PG with AC Wake
		Final	S3/MeOn (CM3)
		Trigger	AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_7.2
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/(CM3-PG)with AC Wake</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S3.</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_7.21		
Title	S3/CM3-PG to S3/CM3 via Intel® AMT network access (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div> <div><input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM-Off to S3/CM3 via Intel® AMT network access with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/CM3-PG
		Final	S3/MeOn (CM3)
		Trigger	Intel® AMT network access
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_7.21
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>Verify that the Intel® ME on the SUT is on.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S3.</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>When in S3: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li> </ul> </li> </ul>

ID	ME_PM_7.22		
Title	S3/CM3-PG with AC wake to S3/CM3 via AC-attach (DC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
			<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
			<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG with AC Wake to S3/CM3 via AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/CM3-PG
		Final	S3/MeOn (CM3)
		Trigger	AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_7.22
Setup	<ol style="list-style-type: none"><li>1. Set the SUT power source to AC+DC.</li><li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>3. Verify that a DC battery is connected to the SUT, and that it is charged.</li><li>4. Set the SUT power source to <b>DC-only</b>.</li><li>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li><li>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li><li>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li><li>8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>9. Suspend the SUT via the Host OS.</li><li>10. Verify that the SUT is in S3/(CM3-PG)with AC Wake.</li></ol>
Procedure	<ol style="list-style-type: none"><li>1. Set the SUT power source to AC+DC.</li><li>2. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li><li>3. Verify that the SUT is in S3/MeOn (CM3).</li><li>4. Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li></ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"><li>• The SUT remains in S3.</li><li>• The Intel® ME moves to MeOn (CM3).</li><li>• When in S3:<ul style="list-style-type: none"><li>— Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li><li>— Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li></ul></li></ul>





## 11.11 ME\_PM\_8 - S0/CM0 to S4/CM-Off or S5/CM-Off

ID	ME_PM_8.1		
<b>Title</b>	S0/CM0 to S4/CM-Off via Host OS hibernate (DC-only/PP1/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM-Off via Host OS hibernate with the parameters outlined below.		
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
<b>Parameters</b>	<b>System Power Source</b>		DC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		<b>Trigger</b>	Host OS hibernate
	<b>Intel® AMT</b>	<b>Power Package</b>	PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves to S4, S5, Deep S4, Deep S5, or G3, and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_8.2		
<b>Title</b>	S0/CM0 to S4/CM-Off via Host OS hibernate (AC+DC, AC-only/PP1/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM-Off via Host OS hibernate with the parameters outlined below.		
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		



ID	ME_PM_8.2		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Trigger	Host OS hibernate
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to S4, S5, Deep S4, Deep S5, or G3, and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_8.3		
Title	S0/CM0 to S5/CM-Off via Host OS shutdown (DC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off via Host OS shutdown with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Host OS shutdown
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>		



<b>ID</b>	<b>ME_PM_8.3</b>
<b>Pass Criteria</b>	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).

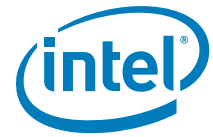
<b>ID</b>	<b>ME_PM_8.4</b>		
<b>Title</b>	S0/CM0 to S5/CM-Off via Host OS shutdown (AC+DC, AC-only/PP1/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S5/CM-Off via Host OS shutdown with the parameters outlined below.		
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	S5, Deep S5, G3/MeOff (CM-Off)
		<b>Trigger</b>	Host OS shutdown
	<b>Intel® AMT</b>	<b>Power Package</b>	PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).		

<b>ID</b>	<b>ME_PM_8.5</b>		
<b>Title</b>	S0/CM0 to S4/CM3-PG with AC Wake via Host OS hibernate (DC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM3-PG with AC Wake via Host OS hibernate with the parameters outlined below.		
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		



ID	ME_PM_8.5		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S4,S5,Deep S4,Deep S5,G3/CM3-PG with AC wake
		Trigger	Host OS hibernate
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4 , S5, Deep S4, Deep S5, G3/CM3-PG.with AC Wake.</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to S4, S5, Deep S4, Deep S5, or G3, and the Intel® ME moves to CM3-PG with Ac Wake.		

ID	ME_PM_8.6		
Title	S0/CM0 to S5/CM3-PG with AC Wake via Host OS shutdown (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3-PG with Ac Wake via Host OS shutdown with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5,Deep S5,G3/CM3-PG with Ac Wake
		Trigger	Host OS shutdown
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		



ID	ME_PM_8.6
Procedure	<ol style="list-style-type: none"><li>1. Shutdown the SUT via the Host OS.</li><li>2. Verify that the SUT is in S5, Deep S5, G3/CM3-PG. with Ac Wake.</li></ol>
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to CM3-PG with AC Wake.



## 11.12 ME\_PM\_9 - G3 or S4/CM-Off or S5/CM-Off (Suspend Well Off) to S0/CM0

ID	ME_PM_9.1		
Title	S4/CM-Off to S0/CM0 via Power Button press (DC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM-Off to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_9.2		
Title	S4/CM-Off to S0/CM0 via Power Button press (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None



ID	ME_PM_9.2		
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM-Off to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		
ID	ME_PM_9.3		
Title	S4/CM3-PG with AC wake to S0/CM0 via Power Button press (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG with AC Wake to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		



ID	ME_PM_9.3		
Parameters	System Power Source		DC-only
	Power States	Initial	S4,S5,Deep S4,Deep S5,G3/CM3-PG with AC Wake
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4 , S5, Deep S4, Deep S5, G3/CM3-PG.with AC wake.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_9.4	
Title	S5/CM-Off to S0/CM0 via Power Button press (DC-only/PP1/LP3)	
Requirement	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S5/CM-Off to S0/CM0 via Power Button press with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>Confirm that the Host OS is configured to shutdown the SUT upon Power Button press.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	





ID	ME_PM_9.4		
Parameters	System Power Source		DC-only
	Power States	Initial	S5, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the brief Power Button press.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5 (or Deep S5 or G3) to S0.</li> <li>The Intel® ME moves to MeOn (CM0).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_9.5		
Title	S5/CM-Off to S0/CM0 via Power Button press (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM-Off to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>Confirm that the Host OS is configured to shutdown the SUT upon Power Button press.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_9.5
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>8. Shutdown the SUT via the brief Power Button press.</li> <li>9. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Briefly press the Power Button on the SUT.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>3. Verify that the Host OS on the SUT is available.</li> <li>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>5. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT moves from S5 (or Deep S5 or G3) to S0.</li> <li>• The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>• Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_9.6		
Title	S5/CM3-PG with AC wake to S0/CM0 via Power Button press (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG with AC Wake to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>Confirm that the Host OS is configured to shutdown the SUT upon Power Button press.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S5,Deep S5,G3/CM3-PG with AC Wake
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	



ID	ME_PM_9.6
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the brief Power Button press.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC wake.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5 (or Deep S5 or G3) to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_9.7		
Title	G3/CM-Off to S0/CM0 via AC-attach (AC+DC, AC-only/PP1/LP3)		
Requirement	Optional		
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from G3/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>Confirm that the BIOS is configured to boot SUT upon AC-attach after G3.</p> <p>Confirm that the Host OS is configured to shutdown the SUT upon Power Button press.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	AC-attach
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	



ID	ME_PM_9.7
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the brief Power Button press.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from G3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_9.8	
Title	G3/CM-Off to S0/CM0 via AC-attach (AC+DC, AC-only/PP2/LP3)	
Requirement	Optional	
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from G3/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>Confirm that the BIOS is configured to boot SUT upon AC-attach after G3.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
		WLAN Link Policy



ID	ME_PM_9.8
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>8. Shutdown the SUT via the Host OS.</li> <li>9. Verify that the SUT is in S5/MeOn (CM3).</li> <li>10. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>11. Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>12. Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> <li>13. Verify that the SUT is in G3/MeOff (CM-Off).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>3. Verify that the Host OS on the SUT is available.</li> <li>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>5. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT moves from G3 to S0.</li> <li>• The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>• Intel® AMT responds to version queries via all available network interfaces.</li> </ul>



## 11.13 ME\_PM\_10 - S4/CM-Off or S5/CM-Off (Suspend Well On) to S0/CM0

ID	ME_PM_10.1		
Title	S4/CM-Off to S0/CM0 via magic packet (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM-Off to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol> <p>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</p>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_10.3		
Title	S4/CM3-PG to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS		



ID	ME_PM_10.3		
Objective	This test checks the SUT power flow from S4/CM3-PG to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that LAN-only network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOff (CM3-PG)
		Final	S0/MeOn (CM0)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S4, S5/CM3-PG.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the <b>LAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves from S4 to S0.</li> <li>The Intel® ME moves to MeOn (CM0).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_10.4		
Title	S4/CM3-PG to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that LAN-only network interfaces are available on the SUT.		



ID	ME_PM_10.4		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOff (CM3-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S4, S5/CM3-PG.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S4 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>		

ID	ME_PM_10.5	
Title	S5/CM-Off to S0/CM0 via magic packet (AC+DC, AC-only/PP1/LP3)	
Requirement	Mandatory	Exemptions   <input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S5/CM-Off to S0/CM0 via magic packet with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test network interface.</p>	





ID	ME_PM_10.5		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol> <p>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</p>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5 (or Deep S5 or G3) to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>		

ID	ME_PM_10.6		
Title	S5/CM-Off to S0/CM0 via Power Button press (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM-Off to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that LAN-only network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)



ID	ME_PM_10.6
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5 (or Deep S5 or G3) to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>

ID	ME_PM_10.7		
Title	S5/CM3-PG to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that LAN-only network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOff (CM3-PG)
		Final	S0/MeOn (CM0)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S5/CM3-PG.</li> </ol>		



ID	ME_PM_10.7
Procedure	<ol style="list-style-type: none"> <li>1. Send three magic packets, at <b>2 second</b> intervals, by means of the <b>LAN</b> network interface.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0).</li> <li>3. Verify that the Host OS on the SUT is available.</li> <li>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>5. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>• The SUT moves from S5 to S0.</li> <li>• The Intel® ME moves to MeOn (CM0).</li> <li>• Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>

ID	ME_PM_10.8		
Title	S5/CM3-PG to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that LAN-only network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOff (CM3-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>4. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>5. Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>8. Shutdown the SUT via the Host OS.</li> <li>9. Verify that the SUT is in S5/MeOn (CM3).</li> <li>10. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>11. Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>12. Verify that the SUT is in S5/CM3-PG.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>1. Briefly press the Power Button on the SUT.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>3. Verify that the Host OS on the SUT is available.</li> <li>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>5. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>• The SUT moves from S5 to S0.</li> <li>• The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>• Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>		



ID	ME_PM_10.9															
Title	S4/CM-Off to S0/CM0 via magic packet (DC-only/PP1/LP3)															
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support</div>													
Method	Automated by Intel® PETS															
Objective	This test checks the SUT power flow from S4/CM-Off to S0/CM0 via magic packet with the parameters outlined below.															
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test.</p>															
Parameters	<table><tr><th colspan="2">System Power Source</th><th>DC-only</th></tr><tr><th rowspan="3">Power States</th><th>Initial</th><td>S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)</td></tr><tr><th>Final</th><td>S0/MeOn (CM0, CM0-PG)</td></tr><tr><th>Trigger</th><td>Magic Packet receipt</td></tr><tr><th>Intel® AMT</th><th>Power Package</th><td>PP1 (Intel® ME on in S0)</td></tr></table>			System Power Source		DC-only	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)	Final	S0/MeOn (CM0, CM0-PG)	Trigger	Magic Packet receipt	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
System Power Source		DC-only														
Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)														
	Final	S0/MeOn (CM0, CM0-PG)														
	Trigger	Magic Packet receipt														
Intel® AMT	Power Package	PP1 (Intel® ME on in S0)														
Setup	<div><div>1.</div><div>Set the SUT power source to AC+DC.</div></div> <div><div>2.</div><div>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div></div> <div><div>3.</div><div>Verify that a DC battery is connected to the SUT, and that it is charged.</div></div> <div><div>4.</div><div>Set the SUT power source to <b>DC-only</b>.</div></div> <div><div>5.</div><div>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div></div> <div><div>6.</div><div>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</div></div> <div><div>7.</div><div>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div></div> <div><div>8.</div><div>Ensure yellow bang is not seen on Drivers in Device Manager.</div></div>															
Procedure	<div><div>1.</div><div>Hibernate the SUT via the Host OS.</div></div> <div><div>2.</div><div>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</div></div> <div><div>3.</div><div>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</div></div> <div><div>4.</div><div>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div></div> <div><div>5.</div><div>Verify that the Host OS on the SUT is available.</div></div> <div><div>6.</div><div>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div></div> <div><div>7.</div><div>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}</div></div> <div><div>8.</div><div>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</div></div> <div><div>9.</div><div>Ensure yellow bang is not seen on Drivers in Device Manager</div></div> <div><div></div><div>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</div></div>															
Pass Criteria	<div>The test passes, if:</div> <div><div>•</div><div>The SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0.</div></div> <div><div>•</div><div>The Intel® ME moves to MeOn (CM0, CM0-PG).</div></div> <div><div>•</div><div>Intel® AMT responds to version queries via LAN network interfaces.</div></div>															

ID	ME_PM_10.10		
Title	S4/CM3-PG with AC Wake to S0/CM0 via magic packet (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
			<input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS		



ID	ME_PM_10.10		
Objective	This test checks the SUT power flow from S4/CM3-PG with AC Wake to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S4,S5,Deep S4,Deep S5,G3/CM3-PG with Ac Wake
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, Deep S4/CM3-PG with AC Wake.</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol> <p>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</p>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>		

ID	ME_PM_10.11		
Title	S5/CM-Off to S0/CM0 via magic packet (DC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM-Off to S0/CM0 via magic packet with the parameters outlined below.		



ID	ME_PM_10.11		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S5, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to AC+DC.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Verify that a DC battery is connected to the SUT, and that it is charged.</li><li>Set the SUT power source to <b>DC-only</b>.</li><li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li><li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager.</li></ol>		
Procedure	<ol style="list-style-type: none"><li>Shutdown the SUT via the Host OS.</li><li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li><li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li><li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>Verify that the Host OS on the SUT is available.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager</li></ol> <p>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</p>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"><li>The SUT moves from S5 (or Deep S5 or G3) to S0.</li><li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li><li>Intel® AMT responds to version queries via LAN network interfaces.</li></ul>		

ID	ME_PM_10.12		
Title	S5/CM3-PG with AC Wake to S0/CM0 via magic packet (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG with AC Wake to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test.</p>		



ID	ME_PM_10.12		
Parameters	System Power Source		DC-only
	Power States	Initial	S5, Deep S5, G3/CM3-PG with AC Wake
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake.</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol> <p>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</p>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5 (or Deep S5 or G3) to S0.</li> <li>The Intel® ME moves to MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>		



## 11.14 ME\_PM\_11 - S0/CM0 to S4, S5/CM3

ID	ME_PM_11.1		
Title	S0/CM0 to S4/CM3 via Host OS hibernate (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM3 via Host OS hibernate with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S4,S5/MeOn (CM3)
		Trigger	Host OS hibernate
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li><li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li></ol>		
Procedure	<ol style="list-style-type: none"><li>Hibernate the SUT via the Host OS.</li><li>Verify that the SUT is in S4, S5/MeOn (CM3).</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li></ol>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"><li>The SUT moves to S4.</li><li>The Intel® ME moves to MeOn (CM3).</li><li>Intel® AMT responds to version queries via all available network interfaces.</li></ul>		

ID	ME_PM_11.2		
Title	S0/CM0 to S5/CM3 via Host OS shutdown (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3 via Host OS shutdown with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5/MeOn (CM3)
		Trigger	Host OS shutdown
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available





ID	ME_PM_11.2
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_11.21		
<b>Title</b>	S0/CM0 to S4/CM3 via Host OS hibernate (AC+DC, AC-only/PP2/LP2)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM3 via Host OS hibernate with the parameters outlined below.		
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	S4,S5/MeOn (CM3)
		<b>Trigger</b>	Host OS hibernate
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP2 (Enabled in S0)
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		



ID	ME_PM_11.21
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S4.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>When in S4: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li> </ul> </li> </ul>

ID	ME_PM_11.22		
Title	S0/CM0 to S5/CM3 via Host OS shutdown (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3 via Host OS shutdown with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5/MeOn (CM3)
		Trigger	Host OS shutdown
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>When in S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li> </ul> </li> </ul>		



## 11.15 ME\_PM\_12 - S4-S5/CM3 to S0/CM0

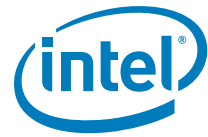
ID	ME_PM_12.1		
Title	S4/CM3 to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support <input checked="" type="checkbox"/> Systems with a WLAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3 to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S0/MeOn (CM0)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that <b>only</b> the Host OS Wake on LAN driver setting is <b>enabled</b> on the SUT; all other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events, and <b>disabling</b> the Host OS Wake on Wireless LAN driver settings, if available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the <b>LAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves from S4 to S0.</li> <li>The Intel® ME is in MeOn (CM0).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_12.2		
Title	S4/CM3 to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		



ID	ME_PM_12.2		
Objective	This test checks the SUT power flow from S4/CM3 to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. This test assumes that either LAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves from S4 to S0.</li> <li>The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_12.4		
Title	S5/CM3 to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support</div> <div><input checked="" type="checkbox"/> Systems with a WLAN-only network interface</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, or both LAN and WLAN network interfaces are available on the SUT.		



ID	ME_PM_12.4		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S0/MeOn (CM0)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that <b>only</b> the Host OS Wake on LAN driver setting is <b>enabled</b> on the SUT; all other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events, and <b>disabling</b> the Host OS Wake on Wireless LAN driver settings, if available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the <b>LAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves from S5 to S0.</li> <li>The Intel® ME is in MeOn (CM0).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_12.5		
Title	S5/CM3 to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. Confirm that the Host OS is configured to shutdown the SUT upon Power Button press. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_12.5
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the brief Power Button press.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5 to S0.</li> <li>The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_12.21		
Title	S4/CM3 to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support</div> <div><input checked="" type="checkbox"/> Systems with a WLAN-only network interface</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3 to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S0/MeOn (CM0)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0) where available



ID	ME_PM_12.21
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0), if the WLAN network interface is available.</li> <li>Ensure that <b>only</b> the Host OS Wake on LAN driver setting is <b>enabled</b> on the SUT; all other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events, and <b>disabling</b> the Host OS Wake on Wireless LAN driver settings, if available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface, if available.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the <b>LAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S4 to S0.</li> <li>The Intel® ME is in MeOn (CM0).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_12.22		
Title	S4/CM3 to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3 to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_12.22
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S4 to S0.</li> <li>The Intel® ME is in MeOn (CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_12.24		
Title	S5/CM3 to S0/CM0 via magic packet (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support
			<input checked="" type="checkbox"/> Systems with a WLAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S0/MeOn (CM0)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0) where available





ID	ME_PM_12.24
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0), if the WLAN network interface is available.</li> <li>Ensure that <b>only</b> the Host OS Wake on LAN driver setting is <b>enabled</b> on the SUT; all other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events, and <b>disabling</b> the Host OS Wake on Wireless LAN driver settings, if available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface, if available.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the <b>LAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5 to S0.</li> <li>The Intel® ME is in MeOn (CM0).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_12.25		
Title	S5/CM3 to S0/CM0 via Power Button press (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S0/CM0 via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. Confirm that the Host OS is configured to shutdown the SUT upon Power Button press. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_12.25
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>8. Briefly press the Power Button on the SUT.</li> <li>9. Verify that the SUT is in S5/MeOn (CM3).</li> <li>10. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>11. Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Briefly press the Power Button on the SUT.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>3. Verify that the Host OS on the SUT is available.</li> <li>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>5. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT moves from S5 to S0.</li> <li>• The Intel® ME is in MeOn (CM0, CM0-PG).</li> <li>• Intel® AMT responds to version queries via all available network interfaces.</li> </ul>



## 11.16 ME\_PM\_13 - S4-S5/CM3 to S4-S5/CM-Off (Without Intel® ME Wake)

ID	ME_PM_13.1		
<b>Title</b>	S4/CM3 to S4/CM3-PG with Ac Wake via AC-detach (AC+DC/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S4/CM3 to S4/CM3-PG with AC Wake via AC-detach with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC
	<b>Power States</b>	<b>Initial</b>	S4,S5/MeOn (CM3)
		<b>Final</b>	S4,S5,Deep S4,Deep S5,G3/CM3-PG with AC Wake
		<b>Trigger</b>	AC-detach
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	1. Set the SUT power source to <b>AC+DC</b> . 2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available. 3. Verify that a DC battery is connected to the SUT, and that it is charged. 4. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC). 5. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available. 6. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events. 7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces. 8. Hibernate the SUT via the Host OS. 9. Verify that the SUT is in S4, S5/MeOn (CM3). 10. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.		
<b>Procedure</b>	1. Set the SUT power source to DC-only. 2. Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/CM3-PG.with AC Wake.		
<b>Pass Criteria</b>	The test passes, if the SUT remains in S4 or S5 (or moves to Deep S4, Deep S5, or G3), and the Intel® ME moves to CM3-PG with AC Wake.		

ID	ME_PM_13.2		
<b>Title</b>	S4/CM3 to S4/CM-Off via Intel® AMT Power Package change (AC+DC, AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S4/CM3 to S4/CM-Off via Intel® AMT Power Package change with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		



ID	ME_PM_13.2		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Trigger	Set Intel® AMT PP1 (Intel® ME on in S0)
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Pass Criteria	The test passes, if the SUT remains in S4 or S5 (or moves to Deep S4, Deep S5, or G3), and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_13.3		
Title	S5/CM3 to S5/CM3-PG with AC Wake via AC-detach (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM3-PG with AC Wake via AC-detach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC
	Power States	Initial	S5/MeOn (CM3)
		Final	S5,Deep S5,G3/CM3-PG with Ac Wake
		Trigger	AC-detach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_13.3
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to DC-only.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake.</li> </ol>
<b>Pass Criteria</b>	The test passes, if the SUT remains in S5 (or moves to Deep S5 or G3), and the Intel® ME moves to CM3-PG with AC Wake.

ID	ME_PM_13.4		
Title	S5/CM3 to S5/CM-Off via Intel® AMT Power Package change (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM-Off via Intel® AMT Power Package change with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Set Intel® AMT PP1 (Intel® ME on in S0)
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	1. Set the SUT power source to <b>AC+DC</b> . 2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available. 3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC). 4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available. 5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events. 6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces. 7. Shutdown the SUT via the Host OS. 8. Verify that the SUT is in S5/MeOn (CM3). 9. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.		
Procedure	1. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0). 2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).		
Pass Criteria	The test passes, if the SUT remains in S5 (or moves to Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).		



ID	ME_PM_13.21	
Title	S4/CM3 to S4/CM3-PG with AC wake via AC-detach (AC+DC/PP2/LP2)	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems  <input checked="" type="checkbox"/> Systems with a LAN-only network interface </div>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S4/CM3 to S4/CM-Off via AC-detach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	AC+DC
		S4,S5/MeOn (CM3)
		S4,S5,Deep S4,Deep S5,G3/CM3-PG with AC Wake
	Intel® AMT	AC-detach
		PP2 (Intel® ME on in S0, wake in Sx/AC)
	WLAN Link Policy	
	LP2 (Enabled in S0)	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to DC-only.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/CM3-PG with AC Wake.</li> </ol>	
Pass Criteria	The test passes, if the SUT remains in S4 or S5 (or moves to Deep S4, Deep S5, or G3), and the Intel® ME moves to CM3-PG with AC Wake.	

ID	ME_PM_13.22	
Title	S4/CM3 to S4/CM-Off via Intel® AMT Power Package change (AC+DC, AC-only/PP2/LP2)	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN) </div>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S4/CM3 to S4/CM-Off via Intel® AMT Power Package change with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that both LAN and WLAN network interfaces are available on the SUT.</p>	



ID	ME_PM_13.22		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Trigger	Set Intel® AMT PP1 (Intel® ME on in S0)
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Pass Criteria	The test passes, if the SUT remains in S4 or S5 (or moves to Deep S4, Deep S5, or G3), and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_13.23		
Title	S5/CM3 to S5/CM3-PG with AC Wake via AC-detach (AC+DC/PP2/LP2)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Systems with a LAN-only network interface</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM-Off via AC-detach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC
	Power States	Initial	S5/MeOn (CM3)
		Final	S5,Deep S5,G3/CM3-PG with AC Wake
		Trigger	AC-detach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP2 (Enabled in S0)	



ID	ME_PM_13.23
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>4. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>5. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>6. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>8. Shutdown the SUT via the Host OS.</li> <li>9. Verify that the SUT is in S5/MeOn (CM3).</li> <li>10. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>11. Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Set the SUT power source to DC-only.</li> <li>2. Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake.</li> </ol>
Pass Criteria	The test passes, if the SUT remains in S5 (or moves to Deep S5 or G3), and the Intel® ME moves to CM3-PG with AC Wake

ID	ME_PM_13.24		
Title	S5/CM3 to S5/CM-Off via Intel® AMT Power Package change (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM-Off via Intel® AMT Power Package change with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>• The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Set Intel® AMT PP1 (Intel® ME on in S0)
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Shutdown the SUT via the Host OS.</li> <li>8. Verify that the SUT is in S5/MeOn (CM3).</li> <li>9. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>10. Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>1. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>		





<b>ID</b>	<b>ME_PM_13.24</b>
<b>Pass Criteria</b>	The test passes, if the SUT remains in S5 (or moves to Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).

## 11.17 ME\_PM\_14 - S4-S5/CM3 to S4-S5/CM-Off (with Intel® ME Wake)

<b>ID</b>	<b>ME_PM_14.1</b>		
<b>Title</b>	S4/CM3 to S4/CM3-PG via Intel® AMT idle timeout (AC+DC, AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S4/CM3 to S4/CM3-PG via Intel® AMT idle timeout with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S4,S5/MeOn (CM3)
		<b>Final</b>	S4,S5/MeOff (CM3-PG)
		<b>Trigger</b>	Intel® AMT idle timeout
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT remains in S4 or S5, and the Intel® ME moves to CM3-PG.		

<b>ID</b>	<b>ME_PM_14.2</b>		
<b>Title</b>	S5/CM3 to S5/CM3-PG via Intel® AMT idle timeout ((AC+DC, AC-only/PP2/LP2)AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S5/CM3 to S5/CM-Off via Intel® AMT idle timeout with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		



ID	ME_PM_14.2		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S5/MeOff (CM3-PG)
		Trigger	Intel® AMT idle timeout
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>		
Pass Criteria	The test passes, if the SUT remains in S5, and the Intel® ME moves to CM3-PG.		

ID	ME_PM_14.21		
Title	S4/CM3 to S4/CM3-PG via Intel® AMT idle timeout (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3 to S4/CM-Off via Intel® AMT idle timeout with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S4,S5/MeOff (CM3-PG)
		Trigger	Intel® AMT idle timeout
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_14.21
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>
Pass Criteria	The test passes, if the SUT remains in S4 or S5, and the Intel® ME moves to MeOff (CM3-PG).

ID	ME_PM_14.22		
Title	S5/CM3 to S5/CM3-PG via Intel® AMT idle timeout (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM3-PG via Intel® AMT idle timeout with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S5/MeOff (CM3-PG)
		Trigger	Intel® AMT idle timeout
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<div>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</div> <div>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</div> <div>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</div> <div>6. Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</div> <div>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>8. Shutdown the SUT via the Host OS.</div> <div>9. Verify that the SUT is in S5/MeOn (CM3).</div> <div>10. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</div> <div>11. Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</div>		
Procedure	<div>1. Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</div> <div>2. Verify that the Intel® ME on the SUT is in CM3-PG.</div>		
Pass Criteria	The test passes, if the SUT remains in S5, and the Intel® ME moves to MeOff (CM3-PG).		



## 11.18 ME\_PM\_15 - G3 or S4-S5/CM-Off (Suspend Well Off) to S4-S5/CM3

ID	ME_PM_15.1		
Title	S4/CM3-PG with Ac Wake to S4/CM3 via AC-attach (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG with Ac Wake to S4/CM3 via AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S4,S5,Deep S4,Deep S5,G3/CM3-PGwith AC Wake
		Final	S4,S5/MeOn (CM3)
		Trigger	AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4 , S5, Deep S4, Deep S5, G3/CM3-PG.with AC Wake.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S4 or S5 (or moves to S4 or S5 from Deep S4, Deep S5, or G3).</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>		

ID	ME_PM_15.2		
Title	S5/CM3-PG with AC Wake to S5/CM3 via AC-attach (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG with AC Wake to S5/CM3 via AC-attach with the parameters outlined below.		



ID	ME_PM_15.2	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	DC-only
		Initial S5,Deep S5,G3/CM3-PGwith Ac Wake
		Final S5/MeOn (CM3)
	Trigger AC-attach	
	Intel® AMT	Power Package PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> </ol>	
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S5 (or moves to S5 from Deep S5 or G3).</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>	

ID	ME_PM_15.3	
Title	G3/CM-Off to S5/CM3 via AC-attach (AC+DC, AC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions   None
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from G3/CM-Off to S5/CM3 via AC-attach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>Confirm that the BIOS is configured to move the SUT to S5 from G3 upon AC-attach.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	AC+DC or AC-only
		Initial G3/MeOff (CM-Off)
		Final S5/MeOn (CM3)
	Trigger AC-attach	
	Intel® AMT	Power Package PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_15.3
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from G3 to S5.</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_15.21		
Title	S4/CM3-PG with Ac Wake to S4/CM3 via AC-attach (DC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Systems with a LAN-only network interface</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG with AC Wake to S4/CM3 via AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S4,S5,Deep S4,Deep S5,G3/CM3-PG with Ac Wake
		Final	S4,S5/MeOn (CM3)
		Trigger	AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP2 (Enabled in S0)	



ID	ME_PM_15.21
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4 , S5, Deep S4, Deep S5, G3/CM3-PG.with AC Wake.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> </ol>
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S4 or S5 (or moves to S4 or S5 from Deep S4, Deep S5, or G3).</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>When in S4 or S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li> </ul> </li> </ul>

ID	ME_PM_15.22		
Title	S5/CM3-PG with AC Wake to S5/CM3 via AC-attach (DC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Systems with a LAN-only network interface</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG with AC Wake to S5/CM3 via AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S5,Deep S5,G3/CM3-PGwith AC Wake
		Final	S5/MeOn (CM3)
		Trigger	AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP2 (Enabled in S0)	



ID	ME_PM_15.22
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S5 (or moves to S5 from Deep S5 or G3).</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>When in S4 or S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li> </ul> </li> </ul>

ID	ME_PM_15.23		
Title	G3/CM-Off to S5/CM3 via AC-attach (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	☑ Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from G3/CM-Off to S5/CM3 via AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. Confirm that the BIOS is configured to move the SUT to S5 from G3 upon AC-attach. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	G3/MeOff (CM-Off)
		Final	S5/MeOn (CM3)
		Trigger	AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)





ID	ME_PM_15.23
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Shutdown the SUT via the Host OS.</li> <li>8. Verify that the SUT is in S5/MeOn (CM3).</li> <li>9. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>10. Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>11. Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>12. Verify that the SUT is in G3/MeOff (CM-Off).</li> <li>13. Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li> <li>2. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>3. Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>4. Verify that the SUT is in S5/MeOn (CM3).</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT moves from G3 to S5.</li> <li>• The Intel® ME moves to MeOn (CM3).</li> <li>• When in S5: <ul style="list-style-type: none"> <li>— Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>— Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li> </ul> </li> </ul>



## 11.19 ME\_PM\_16 - S4-S5/CM-Off (Suspend Well On) to S4-S5/CM3

ID	ME_PM_16.1		
Title	S4/CM3-PG to S4/CM3 via Intel® AMT network access (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG to S4/CM3 via Intel® AMT network access with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOff (CM3-PG)
		Final	S4,S5/MeOn (CM3)
		Trigger	Intel® AMT network access
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li><li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li><li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Hibernate the SUT via the Host OS.</li><li>Verify that the SUT is in S4, S5/MeOn (CM3).</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li></ol>		
Procedure	<ol style="list-style-type: none"><li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li><li>Verify that the Intel® ME on the SUT is in CM3-PG.</li><li>Verify that Intel® AMT on the SUT responds to version query by means of the active network interface.</li><li>Verify that the Intel® ME on the SUT is on.</li></ol> If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"><li>Intel® AMT responds to version queries via all available network interfaces.</li><li>The SUT remains in S4 or S5.</li><li>The Intel® ME moves to MeOn (CM3).</li></ul>		

ID	ME_PM_16.2		
Title	S5/CM3-PG to S5/CM3 via Intel® AMT network access (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		



ID	ME_PM_16.2		
Objective	This test checks the SUT power flow from S5/CM3-PG to S5/CM3 via Intel® AMT network access with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOff (CM3-PG)
		Final	S5/MeOn (CM3)
		Trigger	Intel® AMT network access
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> <li>Verify that Intel® AMT on the SUT responds to version query by means of the active network interface.</li> <li>Verify that the Intel® ME on the SUT is on.</li> </ol> <p>If both LAN and WLAN network interfaces are available, repeat this test procedure with the WLAN interface set as the active network interface.</p>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The SUT remains in S5.</li> <li>The Intel® ME moves to MeOn (CM3).</li> </ul>		

ID	ME_PM_16.21		
Title	S4/CM3-PG to S4/CM3 via Intel® AMT network access (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM-Off to S4/CM3 via Intel® AMT network access with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that both LAN and WLAN network interfaces are available on the SUT.		



ID	ME_PM_16.21		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOff (CM3-PG)
		Final	S4,S5/MeOn (CM3)
		Trigger	Intel® AMT network access
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that the Intel® ME on the SUT is on.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S4 or S5.</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>When in S4 or S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries the <b>WLAN</b> network interface.</li> </ul> </li> </ul>		

ID	ME_PM_16.22		
Title	S5/CM3-PG to S5/CM3 via Intel® AMT network access (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a single network interface (not LAN+WLAN)
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM-Off to S5/CM3 via Intel® AMT network access with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOff (CM3-PG)
		Final	S5/MeOn (CM3)
		Trigger	Intel® AMT network access
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_16.22
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that the Intel® ME on the SUT is on.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S5.</li> <li>The Intel® ME moves to MeOn (CM3).</li> <li>When in S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries via the <b>WLAN</b> network interface.</li> </ul> </li> </ul>



## 11.20 ME\_PM\_17 - Cold Reset

ID	ME_PM_17.6	
Title	S0/CM0 to S0/CM0 via CF9 Cold Reset (AC+DC, AC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions   None
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via CF9 Cold Reset with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source   AC+DC or AC-only	
	Power States	Initial   S0/MeOn (CM0, CM0-PG)
		Final   S0/MeOn (CM0, CM0-PG)
		Trigger   CF9 Cold Reset
	Intel® AMT	Power Package   PP2 (Intel® ME on in S0, wake in Sx/AC) WLAN Link Policy   LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>cleared to 0b</b>.</li> <li>Perform a <b>cold reset</b> of the SUT by writing <b>Eh</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset, or that the Host OS is unavailable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time <b>does not</b> match, or the Host OS is unavailable.</li> </ul>	

## 11.21 ME\_PM\_18 - Global Reset

**Note:** In order for Global reset tests to pass, the SUT should be in manufacturing mode.

ID	ME_PM_18.1	
Title	S0/CM0 to S0/CM0 via CF9 Global Reset (DC-only/PP1/LP3)	
Requirement	Mandatory	Exemptions   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Systems not in Intel® ME manufacturing mode
Method	Automated by Intel® PETS	



ID	ME_PM_18.1		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via CF9 Global Reset with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. Intel® ME should be configured in manufacturing mode. Confirm that the BIOS has <b>not set</b> the CF9 Lockdown. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	CF9 Global Reset
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	1. Set the SUT power source to AC+DC. 2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available. 3. Verify that a DC battery is connected to the SUT, and that it is charged. 4. Set the SUT power source to <b>DC-only</b> . 5. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0). 6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available. 7. Record the Host OS last boot time on the SUT (to verify reset execution). 8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces. 9. Verify that the Intel® ME is configured in manufacturing mode. 10. Ensure yellow bang is not seen on Drivers in Device Manager 11. Write 1b to CF6GR to enable global Reset.		
Procedure	1. Ensure that CF9h Global Reset (CF9GR) is <b>set to 1b</b> to enable global reset. 2. Perform a <b>global reset</b> of the SUT by writing either <b>6h</b> or <b>Eh</b> to I/O register CF9h. 3. Verify that the SUT is in S0/MeOn (CM0,CM0-PG). 4. Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests. 5. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces. 6. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset, or that the Host OS is unavailable. 7. Ensure yellow bang is not seen on Drivers in Device Manager.		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time <b>does not</b> match, or the Host OS is unavailable.</li> </ul>		

ID	ME_PM_18.2		
Title	S0/CM0 to S0/CM0 via CF9 Global Reset (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems not in Intel® ME manufacturing mode
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via CF9 Global Reset with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. Intel® ME should be configured in manufacturing mode. Confirm that the BIOS has <b>not set</b> the CF9 Lockdown. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		



ID	ME_PM_18.2		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	CF9 Global Reset
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the Intel® ME is configured in manufacturing mode.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Write 1b to CF6GR to enable global Reset.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>set to 1b</b> to enable global reset.</li> <li>Perform a <b>global reset</b> of the SUT by writing either <b>6h</b> or <b>Eh</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset, or that the Host OS is unavailable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time <b>does not</b> match, or the Host OS is unavailable.</li> </ul>		

ID	ME_PM_18.3		
Title	S0/CM0 to S0/CM0 via CF9 Global Reset (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Systems not in Intel® ME manufacturing mode
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via CF9 Global Reset with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>Intel® ME should be configured in manufacturing mode.</p> <p>Confirm that the BIOS has <b>not set</b> the CF9 Lockdown.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	CF9 Global Reset
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available





ID	ME_PM_18.3
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the Intel® ME is configured in manufacturing mode.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Write 1b to CF6GR to enable global Reset.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>set</b> to <b>1b</b> to enable global reset.</li> <li>Perform a <b>global reset</b> of the SUT by writing either <b>6h</b> or <b>Eh</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset, or that the Host OS is unavailable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time <b>does not</b> match, or the Host OS is unavailable.</li> </ul>

ID	ME_PM_18.4	
Title	S0/CM0 to S0/CM0 via CF9 Global Reset (AC+DC, AC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions   <input checked="" type="checkbox"/> Systems not in Intel® ME manufacturing mode
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via CF9 Global Reset with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. Intel® ME should be configured in manufacturing mode. Confirm that the BIOS has <b>not set</b> the CF9 Lockdown. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source	
	AC+DC or AC-only	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
WLAN Link Policy		



ID	ME_PM_18.4
Setup	<ol style="list-style-type: none"><li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li><li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li><li>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>5. Record the Host OS last boot time on the SUT (to verify reset execution).</li><li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>7. Verify that the Intel® ME is configured in manufacturing mode.</li><li>8. Ensure yellow bang is not seen on Drivers in Device Manager.</li><li>9. Write 1b to CF6GR to enable global Reset.</li></ol>
Procedure	<ol style="list-style-type: none"><li>1. Ensure that CF9h Global Reset (CF9GR) is <b>set</b> to <b>1b</b> to enable global reset.</li><li>2. Perform a <b>global reset</b> of the SUT by writing either <b>6h</b> or <b>Eh</b> to I/O register CF9h.</li><li>3. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>4. Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li><li>5. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>6. Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset, or that the Host OS is unavailable.</li><li>7. Ensure yellow bang is not seen on Drivers in Device Manager.</li></ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"><li>• The SUT is reset to S0.</li><li>• The Intel® ME is available in MeOn (CM0, CM0-PG).</li><li>• Intel® AMT responds to version queries via all available network interfaces.</li><li>• The Host OS last boot time <b>does not</b> match, or the Host OS is unavailable.</li></ul>



## 11.22 ME\_PM\_19 - Straight-to-S5, Intel® CSME Power Policy is S0 Only

ID	ME_PM_19.1		
Title	S0/CM0 to S5/CM-Off via Power Button override (DC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off via Power Button override with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_19.2		
Title	S0/CM0 to S5/CM-Off via Power Button override (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off via Power Button override with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		



ID	ME_PM_19.2		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_19.3																	
Title	S3/CM-Off to S5/CM-Off via Power Button override (DC-only/PP1/LP3)																	
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div>															
Method	Automated by Intel® PETS																	
Objective	This test checks the SUT power flow from S3/CM-Off to S5/CM-Off via Power Button override with the parameters outlined below.																	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>																	
Parameters	<table><tr><th colspan="2">System Power Source</th><td>DC-only</td></tr><tr><th rowspan="3">Power States</th><th>Initial</th><td>S3/MeOff (CM-Off)</td></tr><tr><th>Final</th><td>S5, Deep S5, G3/MeOff (CM-Off)</td></tr><tr><th>Trigger</th><td>Power Button override</td></tr><tr><th rowspan="2">Intel® AMT</th><th>Power Package</th><td>PP1 (Intel® ME on in S0)</td></tr><tr><th>WLAN Link Policy</th><td>LP3 (Enabled in S0, Sx/AC) where available</td></tr></table>			System Power Source		DC-only	Power States	Initial	S3/MeOff (CM-Off)	Final	S5, Deep S5, G3/MeOff (CM-Off)	Trigger	Power Button override	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)	WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
System Power Source		DC-only																
Power States	Initial	S3/MeOff (CM-Off)																
	Final	S5, Deep S5, G3/MeOff (CM-Off)																
	Trigger	Power Button override																
Intel® AMT	Power Package	PP1 (Intel® ME on in S0)																
	WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available																



ID	ME_PM_19.3
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>
Pass Criteria	<p>The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME is in MeOff (CM-Off).</p> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).</p>

ID	ME_PM_19.4		
Title	S3/CM-Off to S5/CM-Off via Power Button override (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM-Off to S5/CM-Off via Power Button override with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOff (CM-Off)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div><div>1.</div><div>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</div></div> <div><div>2.</div><div>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div></div> <div><div>3.</div><div>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div></div> <div><div>4.</div><div>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div></div> <div><div>5.</div><div>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</div></div> <div><div>6.</div><div></div></div> <div><div>7.</div><div>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div></div> <div><div>8.</div><div>Suspend the SUT via the Host OS.</div></div> <div><div>9.</div><div>Verify that the SUT is in S3/MeOff (CM-Off).</div></div>		
Procedure	<div><div>1.</div><div>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</div></div> <div><div>2.</div><div>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</div></div>		



ID	ME_PM_19.4
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME is in MeOff (CM-Off). <b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).

ID	ME_PM_19.5		
Title	S4/CM-Off to S5/CM-Off via Power Button override (DC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM-Off to S5/CM-Off via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</div> <div>8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>9. Hibernate the SUT via the Host OS.</div> <div>10. Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</div>		
Procedure	<div>1. Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</div> <div>2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</div>		
Pass Criteria	The test passes, if the SUT moves to, if not already there, S5 (or Deep S5 or G3), and the Intel® ME is in MeOff (CM-Off).  <b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).		

ID	ME_PM_19.6
Title	S4/CM-Off to S5/CM-Off via Power Button override (AC+DC, AC-only/PP1/LP3)
Requirement	Mandatory <b>Exemptions</b>   None
Method	Automated by Intel® PETS
Objective	This test checks the SUT power flow from S4/CM-Off to S5/CM-Off via Power Button override with the parameters outlined below.



ID	ME_PM_19.6	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b> S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		<b>Final</b> S5, Deep S5, G3/MeOff (CM-Off)
		<b>Trigger</b> Power Button override
	<b>Intel® AMT</b>	<b>Power Package</b> PP1 (Intel® ME on in S0) <b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>	
<b>Pass Criteria</b>	<p>The test passes, if the SUT moves to, if not already there, S5 (or Deep S5 or G3), and the Intel® ME is in MeOff (CM-Off).</p> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).</p>	

ID	ME_PM_19.7	
<b>Title</b>	S5/CM-Off to S5/CM-Off via Power Button override (DC-only/PP1/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S5/CM-Off to S5/CM-Off via Power Button override with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	DC-only
	<b>Power States</b>	<b>Initial</b> S5, Deep S5, G3/MeOff (CM-Off)
		<b>Final</b> S5, Deep S5, G3/MeOff (CM-Off)
		<b>Trigger</b> Power Button override
	<b>Intel® AMT</b>	<b>Power Package</b> PP1 (Intel® ME on in S0) <b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_19.7
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>
Pass Criteria	<p>The test passes, if the SUT ends the test in S5 (or Deep S5 or G3), and the Intel® ME is in MeOff (CM-Off).</p> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).</p>

ID	ME_PM_19.8		
Title	S5/CM-Off to S5/CM-Off via Power Button override (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM-Off to S5/CM-Off via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5, Deep S5, G3/MeOff (CM-Off)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div> <div>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</div> <div>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>7. Shutdown the SUT via the Host OS.</div> <div>8. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</div>		
Procedure	<div>1. Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</div> <div>2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</div>		
Pass Criteria	The test passes, if the SUT ends the test in S5 (or Deep S5 or G3), and the Intel® ME is in MeOff (CM-Off). <b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).		





<b>ID</b>	<b>ME_PM_19.9</b>		
<b>Title</b>	S0/CM0 to G3/CM-Off via Power loss (DC-only/PP1/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to G3/CM-Off via Power loss with the parameters outlined below.		
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
<b>Parameters</b>	<b>System Power Source</b>		DC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0, CM0-PG)
		<b>Final</b>	S5, Deep S5, G3/MeOff (CM-Off)
		<b>Trigger</b>	Power loss
	<b>Intel® AMT</b>	<b>Power Package</b>	PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Put the system to S5/ G3 via Unconditional Power Loss.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).		



## 11.23 ME\_PM\_20 - Straight-to-S5 via Power Button Override

ID	ME_PM_20.1	
Title	S0/CM0 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions   None
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3 via Power Button override with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source   AC+DC or AC-only	
	Power States	Initial   S0/MeOn (CM0, CM0-PG)
		Final   S5/MeOn (CM3)
		Trigger   Power Button override
	Intel® AMT	Power Package   PP2 (Intel® ME on in S0, wake in Sx/AC) WLAN Link Policy   LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>	
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>	

ID	ME_PM_20.2	
Title	S0/CM0 to S5/CM3-PG with AC Wake via Power Button override (DC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3-PG with Ac Wake via Power Button override with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	



ID	ME_PM_20.2		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5, Deep S5, G3/CM3-PG with AC Wake
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0, CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG with AC Wake.</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to CM3-PG with AC Wake.		

ID	ME_PM_20.3		
Title	S3/CM3 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0, CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		



ID	ME_PM_20.3
Procedure	<ol style="list-style-type: none"> <li>1. Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>2. Verify that the SUT is in S5/MeOn (CM3).</li> <li>3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT moves to S5.</li> <li>• The Intel® ME is in MeOn (CM3).</li> <li>• Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.4		
Title	S3/CM3-PG to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/CM3-PG
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<div>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>5. Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</div> <div>6. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</div> <div>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>8. Suspend the SUT via the Host OS.</div> <div>9. Verify that the SUT is in S3/MeOn (CM3).</div> <div>10. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>11. Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</div> <div>12. Verify that the Intel® ME on the SUT is in CM3-PG.</div>		
Procedure	<div>1. Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</div> <div>2. Verify that the SUT is in S5/MeOn (CM3).</div> <div>3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"><li>• The SUT moves to S5.</li><li>• The Intel® ME is in MeOn (CM3).</li><li>• Intel® AMT responds to version queries via all available network interfaces.</li></ul> <b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.		
ID	ME_PM_20.5		
Title	S4/CM3 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP3)		



ID	ME_PM_20.5		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3 to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.		

ID	ME_PM_20.6		
Title	S4/CM3-PG to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOff (CM3-PG)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_20.6
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.7		
Title	S5/CM3-PG to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOff (CM3-PG)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_20.7
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT ends the test in S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.8	
Title	S5/CM3 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions   None
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM3 via Power Button override with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source   AC+DC or AC-only	
	Power States	Initial   S5/MeOn (CM3)
		Final   S5/MeOn (CM3)
		Trigger   Power Button override
	Intel® AMT	Power Package   PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy   LP3 (Enabled in S0, Sx/AC) where available		



ID	ME_PM_20.8
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT ends the test in S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.9		
Title	S3/CM3-PG with AC Wake to S5/CM3-PG with AC Wake via Power Button override (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG with Ac Wake to S5/CM3-PG with AC Wake via Power Button override with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/CM3-PG with Ac Wake
		Final	S5,Deep S5,G3/CM3-PG with AC Wake
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available





ID	ME_PM_20.9
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/(CM3-PG)with AC Wake.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake</li> </ol>
Pass Criteria	<p>The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME is in CM3-PG.</p> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).</p>

ID	ME_PM_20.10		
Title	S4/CM3-PG with AC Wake to S5/CM3-PG with AC Wake via Power Button override (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG with AC Wake to S5/CM3-PG with AC Wake via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S4,S5,Deep S4,Deep S5,G3/CM3-PG with AC Wake
		Final	S5,Deep S5,G3/CM3-PG with AC Wake
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</div> <div>8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>9. Hibernate the SUT via the Host OS.</div> <div>10. Verify that the SUT is in S4 , S5, Deep S4, Deep S5, G3/CM3-PG.with AC Wake</div>		
Procedure	<div>1. Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</div> <div>2. Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake</div>		



ID	ME_PM_20.10
Pass Criteria	The test passes, if the SUT moves to, if not already there, S5 (or Deep S5 or G3), and the Intel® ME is in CM3-PG. <b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).

ID	ME_PM_20.11	
Title	S5/CM3-PG with AC Wake to S5/CM3-PG with AC Wake via Power Button override (DC-only/PP2/LP3)	
Requirement	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S5/CM3-PG to S5/CM3-PG via Power Button override with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	<b>System Power Source</b> DC-only	
	<b>Power States</b>	<b>Initial</b> S5, Deep S5, G3/MeOff (CM-Off)
		<b>Final</b> S5, Deep S5, G3/MeOff (CM-Off)
		<b>Trigger</b> Power Button override
	<b>Intel® AMT</b>	<b>Power Package</b> PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to AC+DC.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Verify that a DC battery is connected to the SUT, and that it is charged.</li><li>Set the SUT power source to <b>DC-only</b>.</li><li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li><li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Shutdown the SUT via the Host OS.</li><li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.</li></ol>	
Procedure	<ol style="list-style-type: none"><li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li><li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.</li></ol>	
Pass Criteria	The test passes, if the SUT ends the test in S5 (or Deep S5 or G3), and the Intel® ME is in MeOff (CM-Off). <b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5 (or Deep S5 or G3).	

ID	ME_PM_20.21
Title	S0/CM0 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP2)
Requirement	Mandatory <b>Exemptions</b>   <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3 via Power Button override with the parameters outlined below.
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.



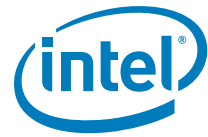
ID	ME_PM_20.21		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>When in S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries via the <b>WLAN</b> network interface.</li> </ul> </li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>		

ID	ME_PM_20.22		
Title	S3/CM3 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_20.22
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>When in S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries via the <b>WLAN</b> network interface.</li> </ul> </li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.23		
Title	S3/CM3-PG to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div> <div><input checked="" type="checkbox"/> Systems with a LAN-only network interface</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S3/MeOn (CM3)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_20.23
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>When in S5: <ul style="list-style-type: none"> <li>Intel® AMT on the SUT <b>does</b> respond to version queries via the <b>LAN</b> network interface, if available.</li> <li>Intel® AMT on the SUT <b>does not</b> respond to version queries via the <b>WLAN</b> network interface.</li> </ul> </li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.24		
Title	S4/CM3 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3 to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOn (CM3)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_20.24
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.25		
Title	S4/CM3-PG to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4,S5/MeOff (CM3-PG)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_20.25
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.26		
Title	S5/CM3-PG to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3-PG to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOff (CM3-PG)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)



ID	ME_PM_20.26
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.27		
Title	S5/CM3 to S5/CM3 via Power Button override (AC+DC, AC-only/PP2/LP2)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM3 via Power Button override with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S5/MeOn (CM3)
		Final	S5/MeOn (CM3)
		Trigger	Power Button override
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP2 (Enabled in S0)





ID	ME_PM_20.27
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface, if available.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version query via the <b>WLAN</b> network interface.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via a Power Button press for more than <b>5 seconds</b>.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>The Intel® ME is in MeOn (CM3).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul> <p><b>Note:</b> Some systems may briefly move electrically to S0 before final transition to S5.</p>

ID	ME_PM_20.28		
Title	S0/CM0 to G3/CM-Off via Power loss (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to G3/CM-Off via Power loss with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger	Power loss
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</div> <div>8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div>		



<b>ID</b>	<b>ME_PM_20.28</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Put the system to S5/ G3 via Unconditional Power Loss.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>
<b>Pass Criteria</b>	The test passes, if the SUT moves to S5 (or Deep S5 or G3) on unconditional Power Loss, and the Intel® ME moves to MeOff (CM-Off).

## 11.24 ME\_PM\_21 - S3/CM-Off (with/Intel® CSME Wake) to S3/CM-Off (Without Intel® CSME Wake)

ID	ME_PM_21.1		
Title	S3/CM3-PG with AC Wake to S3/CM3-PG with AC Wake via Intel® AMT idle timeout (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
			<input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3-PG to S3/CM-Off via Intel® AMT idle timeout with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode.		
	This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S3/CM3-PG
		Final	S3/CM3-PG
		Trigger	(AC-attach then) Intel® AMT idle timeout
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</div> <div>8. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</div> <div>9. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>10. Suspend the SUT via the Host OS.</div> <div>11. Verify that the SUT is in S3/(CM3-PG)with AC Wake.</div>		
Procedure	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>3. Verify that the SUT is in S3/MeOn (CM3).</div> <div>4. Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</div> <div>5. Verify that the SUT is in S3/CM3-PG.</div>		
Pass Criteria	<div>The test passes, if:</div> <div><div><div></div><div>The SUT remains in S3.</div></div><div><div></div><div>When in S3/MeOn (CM3), Intel® AMT responds to version queries via all available network interfaces.</div></div><div><div></div><div>The Intel® ME ends the test in MeOff (CM3-PG).</div></div></div>		



## 11.25 ME\_PM\_22 - S3/CM3-PG (with/ Intel® CSME Wake) to S3/CM-Off (Without Intel® CSME Wake)

ID	ME_PM_22.1	
<b>Title</b>	S3/CM3-PG to S3/CM3-PG with AC Wake via AC-detach (AC+DC/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b> <ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</li> <li><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</li> </ul>
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S3/CM3-PG to S3/CM-Off via AC-detach with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
<b>Parameters</b>	<b>System Power Source</b> AC+DC	
	<b>Power States</b>	<b>Initial</b> S3/CM3-PG
		<b>Final</b> S3/MeOff (CM-Off)
		<b>Trigger</b> (Intel® AMT idle timeout then) AC-detach
	<b>Intel® AMT</b>	<b>Power Package</b> PP2 (Intel® ME on in S0, wake in Sx/AC) <b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to DC-only.</li> <li>Verify that the SUT is in S3/(CM3-PG)with AC Wake.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> </ol>	
<b>Pass Criteria</b>	The test passes, if: <ul style="list-style-type: none"> <li>The SUT remains in S3.</li> <li>Intel® AMT does <b>not</b> respond to version queries via any available network interface.</li> <li>The Intel® ME ends the test in MeOff (CM-Off).</li> </ul>	



## 11.26 ME\_PM\_23 - G3 or S4-S5/CM-Off (Without Intel® CSME Wake) to S4-S5/CM-Off (with Intel® CSME Wake)

ID	ME_PM_23.1		
Title	S4/CM3-PG with AC Wake to S4/CM3-PG with AC Wake via Intel® AMT idle timeout (DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S4/CM3-PG to S4/CM3-PG via Intel® AMT idle timeout with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Final	S4,S5/MeOff (CM3-PG)
		Trigger	(AC-attach then) Intel® AMT idle timeout
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S4, S5/CM3-PG.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S4 or S5 (or moves to S4 or S5 from Deep S4, Deep S5, or G3).</li> <li>When in S4,S5/MeOn (CM3), Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Intel® ME ends the test in MeOff (CM3-PG).</li> </ul>		

ID	ME_PM_23.2		
Title	S5/CM3-PG to S5/CM3-PG via Intel® AMT idle timeout (AC+DC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems



ID	ME_PM_23.2	
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S5/CM3-PG to S5/CM3-PG via Intel® AMT idle timeout with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source	
	Power States	Initial S5, Deep S5, G3/MeOff (CM-Off)
		Final S5/MeOff (CM3-PG)
		Trigger (AC-attach then) Intel® AMT idle timeout
	Intel® AMT	Power Package PP2 (Intel® ME on in S0, wake in Sx/AC) WLAN Link Policy LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S5/CM3-PG.</li> </ol>	
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT remains in S5 (or moves to S5 from Deep S5 or G3).</li> <li>When in S5/MeOn (CM3), Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Intel® ME ends the test in MeOff (CM3-PG).</li> </ul>	

ID	ME_PM_23.3	
Title	G3/CM-Off to S5/CM3-PG via Intel® AMT idle timeout (AC+DC/PP2/LP3)	
Requirement	Mandatory	Exemptions <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from G3/CM-Off to S5/CM3-PG via Intel® AMT idle timeout with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. Confirm that the BIOS is configured to move the SUT to S5 from G3 upon AC-attach. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	



ID	ME_PM_23.3		
Parameters	System Power Source		AC+DC
	Power States	Initial	G3/MeOff (CM-Off)
		Final	S5/MeOff (CM3-PG)
		Trigger	(AC-attach then) Intel® AMT idle timeout
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S5/CM3-PG.</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves to S5.</li> <li>When in S5/MeOn (CM3), Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Intel® ME ends the test in MeOff (CM3-PG).</li> </ul>		



## 11.27 ME\_PM\_24 - S4-S5/CM-Off (with Intel® CSME Wake) to S4-S5/CM-Off (Without Intel® CSME Wake)

ID	ME_PM_24.1	
<b>Title</b>	S4/CM3-PG to S4/CM3-PG with AC Wake via AC-detach (AC+DC/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S4/CM3-PG to S4/CM-Off via AC-detach with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b> AC+DC	
	<b>Power States</b>	<b>Initial</b> S4,S5/MeOff (CM3-PG)
		<b>Final</b> S4,S5,Deep S4,Deep S5,G3/CM3-PG
		<b>Trigger</b> (Intel® AMT idle timeout then) AC-detach
	<b>Intel® AMT</b>	<b>Power Package</b> PP2 (Intel® ME on in S0, wake in Sx/AC) <b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to DC-only.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/CM3-PG with Ac Wake</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> </ol>	
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S4 or S5 (or moves to Deep S4, Deep S5, or G3).</li> <li>Intel® AMT does <b>not</b> respond to version queries via any available network interface.</li> <li>The Intel® ME ends the test in MeOff (CM3-PG) with AC Wake.</li> </ul>	

ID	ME_PM_24.2	
<b>Title</b>	S5/CM3-PG to S5/CM3-PG with AC Wake via AC-detach (AC+DC/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems



<b>ID</b>	<b>ME_PM_24.2</b>	
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S5/CM3-PG to S5/CM3-PG with Ac Wake via AC-detach with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	AC+DC
	<b>Power States</b>	<b>Initial</b> S5/MeOff (CM3-PG)
		<b>Final</b> S5,Deep S5,G3/CM3-PG with Ac wake
		<b>Trigger</b> (Intel® AMT idle timeout then) AC-detach
	<b>Intel® AMT</b>	<b>Power Package</b> PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM3-PG after Intel® AMT idle timeout.</li> <li>Verify that the Intel® ME on the SUT is in CM3-PG.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to DC-only.</li> <li>Verify that the SUT is in S5, Deep S5, G3/CM3-PG.with AC Wake.</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> </ol>	
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT remains in S5 (or moves to Deep S5 or G3).</li> <li>Intel® AMT <b>does not</b> respond to version queries via any available network interface.</li> <li>The Intel® ME ends the test in MeOff (CM3-PG) with AC Wake.</li> </ul>	





## 11.28 ME\_PM\_25 - S4-S5/CM-Off (Suspend Well Off) to S4-S5/CM-Off (with Host WoL) to S0/CM0 via Host WoL/WoWLAN

ID	ME_PM_25.1															
Title	S4/CM-Off to S0/CM0 via magic packet (DC-only/PP1/LP3)															
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> System without LAN support</div>													
Method	Automated by Intel® PETS															
Objective	This test checks the SUT power flow from S4/CM-Off to S0/CM0 via magic packet with the parameters outlined below.															
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that LAN-only network interfaces is available on the SUT. LAN shall be the initial active network interface in the test.</p>															
Parameters	<table><tr><th colspan="2">System Power Source</th><td>DC-only</td></tr><tr><th rowspan="3">Power States</th><th>Initial</th><td>S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)</td></tr><tr><th>Final</th><td>S0/MeOn (CM0, CM0-PG)</td></tr><tr><th>Trigger</th><td>Magic Packet receipt</td></tr><tr><th>Intel® AMT</th><th>Power Package</th><td>PP1 (Intel® ME on in S0)</td></tr></table>			System Power Source		DC-only	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)	Final	S0/MeOn (CM0, CM0-PG)	Trigger	Magic Packet receipt	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
System Power Source		DC-only														
Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)														
	Final	S0/MeOn (CM0, CM0-PG)														
	Trigger	Magic Packet receipt														
Intel® AMT	Power Package	PP1 (Intel® ME on in S0)														
Setup	<div><div>1.</div><div>Set the SUT power source to AC+DC.</div></div> <div><div>2.</div><div>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div></div> <div><div>3.</div><div>Verify that a DC battery is connected to the SUT, and that it is charged.</div></div> <div><div>4.</div><div>Set the SUT power source to <b>DC-only</b>.</div></div> <div><div>5.</div><div>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div></div> <div><div>6.</div><div>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</div></div> <div><div>7.</div><div>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div></div> <div><div>8.</div><div>Ensure yellow bang is not seen on Drivers in Device Manager</div></div>															
Procedure	<div><div>1.</div><div>Hibernate the SUT via the Host OS.</div></div> <div><div>2.</div><div>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</div></div> <div><div>3.</div><div>Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</div></div> <div><div>4.</div><div>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</div></div> <div><div>5.</div><div>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</div></div> <div><div>6.</div><div>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div></div> <div><div>7.</div><div>Verify that the Host OS on the SUT is available.</div></div> <div><div>8.</div><div>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div></div> <div><div>9.</div><div>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}</div></div> <div><div>10.</div><div>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</div></div> <div><div>11.</div><div>Ensure yellow bang is not seen on Drivers in Device Manager.</div></div> <div><div></div><div>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</div></div>															
Pass Criteria	<div>The test passes, if:</div> <div><div><div>•</div><div>The SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0.</div></div><div><div>•</div><div>The Intel® ME moves to MeOn (CM0).</div></div><div><div>•</div><div>Intel® AMT responds to version queries via LAN network interfaces.</div></div></div>															



ID	ME_PM_25.2		
Title	S5/CM-Off to S0/CM0 via magic packet (DC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
			<input checked="" type="checkbox"/> System without LAN support
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM-Off to S0/CM0 via magic packet with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li><li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S5, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to AC+DC.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Verify that a DC battery is connected to the SUT, and that it is charged.</li><li>Set the SUT power source to <b>DC-only</b>.</li><li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li><li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager</li></ol>		
Procedure	<ol style="list-style-type: none"><li>Shutdown the SUT via the Host OS.</li><li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li><li>Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li><li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li><li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li><li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>Verify that the Host OS on the SUT is available.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x6Qxxxxxx.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager</li></ol> <p>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</p>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"><li>The SUT moves from S5, (or Deep S5 or G3) to S0.</li><li>The Intel® ME moves to MeOn (CM0).</li><li>Intel® AMT responds to version queries via LAN network interfaces.</li></ul>		



ID	ME_PM_25.3	
Title	G3/CM-Off to S0/CM0 via magic packet (DC-only/PP1/LP3)	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems  <input checked="" type="checkbox"/> System without LAN support </div>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from G3/CM-Off to S0/CM0 via magic packet with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>Confirm that the Host OS is configured to shutdown the SUT upon Power Button press.</p> <p>This test assumes that LAN-only network interfaces are available on the SUT. Where network interfaces are available, LAN shall be the initial active network interface in the test.</p>	
Parameters	System Power Source	
	Power States	Initial G3/MeOff (CM-Off)
		Final S0/MeOn (CM0, CM0-PG)
		Trigger Magic Packet receipt
	Intel® AMT	Power Package PP1 (Intel® ME on in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol> <p>If LAN network interfaces are available, repeat this test procedure with the LAN interface set as the active network interface.</p>	
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT moves from S5, (or Deep S5 or G3) to S0.</li> <li>The Intel® ME moves to MeOn (CM0).</li> <li>Intel® AMT responds to version queries via LAN network interfaces.</li> </ul>	



## 11.29 ME\_PM\_26 - Warm Reset

ID	ME_PM_26.5	
Title	S0/CM0 to S0/CM0 via Reset Button press (or logic) (DC-only/PP1/LP3)	
Requirement	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Reset Button press (or logic) with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	<b>System Power Source</b> DC-only	
	<b>Power States</b>	<b>Initial</b> S0/MeOn (CM0, CM0-PG)
		<b>Final</b> S0/MeOn (CM0, CM0-PG)
		<b>Trigger</b> Reset Button press (or logic)
	<b>Intel® AMT</b>	<b>Power Package</b> PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to AC+DC.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>Verify that a DC battery is connected to the SUT, and that it is charged.</li><li>Set the SUT power source to <b>DC-only</b>.</li><li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li><li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager.</li></ol>	
Procedure	<ol style="list-style-type: none"><li>Perform a <b>warm reset</b> of the SUT by pressing the Reset Button. For designs without a Reset Button, access to the system reset logic should be prepared via blue wire.</li><li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x69xxxxxx.</li><li>Ensure yellow bang is not seen on Drivers in Device Manager</li></ol>	
Pass Criteria	The test passes, if: <ul style="list-style-type: none"><li>The SUT is reset to S0.</li><li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li><li>Intel® AMT responds to version queries via all available network interfaces.</li></ul>	

ID	ME_PM_26.6	
Title	S0/CM0 to S0/CM0 via Reset Button press (or logic) (AC+DC, AC-only/PP1/LP3)	
Requirement	Mandatory	<b>Exemptions</b>   None
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Reset Button press (or logic) with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	



ID	ME_PM_26.6	
Parameters	System Power Source	AC+DC or AC-only
	Power States	Initial S0/MeOn (CM0, CM0-PG)
		Final S0/MeOn (CM0, CM0-PG)
		Trigger Reset Button press (or logic)
	Intel® AMT	Power Package PP1 (Intel® ME on in S0)
		WLAN Link Policy LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Perform a <b>warm reset</b> of the SUT by pressing the Reset Button. For designs without a Reset Button, access to the system reset logic should be prepared via blue wire.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x69xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>	
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>	

ID	ME_PM_26.7	
Title	S0/CM0 to S0/CM0 via Reset Button press (or logic) (DC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Reset Button press (or logic) with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source	DC-only
	Power States	Initial S0/MeOn (CM0, CM0-PG)
		Final S0/MeOn (CM0, CM0-PG)
		Trigger Reset Button press (or logic)
	Intel® AMT	Power Package PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_26.7
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to AC+DC.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>4. Set the SUT power source to <b>DC-only</b>.</li> <li>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>8. Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Perform a <b>warm reset</b> of the SUT by pressing the Reset Button. For designs without a Reset Button, access to the system reset logic should be prepared via blue wire.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>3. Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li> <li>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>5. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x69xxxxxx.</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT is reset to S0.</li> <li>• The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>• Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_26.8		
Title	S0/CM0 to S0/CM0 via Reset Button press (or logic) (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Reset Button press (or logic) with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Reset Button press (or logic)
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<div>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>5. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>6. Ensure yellow bang is not seen on Drivers in Device Manager.</div>		



ID	ME_PM_26.8
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Perform a <b>warm reset</b> of the SUT by pressing the Reset Button. For designs without a Reset Button, access to the system reset logic should be prepared via blue wire.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>3. Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li> <li>4. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>5. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x69xxxxxx.</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT is reset to S0.</li> <li>• The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>• Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_26.9		
Title	S0/CM0 to S0/CM0 via Host OS restart (DC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Host OS restart with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Host OS restart
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<div>1. Set the SUT power source to AC+DC.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</div> <div>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>8. Ensure yellow bang is not seen on Drivers in Device Manager</div>		
Procedure	<div>1. Perform a <b>warm reset</b> of the SUT via Host OS graceful restart.</div> <div>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div> <div>3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>4. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x69xxxxx.</div> <div>5. Ensure yellow bang is not seen on Drivers in Device Manager</div>		
Pass Criteria	The test passes, if: <ul style="list-style-type: none"><li>The SUT is reset to S0.</li><li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li><li>Intel® AMT responds to version queries via all available network interfaces.</li></ul>		

ID	ME_PM_26.10
<b>Title</b>	S0/CM0 to S0/CM0 via Host OS restart (AC+DC, AC-only/PP1/LP3)



ID	ME_PM_26.10	
Requirement	Mandatory	Exemptions   None
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Host OS restart with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source   AC+DC or AC-only	
	Power States	Initial   S0/MeOn (CM0, CM0-PG)
		Final   S0/MeOn (CM0, CM0-PG)
		Trigger   Host OS restart
	Intel® AMT	Power Package   PP1 (Intel® ME on in S0)
		WLAN Link Policy   LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Perform a <b>warm reset</b> of the SUT via Host OS graceful restart.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x62xxxxxx.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>	
Pass Criteria	The test passes, if: <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>	

ID	ME_PM_26.11	
Title	S0/CM0 to S0/CM0 via Host OS restart (DC-only/PP2/LP3)	
Requirement	Mandatory	Exemptions   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Host OS restart with the parameters outlined below.	
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	System Power Source   DC-only	
	Power States	Initial   S0/MeOn (CM0, CM0-PG)
		Final   S0/MeOn (CM0, CM0-PG)
		Trigger   Host OS restart
	Intel® AMT	Power Package   PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy   LP3 (Enabled in S0, Sx/AC) where available





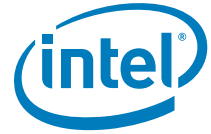
ID	ME_PM_26.11
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. Set the SUT power source to AC+DC.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>4. Set the SUT power source to <b>DC-only</b>.</li> <li>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>8. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Perform a <b>warm reset</b> of the SUT via Host OS graceful restart.</li> <li>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>4. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x69xxxxxx.</li> <li>5. Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Pass Criteria</b>	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>• The SUT is reset to S0.</li> <li>• The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>• Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_26.12		
Title	S0/CM0 to S0/CM0 via Host OS restart (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Host OS restart with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	Host OS restart
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<div>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>5. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>6. Ensure yellow bang is not seen on Drivers in Device Manager</div>		
Procedure	<div>1. Perform a <b>warm reset</b> of the SUT via Host OS graceful restart.</div> <div>2. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div> <div>3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>4. Verify that the second nibble of the FWSTS2 register on the SUT have a value of 0x69xxxxxx.</div> <div>5. Ensure yellow bang is not seen on Drivers in Device Manager.</div>		



ID	ME_PM_26.12
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> </ul>

ID	ME_PM_26.13		
Title	S0/CM0 to S0/CM0 via CF9 Warm Reset (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via CF9 Warm Reset with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0, CM0-PG)
		Final	S0/MeOn (CM0, CM0-PG)
		Trigger	CF9 Warm Reset
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>cleared to 0b</b>.</li> <li>Perform a <b>Warm reset</b> of the SUT by writing <b>6h</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding if the WLAN network interface is available. Because the Host OS may boot to error recovery screen following unexpected shutdown, the Host OS WLAN driver may not become available immediately. This delay allows enough time for Intel® AMT firmware to take control over the WLAN hardware and respond to manageability requests.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset, or that the Host OS is unavailable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>		
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0, CM0-PG).</li> <li>Intel® AMT responds to version queries via all available network interfaces.</li> <li>The Host OS last boot time <b>does not</b> match, or the Host OS is unavailable.</li> </ul>		



## 11.30 ME\_PM\_27 - S0/CM0 or Sx/Mx to G3

ID	ME_PM_27.1	
<b>Title</b>	S0/CM0 to G3/CM-Off via Power loss (AC+DC, AC-only/PP1/LP2)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   None
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to G3/CM-Off via Power loss with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
<b>Parameters</b>	<b>System Power Source</b> AC+DC or AC-only	
	<b>Power States</b>	<b>Initial</b> S0/MeOn (CM0, CM0-PG)
		<b>Final</b> G3/MeOff (CM-Off)
		<b>Trigger</b> Power loss
	<b>Intel® AMT</b>	<b>Power Package</b> PP1 (Intel® ME on in S0) <b>WLAN Link Policy</b> LP2 (Enabled in S0) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 2</b> (Enabled in S0), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> </ol>	
<b>Pass Criteria</b>	The test passes, if the SUT moves from S0 to G3, and the Intel® ME moves to MeOff (CM-Off).	

ID	ME_PM_27.2	
<b>Title</b>	S0/CM0 to G3/CM-Off via Power loss (AC+DC, AC-only/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   None
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to G3/CM-Off via Power loss with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
<b>Parameters</b>	<b>System Power Source</b> AC+DC or AC-only	
	<b>Power States</b>	<b>Initial</b> S0/MeOn (CM0, CM0-PG)
		<b>Final</b> G3/MeOff (CM-Off)
		<b>Trigger</b> Power loss
	<b>Intel® AMT</b>	<b>Power Package</b> PP2 (Intel® ME on in S0, wake in Sx/AC) <b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_27.2
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> </ol>
<b>Pass Criteria</b>	The test passes, if the SUT moves from S0 to G3, and the Intel® ME moves to MeOff (CM-Off).

ID	ME_PM_27.3		
<b>Title</b>	S5/CM3 to G3/CM-Off via Power loss after Host OS shutdown (AC+DC, AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S5/CM3 to G3/CM-Off via Power loss after Host OS shutdown with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S5/CM3
		<b>Final</b>	G3/MeOff (CM-Off)
		<b>Trigger</b>	Power loss
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> </ol>		
<b>Pass Criteria</b>	The test passes, if the SUT moves from S5 to G3, and the Intel® ME moves to MeOff (CM-Off).		



## 11.31 ME\_PM\_44 - S0/CM0-PG, CM0 to S4-S5/CM-Off

ID	ME_PM_44.3		
Title	S0/CM0-PG to S4/CM-Off via Host OS hibernate (DC-only)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction.		
Objective	This test checks the SUT power flow from S0/CM0-PG to S4/CM-Off via Host OS hibernate with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Trigger	Host OS hibernate
	Intel® AMT	Power Package WLAN Link Policy	[Intel® AMT is not provisioned.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> </ol>		
Pass Criteria	The test passes, if the SUT moves to S4, S5, Deep S4, Deep S5, or G3, and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_44.4		
Title	S0/CM0-PG to S4/CM-Off via Host OS hibernate (AC+DC, AC-only)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0-PG to S4/CM-Off via Host OS hibernate with the parameters outlined below.		



ID	ME_PM_44.4		
Configuration	<p>Intel® AMT should <b>not</b> be provisioned.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Trigger	Host OS hibernate
	Intel® AMT	Power Package	[Intel® AMT is not provisioned.]
WLAN Link Policy			
Setup	<ol style="list-style-type: none"><li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li><li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>3. Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li><li>4. Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li><li>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li><li>6. Verify that the Host OS on the SUT is available.</li><li>7. If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li><li>8. Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li><li>9. Verify that the SUT is in S0/MeOn (CM0-PG).</li></ol>		
Procedure	<ol style="list-style-type: none"><li>1. Hibernate the SUT via the Host OS.</li><li>2. Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li><li>3. If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li></ol>		
Pass Criteria	The test passes, if the SUT moves to S4, S5, Deep S4, Deep S5, or G3, and the Intel® ME moves to MeOff (CM-Off).		

ID	ME_PM_44.5	
Title	S0/CM0-PG to S5/CM-Off via Host OS shutdown (DC-only)	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems           <input checked="" type="checkbox"/> Systems with a LAN-only network interface         </div>
Method	Automated by Intel® PETS with potential Test Operator Interaction	
Objective	This test checks the SUT power flow from S0/CM0-PG to S5/CM-Off via Host OS shutdown with the parameters outlined below.	
Configuration	<p>Intel® AMT should <b>not</b> be provisioned.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	DC-only
	Power States	Initial S0/MeOn (CM0-PG)
		Final S5, Deep S5, G3/MeOff (CM-Off)
		Trigger Host OS shutdown
Intel® AMT	Power Package	[Intel® AMT is not provisioned.]
	WLAN Link Policy	



ID	ME_PM_44.5
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> </ol>
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).

ID	ME_PM_44.6	
Title	S0/CM0-PG to S5/CM-Off via Host OS shutdown (AC+DC, AC-only)	
Requirement	Mandatory	Exemptions   <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction	
Objective	This test checks the SUT power flow from S0/CM0-PG to S5/CM-Off via Host OS shutdown with the parameters outlined below.	
Configuration	<p>Intel® AMT should <b>not</b> be provisioned.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	Initial S0/MeOn (CM0-PG)
		Final S5, Deep S5, G3/MeOff (CM-Off)
		Trigger Host OS shutdown
	Intel® AMT	Power Package WLAN Link Policy [Intel® AMT is not provisioned.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> </ol>	



ID	ME_PM_44.6
Procedure	<ol style="list-style-type: none"> <li>1. Shutdown the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>3. If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> </ol>
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).

ID	ME_PM_44.7	
Title	S0/CM0 to S5/CM-Off via Host OS shutdown (AC+DC, AC-only/PP1/LP1)	
Requirement	Mandatory	
Method	Automated by Intel® PETS with potential Test Operator Interaction	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off via Host OS shutdown with the parameters outlined below.	
Configuration	<p>Intel® AMT should <b>not</b> be provisioned.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>• The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	AC+DC or AC-only	
	Power States	Initial
		S0/MeOn (CM0)
		Final
	Intel® AMT	S5, Deep S5, G3/MeOff (CM-Off)
		Trigger
		Host OS shutdown
	Intel® AMT	Power Package
		PP1 (Intel® ME on in S0)
	Intel® AMT	WLAN Link Policy
		LP1 (Disabled) where available
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0), and confirm that the Host OS is available.</li> <li>3. Ensure that Intel® AMT on the SUT <b>is provisioned</b>.</li> <li>4. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>5. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 1</b> (Disabled), if the WLAN network interface is available.</li> <li>6. Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li> <li>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>8. Verify that the Host OS on the SUT is available.</li> <li>9. Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM0-PG (as if it were allowed to enter the PG state).</li> <li>10. Verify that the SUT is in S0/MeOn (CM0).</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>1. Shutdown the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>	
Pass Criteria	The test passes, if the SUT moves to S5 (or Deep S5 or G3), and the Intel® ME moves to MeOff (CM-Off).	





## 11.32 ME\_PM\_45 - G3 or S4-S5/CM-Off to S0/CM0-PG, CM0

ID	ME_PM_45.3		
Title	S4/CM-Off to S0/CM0-PG via Power Button press (DC-only)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S4/CM-Off to S0/CM0-PG via Power Button press with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0-PG)
		Trigger	Power Button press
	Intel® AMT	Power Package WLAN Link Policy	[Intel® AMT is not provisioned.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	The test passes, if the SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0, and the Intel® ME moves to MeOn (CM0-PG).		

ID	ME_PM_45.4
Title	S4/CM-Off to S0/CM0-PG via magic packet (AC+DC, AC-only)



ID	ME_PM_45.4		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems without WoL and/or WoWLAN support <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S4/CM-Off to S0/CM0-PG via magic packet with the parameters outlined below.		
Configuration	<p>Intel® AMT should <b>not</b> be provisioned.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"><li>• The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li><li>• The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li></ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off)
		Final	S0/MeOn (CM0-PG)
		Trigger	Magic Packet receipt
	Intel® AMT	Power Package	[Intel® AMT is not provisioned.]
WLAN Link Policy			
Setup	<ol style="list-style-type: none"><li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li><li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li><li>3. Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li><li>4. Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li><li>5. Ensure that, where available, <b>only</b> the Host OS Wake on LAN and/or Wake on Wireless LAN driver setting(s) are <b>enabled</b> on the SUT. All other network wake sources must be <b>disabled</b>. This includes <b>enabling</b> ARP and/or NS Offload features where available to help prevent unexpected host wake events.</li><li>6. Verify that the Host OS on the SUT is available.</li><li>7. If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li><li>8. Ensure yellow bang is not seen on Drivers in Device Manager.</li></ol>		
Procedure	<ol style="list-style-type: none"><li>1. Hibernate the SUT via the Host OS.</li><li>2. Verify that the SUT is in S4, S5, Deep S4, Deep S5, G3/MeOff (CM-Off).</li><li>3. Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li><li>4. Verify that the SUT is in S0.</li><li>5. Verify that the Host OS on the SUT is available.</li><li>6. Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b></li><li>7. Verify that the SUT is in S0/MeOn (CM0-PG).</li><li>8. Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li><li>9. If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li><li>10. Ensure yellow bang is not seen on Drivers in Device Manager</li></ol>		
Pass Criteria	The test passes, if the SUT moves from S4, S5, Deep S4, Deep S5, or G3 to S0, and the Intel® ME moves to MeOn (CM0-PG).		



ID	ME_PM_45.5	
Title	S5/CM-Off to S0/CM0-PG via Power Button press (DC-only)	
Requirement	Mandatory	<b>Exemptions</b> <ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</li> <li><input checked="" type="checkbox"/> Systems with a LAN-only network interface</li> </ul>
Method	Automated by Intel® PETS with potential Test Operator Interaction	
Objective	This test checks the SUT power flow from S5/CM-Off to S0/CM0-PG via Power Button press with the parameters outlined below.	
Configuration	<p>Intel® AMT should <b>not</b> be provisioned.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
		WLAN Link Policy
	[Intel® AMT is not provisioned.]	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b></li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>	
Pass Criteria	The test passes, if the SUT moves from S5 (or Deep S5 or G3) to S0, and the Intel® ME moves to MeOn (CM0-PG).	
ID	ME_PM_45.7	
Title	G3/CM-Off to S0/CM0-PG via Power Button press (DC-only)	
Requirement	Mandatory	<b>Exemptions</b> <ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</li> <li><input checked="" type="checkbox"/> Systems with a LAN-only network interface</li> </ul>
Method	Automated by Intel® PETS with potential Test Operator Interaction	
Objective	This test checks the SUT power flow from G3/CM-Off to S0/CM0-PG via Power Button press with the parameters outlined below.	



ID	ME_PM_45.7	
Configuration	<p>Intel® AMT should <b>not</b> be provisioned.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
		WLAN Link Policy
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Remove power from the SUT via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to DC-only.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the SUT moves from G3 through S5 (or Deep S5 or G3) to S0, and the Intel® ME moves to MeOn (CM0-PG).	



## 11.33 ME\_PM\_46 - S0/CM0-PG, CM0 to S0/CM0-PG, CM0

ID	ME_PM_46.1		
Title	S0/CM0-PG to S0/CM0-PG via Host OS restart (DC-only)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0-PG to S0/CM0-PG via Host OS restart with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S0/MeOn (CM0-PG)
		Trigger	Host OS restart
	Intel® AMT	Power Package WLAN Link Policy	[Intel® AMT is not provisioned.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned. If SUT is provisioned, we have to unprovision and wait for 3 minutes for RSA key readiness, If SUT is not provisioned, no wait is needed.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Perform a <b>warm reset</b> of the SUT via Host OS graceful restart.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	The test passes, if the SUT is reset to S0, and the Intel® ME is available in MeOn (CM0-PG).		

ID	ME_PM_46.2		
Title	S0/CM0-PG to S0/CM0-PG via Host OS restart (AC+DC, AC-only)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0-PG to S0/CM0-PG via Host OS restart with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		



ID	ME_PM_46.2		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S0/MeOn (CM0-PG)
		Trigger	Host OS restart
	Intel® AMT	Power Package WLAN Link Policy	[Intel® AMT is not provisioned.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Perform a <b>warm reset</b> of the SUT via Host OS graceful restart.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	The test passes, if the SUT is reset to S0, and the Intel® ME is available in MeOn (CM0-PG).		

ID	ME_PM_46.3		
Title	S0/CM0-PG to S0/CM0-PG via CF9 Cold Reset (DC-only)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0-PG to S0/CM0-PG via CF9 Cold Reset with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S0/MeOn (CM0-PG)
		Trigger	CF9 Cold Reset
	Intel® AMT	Power Package WLAN Link Policy	[Intel® AMT is not provisioned.]



ID	ME_PM_46.3
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>cleared to 0b</b>.</li> <li>Perform a <b>cold reset</b> of the SUT by writing <b>Eh</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0-PG).</li> <li>The Host OS last boot time <b>does not</b> match.</li> </ul>

ID	ME_PM_46.4		
Title	S0/CM0-PG to S0/CM0-PG via CF9 Cold Reset (AC+DC, AC-only)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Systems with a LAN-only network interface
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0-PG to S0/CM0-PG via CF9 Cold Reset with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S0/MeOn (CM0-PG)
		Trigger	CF9 Cold Reset
	Intel® AMT	Power Package	[Intel® AMT is not provisioned.]
WLAN Link Policy			



ID	ME_PM_46.4
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>cleared to 0b</b>.</li> <li>Perform a <b>cold reset</b> of the SUT by writing <b>Eh</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0-PG).</li> <li>The Host OS last boot time <b>does not</b> match.</li> </ul>

ID	ME_PM_46.5		
Title	S0/CM0-PG to S0/CM0-PG via CF9 Global Reset (DC-only)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Systems with a LAN-only network interface</div> <div><input checked="" type="checkbox"/> Systems not in Intel® ME manufacturing mode</div>
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0-PG to S0/CM0-PG via CF9 Global Reset with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. Intel® ME should be configured in manufacturing mode. Confirm that the BIOS has <b>not set</b> the CF9 Lockdown. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S0/MeOn (CM0-PG)
		Trigger	CF9 Global Reset
	Intel® AMT	Power Package	[Intel® AMT is not provisioned.]
		WLAN Link Policy	





ID	ME_PM_46.5
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to AC+DC.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC or DC power.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>Verify that the Intel® ME is configured in manufacturing mode.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>Write 1b to CF6GR to enable global Reset.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>set</b> to <b>1b</b> to enable global reset.</li> <li>Perform a <b>global reset</b> of the SUT by writing either <b>6h</b> or <b>Eh</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b>.</li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0-PG).</li> <li>The Host OS last boot time <b>does not</b> match.</li> </ul>

ID	ME_PM_46.6		
Title	S0/CM0-PG to S0/CM0-PG via CF9 Global Reset (AC+DC, AC-only)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Systems with a LAN-only network interface</div> <div><input checked="" type="checkbox"/> Systems not in Intel® ME manufacturing mode</div>
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0-PG to S0/CM0-PG via CF9 Global Reset with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. Intel® ME should be configured in manufacturing mode. Confirm that the BIOS has <b>not set</b> the CF9 Lockdown. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0-PG)
		Final	S0/MeOn (CM0-PG)
		Trigger	CF9 Global Reset
	Intel® AMT	Power Package	[Intel® AMT is not provisioned.]
		WLAN Link Policy	



ID	ME_PM_46.6
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Ensure that Intel® AMT on the SUT is <b>not</b> provisioned.</li> <li>Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Record the Host OS last boot time on the SUT (to verify reset execution).</li> <li>Verify that the Intel® ME is configured in manufacturing mode.</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to disconnect the LAN cable. The Intel® ME may not move to a power gated state while the LAN is physically connected.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b></li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>Write 1b to CF6GR to enable global Reset.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>Ensure that CF9h Global Reset (CF9GR) is <b>set</b> to <b>1b</b> to enable global reset.</li> <li>Perform a <b>global reset</b> of the SUT by writing either <b>6h</b> or <b>Eh</b> to I/O register CF9h.</li> <li>Verify that the SUT is in S0.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT <b>does not</b> match the boot time recorded before reset.</li> <li>Check that Intel® ME is in CM0-PG state for more than 50% within a time interval of <b>1 minute</b></li> <li>Verify that the SUT is in S0/MeOn (CM0-PG).</li> <li>If the SUT supports LAN connectivity, Test Operator Interaction may require to reconnect the LAN cable.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>
Pass Criteria	<p>The test passes, if:</p> <ul style="list-style-type: none"> <li>The SUT is reset to S0.</li> <li>The Intel® ME is available in MeOn (CM0-PG).</li> <li>The Host OS last boot time <b>does not</b> match.</li> </ul>

ID	ME_PM_46.7		
Title	S0/CM0 to S0/CM0 via Host OS restart (AC+DC, AC-only)		
Requirement	Mandatory		
Method	Automated by Intel® PETS with potential Test Operator Interaction		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Host OS restart with the parameters outlined below.		
Configuration	Intel® AMT should <b>not</b> be provisioned. This test assumes that either WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0)
		Final	S0/MeOn (CM0)
		Trigger	Host OS restart
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP1 (Disabled) where available



ID	ME_PM_46.7
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Ensure that Intel® AMT on the SUT <b>is provisioned</b>.</li> <li>4. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>5. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 1</b> (Disabled), if the WLAN network interface is available.</li> <li>6. Ensure that the Host OS is configured to <b>not</b> sleep on either AC (or DC, where available) power source configuration.</li> <li>7. Verify that the Host OS on the SUT is available.</li> <li>8. Ensure yellow bang is not seen on Drivers in Device Manager.</li> <li>9. Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM0-PG (as if it were allowed to enter the PG state).</li> <li>10. Verify that the SUT is in S0/MeOn (CM0).</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Perform a <b>warm reset</b> of the SUT via Host OS graceful restart.</li> <li>2. Verify that the SUT is in S0.</li> <li>3. Verify that the Host OS on the SUT is available.</li> <li>4. Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to CM0-PG (as if it were allowed to enter the PG state).</li> <li>5. Verify that the SUT is in S0/MeOn (CM0).</li> <li>6. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	The test passes, if the SUT is reset to S0, and the Intel® ME is available in MeOn (CM0).



## 11.34 ME\_PM\_50 - S0/CM0 to Sx/(CM3 or CM-Off) to S0/CM0 via AC Attach

ID	ME_PM_50.1		
Title	S0/CM0 to S3/CM3 to S0/CM0 via AC-attach (PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM3 to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S3 state
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return to S3).</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	The test passes, if the Intel® ME functions properly when AC Source attached in S3 state.		

ID	ME_PM_50.2		
Title	S0/CM0 to S4/CM3 to S0/CM0 via AC-attach (PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		



ID	ME_PM_50.2	
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM3 to S0/CM0 via AC-attach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
		WLAN Link Policy
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S4/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME functions properly when AC Source attached in S4 state.	
ID	ME_PM_50.3	
Title	S0/CM0 to S5/CM3 to S0/CM0 via AC-attach (PP2/LP3)	
Requirement	Mandatory	Exemptions
		<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3 to S0/CM0 via AC-attach with the parameters outlined below.	



ID	ME_PM_50.3	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source DC-only	
	Power States	Initial S0/MeOn (CM0)
		Final S0/MeOn (CM0)
		Trigger AC-attach in S5 state
	Intel® AMT	Power Package PP2 (Intel® ME on in S0, wake in Sx/AC) WLAN Link Policy LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME functions properly when AC Source attached in S5 state.	

ID	ME_PM_50.4	
Title	S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach (PP1)	
Requirement	Mandatory	Exemptions <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	



ID	ME_PM_50.4		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S3 state
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to DC-only.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return to S3).</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	The test passes, if the Intel® ME functions properly i.e. stays MeOff when AC Source attached in S3 state.		

ID	ME_PM_50.5		
Title	S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach (PP1)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S4 state
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available



ID	ME_PM_50.5	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME functions properly i.e. stays MEOff when AC Source attached in S4 state.	

ID	ME_PM_50.6	
Title	S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach (PP1)	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems  <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems </div>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	DC-only
		Initial S0/MeOn (CM0)
		Final S0/MeOn (CM0)
	Trigger	
Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
	WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available





ID	ME_PM_50.6	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>Verify that Intel® AMT on the SUT <b>does not</b> respond to version queries via <b>any</b> of the available network interfaces.</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME functions properly i.e. stays MeOff when AC Source attached in S5 state.	

ID	ME_PM_50.7	
Title	S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach	
Requirement	Mandatory	<b>Exemptions</b> <ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</li> <li><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</li> </ul>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
Configuration	Intel® AMT should be not provisioned. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	<b>System Power Source</b>	
	<b>Power States</b>	<b>Initial</b> S0/MeOn (CM0)
		<b>Final</b> S0/MeOn (CM0)
		<b>Trigger</b> AC-attach in S3 state
	<b>Intel® AMT</b>	<b>Power Package</b> [Intel® AMT is not provisioned.]
		<b>WLAN Link Policy</b> [Intel® AMT is not provisioned.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure Intel (R) AMT is not provisioned.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return to S3)</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	



ID	ME_PM_50.7	
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME functions properly i.e. stays MeOff when AC Source attached in S3 state.	

ID	ME_PM_50.8	
Title	S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems  <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems </div>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be not provisioned</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	DC-only
		Initial S0/MeOn (CM0)
		Final S0/MeOn (CM0)
	Intel® AMT	Trigger AC-attach in S4 state
		Power Package [Intel® AMT is not provisioned.]
		WLAN Link Policy [Intel® AMT is not provisioned.]
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure Intel (R) AMT is not provisioned.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME functions properly i.e. stays MeOff when AC Source attached in S4 state.	



ID	ME_PM_50.9	
Title	S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach	
Requirement	Mandatory	<b>Exemptions</b> <ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</li> <li><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</li> </ul>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
Configuration	Intel® AMT should be not provisioned If Deep S5 and/or G3 are supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
Parameters	<b>System Power Source</b>	
	<b>Power States</b>	<b>Initial</b> S0/MeOn (CM0)
		<b>Final</b> S0/MeOn (CM0)
		<b>Trigger</b> AC-attach in S5 state
	<b>Intel® AMT</b>	<b>Power Package</b> [Intel® AMT is not provisioned.]
		<b>WLAN Link Policy</b> [Intel® AMT is not provisioned.]
Setup	1. Set the SUT power source to <b>AC+DC</b> . 2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available. 3. Verify that a DC battery is connected to the SUT, and that it is charged. 4. Set the SUT power source to <b>DC-only</b> . 5. Ensure Intel (R) AMT is not provisioned. 6. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b> , if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS. 7. Ensure yellow bang is not seen on Drivers in Device Manager.	
Procedure	1. Shutdown the SUT via the Host OS. 2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off). 3. Set the SUT power source to AC+DC. 4. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off). 5. Briefly press the Power Button on the SUT. 6. Verify that the SUT is in S0/MeOn (CM0,CM0-PG). 7. Verify that the Host OS on the SUT is available. 8. Ensure yellow bang is not seen on Drivers in Device Manager	
Pass Criteria	The test passes, if the Intel® ME functions properly i.e. stays MeOff when AC Source attached in S5 state.	



## 11.35 ME\_PM\_51 - S0/CM0 to Sx/CM-Off to S0/CM0 via AC Detach in Sx State

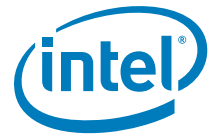
ID	ME_PM_51.1		
Title	S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach (PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Final	S0/MeOn (CM0)
		Trigger	AC-detach in S3 state
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return to S3).</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>		
Pass Criteria	The test passes, if the Intel® ME becomes Me-Off when AC Detached in S3 state and becomes MeOn after AC attached in S3 state.		
ID	ME_PM_51.2		
Title	S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach (PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems
Method	Automated by Intel® PETS		



ID	ME_PM_51.2	
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
		WLAN Link Policy
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOn (CM3).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S4/MeOn (CM3).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME becomes Me-Off when AC Detached in S4 state and becomes MeOn after AC attached in S4 state.	
ID	ME_PM_51.3	
Title	S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach (PP2/LP3)	
Requirement	Mandatory	<b>Exemptions</b> <ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</li> <li><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</li> </ul>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	



ID	ME_PM_51.3		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Final	S0/MeOn (CM0)
		Trigger	AC-detach in S5 state
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	
Setup	<div>1. Set the SUT power source to <b>AC+DC</b>.</div> <div>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</div> <div>3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME in S0, wake in Sx/AC).</div> <div>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</div> <div>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</div> <div>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>7. Ensure yellow bang is not seen on Drivers in Device Manager</div>		
Procedure	<div>1. Shutdown the SUT via the Host OS.</div> <div>2. Verify that the SUT is in S5/MeOn (CM3).</div> <div>3. Verify that a DC battery is connected to the SUT, and that it is charged.</div> <div>4. Set the SUT power source to <b>DC-only</b>.</div> <div>5. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</div> <div>6. Set the SUT power source to AC+DC.</div> <div>7. Verify that the SUT is in S5/MeOn (CM3).</div> <div>8. Briefly press the Power Button on the SUT.</div> <div>9. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</div> <div>10. Verify that the Host OS on the SUT is available.</div> <div>11. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</div> <div>12. Ensure yellow bang is not seen on Drivers in Device Manager.</div>		
Pass Criteria	The test passes, if the Intel® ME becomes Me-Off when AC Detached in S5 state and becomes MeOn after AC attached in S5 state.		
ID	ME_PM_51.4		
Title	S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach (PP1)		
Requirement	Mandatory	Exemptions	<div><input checked="" type="checkbox"/> Non-Mobile (AC-only) systems</div> <div><input checked="" type="checkbox"/> Modern Standby and InstantGo* systems</div>
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Final	S0/MeOn (CM0)
		Trigger	AC-detach in S3 state
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
WLAN Link Policy		LP3 (Enabled in S0, Sx/AC) where available	



ID	ME_PM_51.4	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return to S3).</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME stays MeOff when Ac Detached in S3 state and stays MeOff when attached AC Source in S3 state.	

ID	ME_PM_51.5	
Title	S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach (PP1)	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems  <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems </div>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4, Deep S5, and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
		WLAN Link Policy



ID	ME_PM_51.5	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "run the following power shell command": Get-WinEvent -ProviderName Microsoft-Windows-Kernel-boot -MaxEvents 10   Where-Object {\$_.message -like "The boot type*"}.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>	
Pass Criteria	The test passes, if the Intel® ME stays MeOff when Ac Detached in S4 state and stays MeOff when attached AC Source in S4 state.	

ID	ME_PM_51.6	
Title	S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach (PP1)	
Requirement	Mandatory	<div>Exemptions</div> <div> <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems  <input checked="" type="checkbox"/> Modern Standby and InstantGo* systems </div>
Method	Automated by Intel® PETS	
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 and/or G3 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 or G3 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
Parameters	System Power Source	
	Power States	DC-only
		Initial S0/MeOn (CM0)
		Final S0/MeOn (CM0)
	Trigger AC-detach in S5 state	
Intel® AMT	Power Package PP1 (Intel® ME on in S0)	
	WLAN Link Policy LP3 (Enabled in S0, Sx/AC) where available	





ID	ME_PM_51.6
Setup	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>5. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available. In addition, ensure that WOWLAN setting is disabled in the BIOS.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Procedure	<ol style="list-style-type: none"> <li>1. Suspend the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>3. Verify that a DC battery is connected to the SUT, and that it is charged.</li> <li>4. Set the SUT power source to <b>DC-only</b>.</li> <li>5. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>6. Set the SUT power source to AC+DC.</li> <li>7. Verify that the SUT is in S5, Deep S5, G3/MeOff (CM-Off).</li> <li>8. Briefly press the Power Button on the SUT.</li> <li>9. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>10. Verify that the Host OS on the SUT is available.</li> <li>11. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>12. Ensure yellow bang is not seen on Drivers in Device Manager.</li> </ol>
Pass Criteria	The test passes, if the Intel® ME stays MeOff when Ac Detached in S5 state and stays MeOff when attached AC Source in S5 state.

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## 12 Intel® CSME Power Management for Corporate Designs—Stress Testing

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This chapter covers system power flow transitions, which involve the Intel® ME firmware (and/or software). Intel® Active Management Technology (Intel® AMT), as an application operating within in the Intel® ME, related configurations and flows found in Corporate designs are also included herein. The tests in this chapter are specifically intended to cover topics related to stress testing of the System Under Test (SUT).

### 12.1 System Power States

The following section describes power states that exist beyond the standard ACPI System Level Sx (S0, S3, S4, and S5) system S-states. Refer the main Power Management chapter for further details on Deep Sx and Intel® ME Power Gating.

### 12.2 Test Environment and System Configuration

Each test in this chapter contains a section outlining the test configuration.

Unless, where stated otherwise, Intel® AMT should be provisioned.

Because of the nature of the stress test and the flows that run, some tests are better suited for execution in an environment, where the SUT is configured to boot to DOS (via USB Key) or UEFI Shell. These tests are designated by the "(DOS/UEFI)" tag on their name as well as description in the test configuration.

The Intel® AMT networking interface used by the test, if any, is documented in the test configuration section as well. 'LAN' and 'WLAN' indicate that the test is explicitly using the respective LAN and/or wireless LAN (WLAN) interface. Some tests may have a combination of targeted network configurations. Example: WLAN-only and/or LAN+WLAN.

The test should be run on the SUT only in the case, where a matching network configuration is described.

**Note:** Not all Workstation and Intel® AMT Server designs may have Intel® AMT wireless LAN interface support.

Other details about the configuration of the SUT are described on a per-test basis. Refer the test contents for details.

#### 12.2.1 Test Parameters

Each test in this chapter contains a table describing the system configuration to which the test is applicable. Below are some example test parameters blocks:



<b>System Power Source</b>		AC+DC or AC-only
<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0,CM0-PG)
	<b>Final</b>	S0/MeOn (CM0,CM0-PG)
	<b>Trigger</b>	Remote Power Cycle
<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
	<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available

**Example 1:** Two-state with single trigger.

<b>System Power Source</b>		AC+DC or AC-only
<b>Power States</b>	<b>Initial</b>	S5/MeOn (CM3)
	<b>Middle</b>	G3/MeOff (CM-Off)
	<b>Final</b>	S5/MeOn (CM3)
	<b>Trigger</b>	Power loss → Power attach
<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
	<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available

**Example 2:** Three-state with double trigger**System Power Source:**

Describes the initial power source configuration of the system. Can be one of 'AC-only', 'DC-only', 'AC+DC', 'AC+DC,AC-only' (AC+DC or AC-only). The system may transition to different power source configurations during the test.

**Power States:**

Describes the 'Initial', 'Middle' (where applicable), and 'Final' power states of the SUT. The description is provided in terms of basic ACPI Sx states (S0, S3, S4, S5, G3) as well as Intel® ME availability ('MeOn' or 'MeOff'). Exact detail of system power states, including Deep Sx and/or Intel® ME power gating availability, is provided in each test. Included is also the 'Trigger' used to initiate the power flow transition. Many tests are limited one trigger, but some tests have two.

**Intel® AMT:**

Describes the 'Power Package' and 'WLAN Link Policy' (where available and applicable) that apply to the test. The Power Package controls, when manageability is available on the SUT and what power states the SUT and particularly the Intel® ME may transition to and from. The WLAN Link Policy describes, relative to Wireless LAN support, when manageability is available via Intel® AMT Wireless Networking support.

## 12.2.2 Tools for Testing

The following tools, as provided by Intel, may be used to execute automated tests listed herein:

- Intel® PETS: The latest version of the tool from the Intel® ME Compliancy and Debug kit release. Refer to the Intel® PETS User Guide for exact instructions on how to load and setup the Intel® PETS software.
- Intel® Automated Power Switch (Intel® APS): The SUT should be connected to an Intel® APS 3 unit. In case an Intel® APS 3 is not available, select the Manual configuration in the Intel® PETS SUT profile configuration menu.
- Intel® PETS Local Agent: The local agent must be installed on the SUT.



### 12.2.3 Test Environment Setup

The SUT is to be configured with Intel® AMT set in manual provisioning mode with static IP address or DHCP. The management console may be a laptop or a desktop with a version of Microsoft\* Windows supported by Intel® Platform Enablement Test Suite (Intel® PETS), and the SUT should have a version of Microsoft\* Windows supported by Intel® PETS as well. The test network is comprised of a hub/switch and network cables. The SUT should have only one HDD.

While completing tests within this chapter, especially those which send the system to a specific S-state (S3, S4, S5, Deep Sx, etc.), it is important to ensure that the network wake events are properly configured for each applicable device (LAN and/or WLAN).

If not properly configured, the system may wake from a given S-state unexpectedly during test execution as a result of various network traffic within the test environment, and cause the test to result in a *false failure*.

The following Host OS LAN/WLAN driver settings allow the network device to process specific network frames **without** waking the system, where supported.

- Address Resolution Protocol (ARP) offload should be **enabled**
- Neighbor Solicitation (NS) offload should be **enabled**

The following Host OS LAN/WLAN driver settings allow the network device to wake the system, where supported, when specific network frames are received.

- Wake on Magic Packet should be **disabled**
- Wake on Pattern Match should be **disabled**
- Wake on Magic Packet from power off state should be **disabled**

**Note:** The wording used for the Host OS driver settings above may vary, and in some cases may not be available depending on driver support or system configuration.

Beyond the guidance in this section, refer individual test setup information for details on specifically, when to enable relevant wake functionality in the network device, as applicable to the test. In all other cases, the above settings should be applied by default.

### 12.2.4 Test Step Execution and Verification

The tests described in this chapter contain test steps, which are executed by Intel® PETS. While Intel® PETS brings a certain level of convenience and speed to the testing process, there are times where manual verification of steps is critical toward issue triage and debug.

Review the Test Step Execution and Verification section found in the main Intel® ME Power Management chapter before starting any test in this chapter.

The tests in this chapter are designed to run individually through a large number of iterations. Some of them require changing the system configuration before run. When performing very large numbers of iterations, the tests may take many hours, and in some cases several days.

Intel validation runs each of these tests, the number of iterations indicated. Each OEM should decide on the tolerance level required for their boards, and choose an appropriate number of iterations.



The tests in this section are not designed to run automatically one after the other, the test operator must place the SUT into the appropriate starting state, and then run the test in cycle. However each test individually ends with the SUT in the same state as when it started, allowing for easy iteration.

Apart from where explicitly mentioned, the Intel® AMT idle timeout value should be set larger than 1 minute to ensure the system does not pass the timeout before the required state is verified.

Tests that require the Intel® AMT idle timeout may fail if there is noise on the network preventing the Intel® ME from entering an idle state. Ensure that routers with spanning tree, for example, are not present on the test network.

If the platform is configured with Deep Sx or SUS Well Down enabled (on mobile platforms), according to the enabled Deep Sx S-state (Deep S4/S5), expect the Intel® ME to transition to CM-Off, when reaching that specific Sx state.

When running long iterations, ensure that the management console is set not to go to sleep, as this will pause the test.

Ensure that the SUT can boot to the designated Host OS without prompting the test operator for any actions (such as, scanning drivers and so forth); as this will affect stress tests, which boot the SUT to the Host OS.

Following Test step has been added to Power Flows, which ends at S0 state resuming back from S4 Hibernation. This will ensure System resumed from S4 state only and no other Sx state.

Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10 | where-Object{\$\_.message -like "The boot type\*"}

### 12.2.5 Setup Environment Tests

Review the Setup Environment Tests section found in the main Intel® ME Power Management chapter before starting any test in this chapter. Those tests are also valid for confirming basic test environment configuration and should be run before any other automated test described in this chapter.

Because Intel® AMT is provisioned in many of the tests in this chapter, it is strongly recommended to run the Setup Environment Tests for that technology as well before running any test in this chapter.

## 12.3 Stress Test Coverage Summary

### Test Requirements:

In general, all **applicable** tests are considered Mandatory in this section except for those specifically described as Optional or those which meet an Exemption. Refer the test Requirement section for details on test applicability.

### Form Factor:

Mobile designs are broadly covered by the tests in this chapter, Desktop, All-in-One, and Workstation designs are Exempted, where classified as Non-Mobile (AC-only) systems. Refer the test Requirement section for Exemption details.

**System Power Model:**

Tests, which involve S3 flows will not support Modern Standby or Microsoft\* Windows InstantGo. Refer the test Requirement section for Exemption details.

**Network Configuration:**

In general, all tests may run on systems with any combination of LAN and/or WLAN network interface support. For tests that work with a subset of configurations, such as LAN-only or LAN+WLAN. Refer the test Configuration section for details.

**Methodology:**

All tests are implemented in the Intel® PETS PM\_Stress\_Testing.xml test package.

Test ID	Test Case Title	SUT Boot Target
PM_ST_1	S5/CM3 to G3 to S5/CM3 via Power Cycle (DOS/UEFI)	DOS* or UEFI Shell*
PM_ST_2	Remote Power Cycle S0/CM0 (DOS/UEFI)	DOS* or UEFI Shell*
PM_ST_3	Remote Reset S0/CM0 (DOS/UEFI)	DOS* or UEFI Shell*
PM_ST_4	S3/CM3 to S3/CM-Off to S3/CM3 via AC-detach/attach	Microsoft* Windows
PM_ST_5	S0/CM0 to S3/CM-Off to S0/CM0 via Suspend/Resume	Microsoft* Windows
PM_ST_6	S0/CM0 to S3/CM3 to S0/CM0 via Suspend/Resume	Microsoft* Windows
PM_ST_7	S0/CM0 to S5/CM3 to S0/CM0 via Power Button Override (DOS/UEFI)	DOS* or UEFI Shell*
PM_ST_8	S0/CM0 to S4/CM-Off to S0/CM0 via Hibernate and WoL/WoWLAN	Microsoft* Windows
PM_ST_9	S0/CM0 to S4/CM3 to S0/CM0 via Hibernate and Remote Power-Up	Microsoft* Windows
PM_ST_10	S0/CM0 to S5/CM-Off to S0/CM0 via Shutdown and Power Button press	Microsoft* Windows
PM_ST_11	S0/CM0 to S5/CM3 to S0/CM0 via Shutdown and Remote Power-Up	Microsoft* Windows
PM_ST_12	S3/CM3 to S3/CM-Off to S3/CM3 via Intel® AMT idle timeout and Intel® AMT network access	Microsoft* Windows
PM_ST_13	S0/CM0 to S3/CM3 to S0/CM0 via Suspend and Remote Power-Up	Microsoft* Windows
PM_ST_14	S0/CM0 to S3/CM-Off to S0/CM0 via Suspend and Power Button press	Microsoft* Windows
PM_ST_16	Remote Power Cycle S0/CM0 (DOS/UEFI)	DOS* or UEFI Shell*
PM_ST_17	Remote Reset S0/CM0 (DOS/UEFI)	DOS* or UEFI Shell*
PM_ST_18	S5/CM3 to S5/CM-Off to S5/CM3 via AC-detach/attach	Microsoft* Windows
PM_ST_19	S5/CM3 to S5/CM-Off to S5/CM3 via Intel® AMT idle timeout and Intel® AMT network access	Microsoft* Windows
PM_ST_20	S0/CM0 to S3/CM3 to S0/CM0 via AC Attach (PP2)	Microsoft* Windows
PM_ST_21	S0/CM0 to S4/CM3 to S0/CM0 via AC Attach (PP2)	Microsoft* Windows
PM_ST_22	S0/CM0 to S5/CM3 to S0/CM0 via AC Attach (PP2)	Microsoft* Windows
PM_ST_23	S0/CM0 to S3/CM-Off to S0/CM0 via AC Attach (PP1)	Microsoft* Windows
PM_ST_24	S0/CM0 to S4/CM-Off to S0/CM0 via AC Attach (PP1)	Microsoft* Windows
PM_ST_25	S0/CM0 to S5/CM-Off to S0/CM0 via AC Attach (PP1)	Microsoft* Windows
PM_ST_26	S0/CM0 to S3/CM-Off to S0/CM0 via AC Attach	Microsoft* Windows
PM_ST_27	S0/CM0 to S4/CM-Off to S0/CM0 via AC Attach	Microsoft* Windows
PM_ST_28	S0/CM0 to S5/CM-Off to S0/CM0 via AC Attach	Microsoft* Windows
PM_ST_29	S0/CM0 to S3/CM-Off to S0/CM0 via AC Detach (PP2)	Microsoft* Windows
PM_ST_30	S0/CM0 to S4/CM-Off to S0/CM0 via AC Detach (PP2)	Microsoft* Windows
PM_ST_31	S0/CM0 to S5/CM-Off to S0/CM0 via AC Detach (PP2)	Microsoft* Windows
PM_ST_32	S0/CM0 to S3/CM-Off to S0/CM0 via AC Detach (PP1)	Microsoft* Windows
PM_ST_33	S0/CM0 to S4/CM-Off to S0/CM0 via AC Detach (PP1)	Microsoft* Windows
PM_ST_34	S0/CM0 to S5/CM-Off to S0/CM0 via AC Detach (PP1)	Microsoft* Windows



## 12.4 PM\_ST\_1 - S5/CM3 to G3 to S5/CM3 via Power Cycle (DOS/UEFI)

ID	PM_ST_1		
<b>Title</b>	S5/CM3 to G3/CM-Off to S5/CM3 via power cycle (AC+DC,AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S5/CM3 to G3/CM-Off to S5/CM3 via power cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. The SUT should be configured to boot to either DOS (via USB key) or UEFI shell. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S5/MeOn (CM3)
		<b>Middle</b>	G3/MeOff (CM-Off)
		<b>Final</b>	S5/MeOn (CM3)
		<b>Trigger</b>	Power loss ➡ Power attach
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG).</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Shutdown the SUT via the brief Power Button press.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Remove power from the SUT via AC-detach, and if necessary also via DC-detach. Wait for <b>10 seconds</b> before continuing to allow full power drain from the SUT.</li> <li>Verify that the SUT is in G3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC where supported; otherwise AC-only. For systems with DC-power support, consult the system design as it may be preferred to connect DC-power before AC-power.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>		
<b>Pass Criteria</b>	<p>Test passes, if all steps are completed successfully for atleast the recommended number of iterations as set by the OEM per the tolerance level of the system design.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>		

## 12.5 PM\_ST\_2 - Remote Power Cycle S0/CM0 (DOS/UEFI)

ID	PM_ST_2		
<b>Title</b>	S0/CM0 to S0/CM0 via Remote Power Cycle (AC+DC, AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		



ID	PM_ST_2		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Remote Power Cycle with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>The SUT should be configured to boot to either DOS (via USB key) or UEFI shell.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0,CM0-PG)
		Final	S0/MeOn (CM0,CM0-PG)
		Trigger	Remote Power Cycle
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG).</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Send a Remote Power Cycle command to the SUT via Intel® AMT by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>If the active network interface is WLAN, wait <b>2 minutes</b> before proceeding.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>If available, set the active network interface to WLAN (from LAN) to run the following :</li> <li>Send a Remote Power Cycle command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>		
Pass Criteria	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>		

## 12.6 PM\_ST\_3 - Remote Reset S0/CM0 (DOS/UEFI)

ID	PM_ST_3		
Title	S0/CM0 to S0/CM0 via Remote Reset (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Remote Reset with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>The SUT should be configured to boot to either DOS (via USB key) or UEFI shell.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.</p>		





ID	PM_ST_3		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0,CM0-PG)
		Final	S0/MeOn (CM0,CM0-PG)
		Trigger	Remote Reset
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC), where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG).</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Send a Remote Reset command to the SUT via Intel® AMT by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>If the active network interface is WLAN, wait <b>2 minutes</b> before proceeding.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li> <li>Send a Remote Reset command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>		
Pass Criteria	<p>Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>		

## 12.7 PM\_ST\_4 - S3/CM3 to S3/CM-Off to S3/CM3 via AC-detach/Attach

ID	PM_ST_4		
Title	S3/CM3 to S3/CM3-PG with AC Wake to S3/CM3 via AC-detach/AC-attach (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Microsoft Windows* InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S3/CM3-PG with AC Wake to S3/CM3 via AC-detach/AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		



ID	PM_ST_4		
Parameters	System Power Source		AC+DC
	Power States	Initial	S3/MeOn (CM3)
		Middle	S3/CM3-PG with Ac Wake
		Final	S3/MeOn (CM3)
		Trigger	AC-detach ➡ AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Verify that the SUT is in S3/CM3-PG with AC Wake.</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>		
Pass Criteria	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



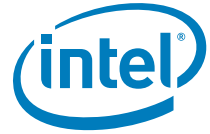
## 12.8 PM\_ST\_5 - S0/CM0 to S3/CM-Off to S0/CM0 via Suspend/Resume

ID	PM_ST_5	
<b>Title</b>	S0/CM0 to S3/CM-Off to S0/CM0 via Host OS suspend/resume (AC+DC,AC-only/PP1/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Microsoft Windows* InstantGo* systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via Host OS suspend/resume with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
<b>Parameters</b>	<b>System Power Source</b>	AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b> S0/MeOn (CM0,CM0-PG)
		<b>Middle</b> S3/MeOff (CM-Off)
		<b>Final</b> S0/MeOn (CM0,CM0-PG)
		<b>Trigger</b> Host OS suspend/resume
	<b>Intel® AMT</b>	<b>Power Package</b> PP1 (Intel® ME on in S0) <b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo-FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>	



## 12.9 PM\_ST\_6 - S0/CM0 to S3/CM3 to S0/CM0 via Suspend/Resume

ID	PM_ST_6	
<b>Title</b>	S0/CM0 to S3/CM3-PG to S0/CM0 via Host OS suspend/resume (AC+DC,AC-only/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Microsoft Windows* InstantGo* systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM3-PG to S0/CM0 via Host OS suspend/resume with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
<b>Parameters</b>	<b>System Power Source</b>   AC+DC or AC-only	
	<b>Power States</b>	<b>Initial</b>   S0/MeOn (CM0,CM0-PG)
		<b>Middle</b>   S3/MeOn (CM3)
		<b>Final</b>   S0/MeOn (CM0,CM0-PG)
		<b>Trigger</b>   Host OS suspend/resume
	<b>Intel® AMT</b>	<b>Power Package</b>   PP2 (Intel® ME on in S0, wake in Sx/AC) <b>WLAN Link Policy</b>   LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>	



## 12.10 PM\_ST\_7 - S0/CM0 to S5/CM3 to S0/CM0 via Power Button Override (DOS/UEFI)

ID	PM_ST_7		
<b>Title</b>	S0/CM0 to S5/CM3 to S0/CM0 via Power Button override cycle (AC+DC, AC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S5/CM3 to S0/CM0 via Power Button override cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. The SUT should be configured to boot to either DOS (via USB key) or UEFI shell. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC or AC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0,CM0-PG)
		<b>Middle</b>	S5/MeOn (CM3)
		<b>Final</b>	S0/MeOn (CM0,CM0-PG)
		<b>Trigger</b>	Power Button override ➡ Power Button press
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC), where available
<b>Setup</b>	1. Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b> . 2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG). 3. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC). 4. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.		
<b>Procedure</b>	1. Shutdown the SUT via a Power Button press for more than <b>5 seconds</b> . 2. Verify that the SUT is in S5/MeOn (CM3). 3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces. 4. Briefly press the Power Button on the SUT. 5. Verify that the SUT is in S0/MeOn (CM0,CM0-PG). 6. Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface. 7. Verify that, after <b>2 minutes</b> , Intel® AMT on the SUT responds to version query via the <b>WLAN</b> network interface, if available.  Repeat this procedure for the remaining number of cycles desired in the stress test.		
<b>Pass Criteria</b>	Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.  Suggested Iterations: Mobile: >=2000, Desktop/AIO/Workstation: >=750		

## 12.11 PM\_ST\_8 - S0/CM0 to S4/CM-Off to S0/CM0 via Hibernate and WoL/WoWLAN

ID	PM_ST_8		
<b>Title</b>	S0/CM0 to S4/CM-Off to S0/CM0 via Host OS hibernate/magic packet cycle (AC+DC, AC-only/PP1/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> System without LAN support
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via Host OS hibernate and magic packet cycle with the parameters outlined below.		



ID	PM_ST_8		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4 and/or Deep S5 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that LAN-only network interfaces are available on the SUT, where network interfaces are available, LAN shall be the initial active network interface in the test.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0,CM0-PG)
		Middle	S4, S5, Deep S4, Deep S5/MeOff (CM-Off)
		Final	S0/MeOn (CM0,CM0-PG)
		Trigger	Host OS hibernate ➡ Magic Packet receipt
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4,S5,Deep S4,Deep S5/MeOff (CM-Off).</li> <li>Send three magic packets, at <b>2 second</b> intervals, by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>LAN</b> network interface.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10   where-Object{\$_.message -like "The boot type*"}</li> <li>Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
Pass Criteria	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>		



## 12.12 PM\_ST\_9 - S0/CM0 to S4/CM3 to S0/CM0 via Hibernate and Remote Power-Up

ID	PM_ST_9	
<b>Title</b>	S0/CM0 to S4/CM3 to S0/CM0 via Host OS hibernate/Remote Power Up cycle (AC+DC,AC-only/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   None
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM3 to S0/CM0 via Host OS hibernate and Remote Power Up cycle with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.	
<b>Parameters</b>	<b>System Power Source</b>   AC+DC or AC-only	
	<b>Power States</b>	<b>Initial</b>   S0/MeOn (CM0,CM0-PG)
		<b>Middle</b>   S4, S5/MeOn (CM3)
		<b>Final</b>   S0/MeOn (CM0,CM0-PG)
		<b>Trigger</b>   Host OS hibernate → Remote Power Up
	<b>Intel® AMT</b>	<b>Power Package</b>   PP2 (Intel® ME on in S0, wake in Sx/AC) <b>WLAN Link Policy</b>   LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4,S5/MeOn (CM3).</li> <li>Send a Remote Power Up command to the SUT via Intel® AMT by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10   where-Object{\$_.message -like "The boot type*"}</li> <li>Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x6<b>8</b>xxxxxx.</li> <li>If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4,S5/MeOn (CM3).</li> <li>Send a Remote Power Up command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x6<b>8</b>xxxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>	

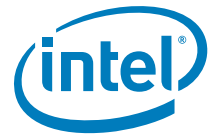


ID	PM_ST_9
Pass Criteria	Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.  Suggested Iterations: Mobile: >=2000, Desktop/AIO/Workstation: >=750

## 12.13 PM\_ST\_10 - S0/CM0 to S5/CM-Off to S0/CM0 via Shutdown and Power Button Press

ID	PM_ST_10		
Title	S0/CM0 to S5/CM-Off to S0/CM0 via Host OS shutdown/Power Button press cycle (AC+DC, AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via Host OS shutdown and Power Button press cycle with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 is supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0,CM0-PG)
		Middle	S4, S5, Deep S4, Deep S5/MeOff (CM-Off)
		Final	S0/MeOn (CM0,CM0-PG)
		Trigger	Host OS shutdown → Power Button press
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Briefly press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Verify that the Host OS on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo-FWSTS")</p>		





ID	PM_ST_10
Pass Criteria	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: <math>\geq 2000</math>, Desktop/AIO/Workstation: <math>\geq 750</math></p>



## 12.14 PM\_ST\_11 - S0/CM0 to S5/CM3 to S0/CM0 via Shutdown and Remote Power-Up

ID	PM_ST_11		
Title	S0/CM0 to S5/CM3 to S0/CM0 via Host OS shutdown/Remote Power Up cycle (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3 to S0/CM0 via Host OS shutdown and Remote Power Up cycle with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.</p>		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0,CM0-PG)
		Middle	S5/MeOn (CM3)
		Final	S0/MeOn (CM0,CM0-PG)
		Trigger	Host OS shutdown → Remote Power Up
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		



ID	PM_ST_11
Procedure	<ol style="list-style-type: none"> <li>1. Shutdown the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S5/MeOn (CM3).</li> <li>3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>4. Send a Remote Power Up command to the SUT via Intel® AMT by means of the active network interface.</li> <li>5. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>6. Verify that the Host OS on the SUT is available.</li> <li>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>8. Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> <li>9. If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li> <li>10. Shutdown the SUT via the Host OS.</li> <li>11. Verify that the SUT is in S5/MeOn (CM3).</li> <li>12. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>13. Send a Remote Power Up command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li> <li>14. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>15. Verify that the Host OS on the SUT is available.</li> <li>16. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>17. Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x68xxxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>
Pass Criteria	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>



## 12.15 PM\_ST\_12 - S3/CM3 to S3/CM-Off to S3/CM3 via Intel® AMT Idle Timeout and Intel® AMT Network Access

ID	PM_ST_12		
Title	S3/CM3 to S3/CM3-PG to S3/CM3 via Intel® AMT idle timeout/Intel® AMT network access (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Microsoft Windows* InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S3/CM3 to S3/CM3-PG to S3/CM3 via AC-detach/AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC
	Power States	Initial	S3/MeOn (CM3)
		Middle	S3/CM3-PG
		Final	S3/MeOn (CM3)
		Trigger	Intel® AMT idle timeout ➔ Intel® AMT network access
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC), where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available.</li> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to MeOff (CM3-PG) after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S3/CM3-PG.</li> <li>Verify that Intel® AMT on the SUT responds to version query by means of the active network interface.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to MeOff (CM3-PG) after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S3/CM3-PG.</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>		



ID	PM_ST_12
Pass Criteria	Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.  Suggested Iterations: Mobile: >=2000, Portable AIO >= 750

## 12.16 PM\_ST\_13 - S0/CM0 to S3/CM3 to S0/CM0 via Suspend and Remote Power-Up

ID	PM_ST_13		
Title	S0/CM0 to S3/CM3 to S0/CM0 via Host OS suspend/Remote Power Up cycle (AC+DC, AC-only/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Microsoft Windows* InstantGo* systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM3 to S0/CM0 via Host OS suspend and Remote Power Up cycle with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0,CM0-PG)
		Middle	S3/MeOn (CM3)
		Final	S0/MeOn (CM0,CM0-PG)
		Trigger	Host OS suspend ➡ Remote Power Up
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		



ID	PM_ST_13
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Suspend the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S3/MeOn (CM3).</li> <li>3. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>4. Send a Remote Power Cycle command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li> <li>5. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>6. Verify that the Host OS on the SUT is available.</li> <li>7. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>8. Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x6<b>8</b>xxxxxx.</li> <li>9. If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li> <li>10. Shutdown the SUT via the Host OS.</li> <li>11. Verify that the SUT is in S3/MeOn (CM3).</li> <li>12. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>13. Send a Remote Power Up command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li> <li>14. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>15. Verify that the Host OS on the SUT is available.</li> <li>16. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>17. Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x6<b>8</b>xxxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>
<b>Pass Criteria</b>	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>

## 12.17 PM\_ST\_14 - S0/CM0 to S3/CM-Off to S0/CM0 via Suspend and Power Button Press

ID	PM_ST_14		
<b>Title</b>	S0/CM0 to S3/CM3-PG with AC Wake to S0/CM0 via Host OS suspend/Power Button press cycle (DC-only/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems <input checked="" type="checkbox"/> Microsoft Windows* InstantGo* systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via Host OS suspend and Power Button press cycle with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		DC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0,CM0-PG)
		<b>Middle</b>	S3/MeOff (CM-Off) with AC Wake
		<b>Final</b>	S0/MeOn (CM0,CM0-PG)
		<b>Trigger</b>	Host OS suspend ➡ Remote Power Up
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available



ID	PM_ST_14
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. Set the SUT power source to AC+DC.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>4. Set the SUT power source to <b>DC-only</b>.</li> <li>5. Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>6. Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>7. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features where available to prevent unexpected host wake events. Most especially, ensure that the Host OS Wireless Wake on LAN driver setting on the SUT is <b>disabled</b>, if the WLAN network interface is available.</li> <li>8. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Suspend the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S3/CM3-PG with AC Wake.</li> <li>3. Briefly press the Power Button on the SUT.</li> <li>4. Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>5. Verify that the Host OS on the SUT is available.</li> <li>6. Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>7. Verify the second nibble of the FWSTS2 register on the SUT have a value of 0x60xxxxxx.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo-FWSTS")</p>
<b>Pass Criteria</b>	<p>Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO: &gt;=750</p>



## 12.18 PM\_ST\_16 - Remote Power Cycle S0/CM0 (DOS/UEFI)

ID	PM_ST_16		
Title	S0/CM0 to S0/CM0 via Remote Power Cycle (AC+DC,AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Remote Reset with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. The SUT should be configured to boot to either DOS (via USB key) or UEFI shell. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
Parameters	System Power Source		AC+DC or AC-only
	Power States	Initial	S0/MeOn (CM0,CM0-PG)
		Final	S0/MeOn (CM0,CM0-PG)
		Trigger	Remote Power Cycle
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"><li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li><li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG).</li><li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li><li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li></ol>		
Procedure	<ol style="list-style-type: none"><li>Send a Remote Power Cycle command to the SUT via Intel® AMT by means of the active network interface.</li><li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>If the active network interface is WLAN, wait <b>2 minutes</b> before proceeding.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li><li>If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li><li>Send a Remote Power Cycle command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li><li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li><li>Wait <b>2 minutes</b> before proceeding.</li><li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li></ol> Repeat this procedure for the remaining number of cycles desired in the stress test.		
Pass Criteria	Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.  Suggested Iterations: Mobile: >=2000, Desktop/AIO/Workstation: >=750		

## 12.19 PM\_ST\_17 - Remote Reset S0/CM0 (DOS/UEFI)

ID	PM_ST_17		
Title	S0/CM0 to S0/CM0 via Remote Reset (AC+DC,AC-only/PP1/LP3)		
Requirement	Mandatory	Exemptions	None
Method	Automated by Intel® PETS		





ID	PM_ST_17	
Objective	This test checks the SUT power flow from S0/CM0 to S0/CM0 via Remote Reset with the parameters outlined below.	
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>The SUT should be configured to boot to either DOS (via USB key) or UEFI shell.</p> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.</p>	
Parameters	System Power Source	
	Power States	Initial
		Final
		Trigger
	Intel® AMT	Power Package
		WLAN Link Policy
Setup	<p>AC+DC or AC-only</p> <p>S0/MeOn (CM0,CM0-PG)</p> <p>S0/MeOn (CM0,CM0-PG)</p> <p>Remote Reset</p> <p>PP1 (Intel® ME on in S0)</p> <p>LP3 (Enabled in S0, Sx/AC) where available</p>	
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG).</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <ol style="list-style-type: none"> <li>Send a Remote Reset command to the SUT via Intel® AMT by means of the active network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>If the active network interface is WLAN, wait <b>2 minutes</b> before proceeding.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li> <li>Send a Remote Reset command to the SUT via Intel® AMT by means of the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S0/MeOn (CM0,CM0-PG).</li> <li>Wait <b>2 minutes</b> before proceeding.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>	
Pass Criteria	<p>Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Desktop/AIO/Workstation: &gt;=750</p>	



## 12.20 PM\_ST\_18 - S5/CM3 to S5/CM-Off to S5/CM3 via AC-detach/Attach

ID	PM_ST_18		
Title	S5/CM3 to S5/CM3-PG with AC Wake to S5/CM3 via AC-detach/AC-attach (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S5/CM3 to S5/CM-Off to S5/CM3 via AC-detach/AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 is supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		AC+DC
	Power States	Initial	S5/MeOn (CM3)
		Middle	S5, Deep S5/CM3-PG with AC Wake
		Final	S5/MeOn (CM3)
		Trigger	AC-detach → AC-attach
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Verify that the SUT is in S4,S5/MeOff (CM3-PG).with AC Wake.</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>		
Pass Criteria	<p>Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.21 PM\_ST\_19 - S5/CM3 to S5/CM-Off to S5/CM3 via Intel® AMT Idle Timeout and Intel® AMT Network Access

ID	PM_ST_19		
<b>Title</b>	S5/CM3 to S5/CM3-PG to S5/CM3 via Intel® AMT idle timeout/Intel® AMT network access (AC+DC/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	None
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S5/CM3 to S5/CM3-PG to S5/CM3 via AC-detach/AC-attach with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT. Where both network interfaces are available, LAN shall be the initial active network interface in the test, and WLAN shall be the secondary network interface.		
<b>Parameters</b>	<b>System Power Source</b>		AC+DC
	<b>Power States</b>	<b>Initial</b>	S5/MeOn (CM3)
		<b>Middle</b>	S5/MeOff (CM3-PG)
		<b>Final</b>	S5/MeOn (CM3)
		<b>Trigger</b>	Intel® AMT idle timeout ➔ Intel® AMT network access
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b> where supported; otherwise <b>AC-only</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure the Intel® AMT idle timeout on the SUT is set to <b>1 minute</b>.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to MeOff (CM3-PG) after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S5/MeOff (CM3-PG).</li> <li>Verify that Intel® AMT on the SUT responds to version query by means of the active network interface.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>If available, set the active network interface to <b>WLAN</b> (from LAN) to run the following:</li> <li>Wait for <b>3 minutes</b> to allow the Intel® ME on the SUT to move to MeOff (CM3-PG) after Intel® AMT idle timeout.</li> <li>Verify that the SUT is in S5/MeOff (CM3-PG).</li> <li>Verify that Intel® AMT on the SUT responds to version query via the <b>WLAN</b> network interface.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p>		
<b>Pass Criteria</b>	<p>Test passes, if all steps are completed successfully for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.22 PM\_ST\_20 - S0/CM0 to S3/CM3 to S0/CM0 via AC Attach

ID	PM_ST_20		
Title	S0/CM0 to S3/CM3 to S0/CM0 via AC-attach (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM3 to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Middle	S3/MeOn (CM3)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S3 state
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
Pass Criteria	<p>Test passes, if Intel (R) CSME functions Properly when AC Source attached in S3 State with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.23 PM\_ST\_21 - S0/CM0 to S4/CM3 to S0/CM0 via AC-Attach

ID	PM_ST_21	
<b>Title</b>	S0/CM0 to S4/CM3 to S0/CM0 via AC-attach (AC+DC/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM3 to S0/CM0 via AC-attach with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4 and/or Deep S5 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	
	<b>Power States</b>	DC-only
		S0/MeOn (CM0)
		S4/MeOn (CM3)
		S0/MeOn (CM0)
		AC-attach in S4 state
	<b>Intel® AMT</b>	<b>Power Package</b> PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S4/M3 (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10   where-Object{\$_.message -like "The boot type*"}</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if Intel (R) CSME functions Properly, when AC Source attached in S4 State with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>	



## 12.24 PM\_ST\_22 - S0/CM0 to S5/CM3 to S0/CM0 via AC Attach

ID	PM_ST_22		
Title	S0/CM0 to S5/CM3 to S0/CM0 via AC-attach (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM3 to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 is supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Middle	S5/MeOn (CM3)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S5 state
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
Pass Criteria	<p>Test passes, if Intel (R) CSME functions Properly when AC Source attached in S5 State with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.25 PM\_ST\_23 - S0/CM0 to S3/CM-Off to S0/CM0 via AC Attach

ID	PM_ST_23	
<b>Title</b>	S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach (AC+DC/PP1/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.	
<b>Parameters</b>	<b>System Power Source</b>	
	<b>Power States</b>	DC-only
		Initial
		Middle
		Final
	<b>Intel® AMT</b>	Trigger
		Power Package
		WLAN Link Policy
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if Intel (R) CSME functions properly with no flash logs found i.e. stays MOFF, when AC Source attached in S3 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>	



## 12.26 PM\_ST\_24 - S0/CM0 to S4/CM-Off to S0/CM0 via AC Attach

ID	PM_ST_24		
Title	S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach (AC+DC/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4 and/or Deep S5 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Middle	S4/MeOff (CM-Off)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S4 state
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10   where-Object{\$_.message -like "The boot type*"}</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
Pass Criteria	<p>Test passes, if Intel (R) CSME functions properly with no flash logs found.i.e. stays MeOff, when AC Source attached in S4 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		





## 12.27 PM\_ST\_25 - S0/CM0 to S5/CM-Off to S0/CM0 via AC Attach

ID	PM_ST_25	
<b>Title</b>	S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach (AC+DC/PP1/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 is supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	
	<b>Power States</b>	DC-only
		S0/MeOn (CM0)
		S5/MeOff (CM-Off)
		S0/MeOn (CM0)
		AC-attach in S5 state
	<b>Intel® AMT</b>	<b>Power Package</b> PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if Intel® CSME functions properly with no flash logs found i.e. stays MOff, when AC Source attached in S5 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>	



## 12.28 PM\_ST\_26 - S0/CM0 to S3/CM-Off to S0/CM0 via AC Attach

ID	PM_ST_26		
Title	S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach (AC+DC)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems Instant-go Platforms
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	Intel® AMT should not be provisioned i.e. users will have to manually un-provision Intel (R) AMT if it is provisioned. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Middle	S3/MeOff (CM-Off)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S3 state
	Intel® AMT	Power Package	[Intel (R) AMT Not Provisioned]
		WLAN Link Policy	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure Intel (R) AMT is <b>not Provisioned</b></li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo-FWSTS")</p>		
Pass Criteria	<p>Test passes, if Intel (R) CSME functions Properly with no flash logs found i.e. stays MOFF when AC Source attached in S3 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.29 PM\_ST\_27 - S0/CM0 to S4/CM-Off to S0/CM0 via AC Attach

ID	PM_ST_27	
<b>Title</b>	S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach (AC+DC)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should not be provisioned. i.e. users will have to manually un-provision Intel® AMT, if it is provisioned.</p> <p>If Deep S4 and/or Deep S5 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>• If Deep S4 and/or Deep S5 are supported on the SUT, confirm the following:</li> <li>• The SUT and/or BIOS are properly configured to permit Deep S4/S5 entry.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	
	<b>Power States</b>	DC-only
		<b>Initial</b> S0/MeOn (CM0)
		<b>Middle</b> S4/MeOff (CM-Off)
		<b>Final</b> S0/MeOn (CM0)
		<b>Trigger</b> AC-attach in S4 state
	<b>Intel® AMT</b>	<b>Power Package</b> [Intel® AMT Not Provisioned]
		<b>WLAN Link Policy</b>
<b>Setup</b>	<ol style="list-style-type: none"> <li>1. Set the SUT power source to <b>AC+DC</b>.</li> <li>2. Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>3. Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>4. Set the SUT power source to <b>DC-only</b>.</li> <li>5. Ensure Intel® AMT is <b>not Provisioned</b></li> <li>6. Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Hibernate the SUT via the Host OS.</li> <li>2. Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>3. Set the SUT Power Source to AC+DC.</li> <li>4. Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>5. Briefly Press the Power Button on the SUT.</li> <li>6. Verify that the SUT is in S0/MeOn (CM0).</li> <li>7. Verify that the Host on the SUT is available.</li> <li>8. Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10   where-Object{\$_.message -like "The boot type*"}</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if Intel® CSME functions Properly with no flash logs found i.e. stays MOff, when AC Source attached in S4 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>	



## 12.30 PM\_ST\_28 - S0/CM0 to S5/CM-Off to S0/CM0 via AC Attach

ID	PM_ST_28		
Title	S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach (AC+DC)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-attach with the parameters outlined below.		
Configuration	<p>Intel® AMT should not be provisioned. i.e. users will have to manually un-provision Intel® AMT if it is provisioned.</p> <p>If Deep S5 is supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>If Deep S5 is supported on the SUT, confirm the following: <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> </ul> </li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Middle	S5/MeOff (CM-Off)
		Final	S0/MeOn (CM0)
		Trigger	AC-attach in S5 state
	Intel® AMT	Power Package	[Intel (R) AMT Not Provisioned]
		WLAN Link Policy	
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT power source to <b>DC-only</b>.</li> <li>Ensure Intel (R) AMT is <b>not Provisioned</b></li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Set the SUT Power Source to AC+DC.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
Pass Criteria	<p>Test passes, if Intel (R) CSME functions Properly with no flash logs found i.e. stays MOFF, when AC Source attached in S5 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.31 PM\_ST\_29 - S0/CM0 to S3/CM-Off to S0/CM0 via AC Detach

ID	PM_ST_29		
<b>Title</b>	S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach (AC+DC/PP2/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems Instant Go Platforms
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		DC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0)
		<b>Middle</b>	S3/MeOff (CM-Off)
		<b>Final</b>	S0/MeOn (CM0)
		<b>Trigger</b>	AC-detach in S3 state
	<b>Intel® AMT</b>	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT Power Source to <b>DC Only</b>.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
<b>Pass Criteria</b>	<p>Test passes, if Intel® CSME functions Properly with no flash logs found i.e. become MOff, when AC Source detached in S3 State and becomes MeOn after AC Attached in S3 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.32 PM\_ST\_30 - S0/CM0 to S4/CM-Off to S0/CM0 via AC Detach

ID	PM_ST_30		
Title	S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach (AC+DC/PP2/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4 and/or Deep S5 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Middle	S4/MeOff (CM-Off)
		Final	S0/MeOn (CM0)
		Trigger	AC-detach in S4 state
	Intel® AMT	Power Package	PP2 (Intel® ME on in S0, wake in Sx/AC)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/M3 (CM3).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to at least 90% for long run testing.</li> <li>Set the SUT Power Source to <b>DC Only</b>.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S4/M3 (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10   where-Object{\$_.message -like "The boot type*"}</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
Pass Criteria	<p>Test passes, if Intel (R) CSME functions Properly with no flash logs found i.e. become MOff, when AC Source detached in S4 State and becomes MeOn after AC Attached in S4 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		



## 12.33 PM\_ST\_31 - S0/CM0 to S5/CM-Off to S0/CM0 via AC Detach

ID	PM_ST_31	
<b>Title</b>	S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach (AC+DC/PP2/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 is supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	
	<b>Power States</b>	DC-only
		S0/MeOn (CM0)
		S5, Deep S5/MeOff (CM-Off)
		S0/MeOn (CM0)
		AC-detach in S5 state
	<b>Intel® AMT</b>	
	<b>Power Package</b>	PP2 (Intel® ME on in S0, wake in Sx/AC)
	<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 2</b> (Intel® ME on in S0, wake in Sx/AC).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT Power Source to <b>DC Only</b>.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S5/MeOn (CM3).</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo-FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if Intel® CSME functions Properly with no flash logs found i.e. become MOff, when AC Source detached in S5 State and becomes MeOn after AC Attached in S5 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>	



## 12.34 PM\_ST\_32 - S0/CM0 to S3/CM-Off to S0/CM0 via AC Detach

ID	PM_ST_32		
<b>Title</b>	S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach (AC+DC/PP1/LP3)		
<b>Requirement</b>	Mandatory	<b>Exemptions</b>	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS		
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S3/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.		
<b>Configuration</b>	Intel® AMT should be provisioned via manual mode. This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.		
<b>Parameters</b>	<b>System Power Source</b>		DC-only
	<b>Power States</b>	<b>Initial</b>	S0/MeOn (CM0)
		<b>Middle</b>	S3/MeOff (CM-Off)
		<b>Final</b>	S0/MeOn (CM0)
		<b>Trigger</b>	AC-detach in S3 state
	<b>Intel® AMT</b>	<b>Power Package</b>	PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b>	LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> <li>Record the Host OS last boot time on the SUT (to verify successful return from S3).</li> </ol>		
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Suspend the SUT via the Host OS.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT Power Source to <b>DC Only</b></li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S3/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify the Host OS last boot time on the SUT matches the boot time recorded before entry into S3.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
<b>Pass Criteria</b>	<p>Test passes, if Intel® CSME functions Properly become Me-Off, when AC Source detached in S3 State and becomes MeOn after AC Attached in S3 State with no flash logs found.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		





## 12.35 PM\_ST\_33 - S0/CM0 to S4/CM-Off to S0/CM0 via AC Detach

ID	PM_ST_33	
<b>Title</b>	S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach (AC+DC/PP1/LP3)	
<b>Requirement</b>	Mandatory	<b>Exemptions</b>   <input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
<b>Method</b>	Automated by Intel® PETS	
<b>Objective</b>	This test checks the SUT power flow from S0/CM0 to S4/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.	
<b>Configuration</b>	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S4 and/or Deep S5 are supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S4/S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>	
<b>Parameters</b>	<b>System Power Source</b>	
	<b>Power States</b>	DC-only
		S0/MeOn (CM0)
		S4/MeOff (CM-Off)
		S0/MeOn (CM0)
		AC-detach in S3 state
	<b>Intel® AMT</b>	<b>Power Package</b> PP1 (Intel® ME on in S0)
		<b>WLAN Link Policy</b> LP3 (Enabled in S0, Sx/AC) where available
<b>Setup</b>	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>	
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Hibernate the SUT via the Host OS.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT Power Source to DC Only.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S4/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that windows booted from hibernate i.e. value should be 0x02. "Run the following power shell command" Get-WinEvent-ProviderName Microsoft-Windows-Kernel-boot-MaxEvents 10   where-Object{\$_.message -like "The boot type*"}</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>	
<b>Pass Criteria</b>	<p>Test passes, if Intel® CSME functions Properly with no flash logs found i.e. become Me-Off, when AC Source detached in S4 State and becomes MeOn after AC Attached in S4 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>	



## 12.36 PM\_ST\_34 - S0/CM0 to S5/CM-Off to S0/CM0 via AC Detach

ID	PM_ST_34		
Title	S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach (AC+DC/PP1/LP3)		
Requirement	Mandatory	Exemptions	<input checked="" type="checkbox"/> Non-Mobile (AC-only) systems
Method	Automated by Intel® PETS		
Objective	This test checks the SUT power flow from S0/CM0 to S5/CM-Off to S0/CM0 via AC-detach with the parameters outlined below.		
Configuration	<p>Intel® AMT should be provisioned via manual mode.</p> <p>If Deep S5 is supported on the SUT, confirm the following:</p> <ul style="list-style-type: none"> <li>The SUT and/or BIOS are properly configured to permit Deep S5 entry.</li> <li>The correct Deep Sx policy is applied to the SUT profile in Intel® PETS.</li> </ul> <p>This test assumes that either LAN-only, WLAN-only, or both LAN and WLAN network interfaces are available on the SUT.</p>		
Parameters	System Power Source		DC-only
	Power States	Initial	S0/MeOn (CM0)
		Middle	S5, Deep S5/MeOff (CM-Off)
		Final	S0/MeOn (CM0)
		Trigger	AC-detach in S5 state
	Intel® AMT	Power Package	PP1 (Intel® ME on in S0)
		WLAN Link Policy	LP3 (Enabled in S0, Sx/AC) where available
Setup	<ol style="list-style-type: none"> <li>Set the SUT power source to <b>AC+DC</b>.</li> <li>Bring the SUT to the base state of S0/MeOn (CM0,CM0-PG), and confirm that the Host OS is available.</li> <li>Set the active power package on the SUT to <b>Power Package 1</b> (Intel® ME in S0).</li> <li>Set the Intel® AMT WLAN link policy on the SUT to <b>Link Policy 3</b> (Enabled in S0, Sx/AC), if the WLAN network interface is available.</li> <li>Ensure that the Host OS network device drivers are configured to <b>not wake</b> the SUT. This includes <b>enabling</b> ARP and/or NS Offload features, where available to prevent unexpected host wake events.</li> </ol>		
Procedure	<ol style="list-style-type: none"> <li>Shutdown the SUT via the Host OS.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Verify that a DC battery is connected to the SUT, and that it is charged to atleast 90% for long run testing.</li> <li>Set the SUT Power Source to DC Only.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Set the SUT power source to AC+DC.</li> <li>Verify that the SUT is in S5,Deep S5/MeOff (CM-Off).</li> <li>Briefly Press the Power Button on the SUT.</li> <li>Verify that the SUT is in S0/MeOn (CM0).</li> <li>Verify that the Host on the SUT is available.</li> <li>Verify that Intel® AMT on the SUT responds to version queries via <b>all</b> available network interfaces.</li> </ol> <p>Repeat this procedure for the remaining number of cycles desired in the stress test.</p> <p>Check if there are any flash log. Success if there is no flash log.(Can test flash log by "MEInfo -FWSTS")</p>		
Pass Criteria	<p>Test passes, if Intel® CSME functions Properly with no flash logs found i.e. become Me-Off, when AC Source detached in S5 State and becomes MeOn after AC Attached in S5 State.</p> <p>Suggested Iterations: Mobile: &gt;=2000, Portable AIO &gt;= 750</p>		





# 13 Intel® Trusted Execution Technology (Intel® TXT)

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## 13.1 Introduction

This chapter describes a validation strategy for Intel® Trusted Execution Technology (Intel® TXT) on the Client platforms.

Intel Trusted Execution Technology is part of Intel's Safer Computing Initiative. Intel® TXT provides a security foundation to build protections against software based attacks. For the Client platforms, Intel® TXT provides the capabilities to create a measured launched environment (MLE) and have that MLE verified against a good known environment. For more information, refer to the *Intel® TXT Measured Launched Environment Developer's Guide* in <http://www.intel.com/content/www/us/en/software-developers/intel-txt-software-development-guide.html>.

This chapter is intended for validation purposes. The objective is to provide validation professionals with additional insight into Intel® TXT by highlighting key validation considerations in a bottom-up approach.

This chapter is not a technology overview and does not supplant the existing Intel® TXT collaterals. The readers are expected to be familiar with Intel® TXT and to use this document as a validation supplement to develop their own validation plan.

### 13.1.1 Validation Flow

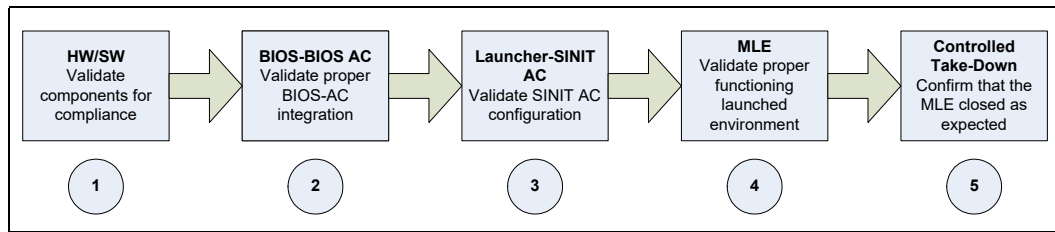
At the processor and chipset level, Intel Corporation applies rigorous validation to ensure these components perform to specification. Feature focused and random test suites are executed on individual components and in comparable pairing to make sure adequate validation coverage is achieved at both component and platform levels.

The infrastructure that is required to validate the processor and chipset at this silicon level requires extensive development. Due to the effort and the complexity, this low level validation of Intel® TXT is outside the scope of this validation guide. Only the portion of the flow that is applicable by platform suppliers (OEM/ODM) is described.

To validate Intel® TXT on client platforms, consider the sequence of events that make up an Intel® TXT verified launch (TXT-VL). This is because TXT-VL effectively utilizes the key hardware and software components that define the Intel® TXT feature.

Figure 13-1 diagrams the key components that make up a TXT-VL. The starting point is the Intel® TXT enabled hardware and software components. Second is proper integration of a BIOS AC module into the system BIOS. Third is correct configuration of the system, by the environment launcher to run the SINIT AC module. Fourth is the measured launch environment (MLE) operation. The last stage is a controlled take-down of the MLE.

**Figure 13-1. Intel® TXT Verified Launch/Validation Flow**



**NOTE:** Intel® TXT VL varies depending on the MLE start-up process, however the steps described above are consistent across MLE launching mechanism.

This document uses the Intel® TXT VL flow as the framework for this bottom-up strategy. The following sections highlight the validation considerations for each step in the flow.

## 13.2 Prerequisite

Before proceeding with the checkout process described in this document, there are a few conditions and preparations that should be done to make the checkout most productive.

### 13.2.1 TPM 1.2 NV Indices Defined and Locked

**Note:** **The AUX and PS indices creation should not be done as part of the validation process.** Absence of these indices on the SUT indicates that the index creation process either in manufacturing or other processes defined by the platform supplier is not functional.

Make sure the AUX and PS indices are defined, as described in “Intel Initiatives Trusted Platform Module (TPM) NV Storage Interface Usage” document. These indices are critical components of the Intel® TXT infrastructure. How and when these indices are defined is up to of the platform supplier. The Intel® TXT requires that the AUX and PS indices are defined in the NV space and that the NV space is enabled and the indices locked before Intel® TXT is used. Refer to the *Intel Initiatives TPM NV Storage Interface Usage* document for information on this requirement.

For the **BIOS development environment**, Intel Corporation provides the TPM provision reference tool as part of the ACM package (refer to Bin directory of the ACM). These scripts that can be used to provision the TPM as required for TXT. Refer to [Appendix A.1](#).

### 13.2.2 TPM 2.0 Indices Defined, Locking, and Hierarchies

Unlike TPM 1.2, where the OEM had to create TPM objects (Example: AUX and PS Policy NVRAM Indexes) and then lock the TPM preventing anyone from deleting or modifying their definitions, TPM 2.0 defines 3 hierarchies that are independent of each other. These are the Platform Hierarchy, Storage Hierarchy, and Endorsement Hierarchy. The Platform Hierarchy is dedicated for the platform vendor, while the Storage Hierarchy and Endorsement Hierarchy are dedicated for the platform owner. This document only deals with the Platform Hierarchy (PH). Each hierarchy has its own



authorization value (AuthValue) and authorization policy (authPolicy). More on authorization policies later, but authPolicy is an alternative way to demonstrate authorization to use the PH.

This means that there is no longer the notion of a LOCKED TPM and the OEM are now able to add, delete, and provision its TPM objects at any time.

However, **PS index should be locked for TPM 2.0 using PS2 attributes and Production ACMs**. PS2 definition is the preferred choice for OEM/ODM.

Unlike the other hierarchies, which have persistent authorization values, the PH authValue and authPolicy are cleared each time the platform resets. It is the BIOS responsibility to establish the PH authValue (and optionally the PH authPolicy) on each platform reset.

The notion is that BIOS sets PH authValue to a random value, use that value, if it needs to perform any operations that require PH authorization and then flush that value from memory (or store it in a protected location) before any executing any untrusted code (option ROMs, boot code, and so forth.).

**If the customer platform BIOS chooses to use a random value for platformAuth value, the TPM 2.0 provisioning tool must be modified to match Platform Policy Digest. OR the customer can choose to make a special BIOS mode where platformAuth.**

For the BIOS development environment, Intel Corporation provides the TPM provision reference tool as part of the ACM package (refer to Bin directory of the ACM). These scripts that can be used to provision the TPM as required for TXT. Refer to [Appendix A.1](#).

### 13.2.3 BIOS Setting

Intel® TXT is dependent on Intel® VT, Intel® VT-d a discrete TPM and requires all Processors and Cores to be enabled. Steps to enable Intel® TXT in system BIOS:

1. Intel® VT => Enabled
2. Intel® VT-d => Enabled
3. Trusted Platform Module => Enabled
4. If Platform supports dTPM and PTT then follow steps 6 and 7.
5. PCH-FW Configuration => TPM Device Selection => dTPM (Discrete TPM)
6. TPM Configuration => Current TPM Selected Device => 1.2 or 2.0 => Enabled

*(Ensure TPM is correctly provisioned before enabling TXT)*

7. Intel® TXT => Enabled

### 13.2.4 Unblocking Mechanism

A key feature for Intel® TXT on client platforms is *secret protection*. Secret protection relies on the BIOS properly invoking the BIOS AC – SCLEAN. Improperly implemented BIOS can leave the system in a blocked state.



Until BIOS implementation has been thoroughly evaluated, it is beneficial to have a mechanism to unblock the system. The system can be unblocked using a BIOS debugger, such as XDP/ITP or using a BIOS version that unconditionally invoke SCLEAN.

Additional method that may work to unblock a system is to replace the TPM. An unblocking mechanism should be defined before executing the secret protection checkout described in this document.

### 13.2.5 SINIT ACM

The SINIT ACM is a critical component of the Intel® TXT architecture. Intel® TXT requires this software component for the verified launch feature. Verify that user have the compatible SINIT ACM for the platform being tested. This module is required for the measured launch test cases. Invoking measured launch (SENDER) with an incompatible SINIT ACM results in an Intel® TXT reset.

TXINFO64.efi can be used to determine SINIT ACM compatibility:

```
EFI> txtinfo64 -a <ACM-filename>
```

Reminder, SINIT ACMs that have the suffix \_debug.bin are only compatible with ES hardware. SINIT ACMs that have suffix \_production/\_release.bin are signed for QS hardware.

Refer to DCL to determine the requirement.

## 13.3 Hardware and Software Components

### 13.3.1 Check Component Compliance

First validation step is to determine, if the Intel® TXT hardware and software components are enabled and are compatible.

**The hardware checks include:**

1. Validate that the processor supports SMX and VMX.
2. Verify that the chipset is Intel® TXT capable.
3. Confirm that processor and chipset are compatible.
  - a. Use an engineering sample (ES) CPU with an ES chipset, or a production sample (QS) CPU with a QS chipset.
4. Confirm that the TPM is TCG 1.2 or TPM 2.0 is TCG 2.0 compliant to the extent required by Intel® TXT.
5. TPM should be provisioned using the corresponding scripts released with the ACM package.

**For software checks:**

1. Verify the chipset compatible BIOS ACM is being used.
2. Verify the chipset compatible SINIT ACM is being used.



3. TPM NV INDEX\_AUX and INDEX\_PS are created and locked (required for production) in the TPM NV space.
4. BIOS ACM and SINIT ACM types have to match i.e. Debug with Debug, NPW with NPW, and Production with Production, respectively.

**The table below summarizes the allowed combination of hardware and software components (Refer TXT ACM packages for TPM Provisioning tools and instructions):**

CPU	PCH	BIOS ACM	TPM Provisioning Type	TPM Lock Required	SINIT ACM	Platform Milestone
ES	ES	Debug (Pre Production)	Pre-Production	No	Debug (Pre Production)	Pre Alpha, Alpha, Beta
QS	QS	Non Production Worthy (NPW)	Production	No	Non Production Worthy (NPW)	Production Candidate (PC)
QS	QS	Production	Production	Yes	Production	Production Version (PV)

#### 13.3.1.1 Processor

TXTINFO64.efi or the CPUID instruction can be used to determine, if the processor is Intel® TXT capable (i.e., supports SMX and VMX).

For more information on CPUID, refer Chapter 3, "Instruction Set Reference, A-M," in the *Intel® 64 and IA-32 Software Developer Manual, Volume 2A*.

#### 13.3.1.2 Chipset

TXTINFO64.efi or the SMX GETSEC[CAPABILITIES] instruction can be used to determine, if the chipset supports Intel® TXT.

For more information on the GETSEC[CAPABILITIES], refer Section 6.2.2.1, "Getsec(Capabilities)" in the *Intel® 64 and IA-32 Software Developer Manual, Volume 2B*.

#### 13.3.1.3 AC Modules

To determine AC module compatibility, check the *Vendor ID* and *Module ID* fields in the AC module header. Make sure they match the chipset *Vendor ID* and *Device ID* of the platform. TXTINFO64.efi also reports the BIOS ACM compatibility. To determine SINIT ACM compatibility, refer to [Section 13.2.5, "SINIT ACM."](#)

For more information on AC Module Identification, refer to the *Intel® Trusted Execution Technology BIOS Specification*.

#### 13.3.1.4 Intel® TXT and Boot Guard Compatibility

Only Production Boot Guard Profiles (0/4/5) are supported for use with TXT. Boot Guard Profile is configured in the FIT during SPI image creation.



### 13.3.1.5 Intel® TXT and Software Guard Extensions (SGX) Compatibility

If both Intel® TXT and Software Guard Extensions (SGX) are intended to be used on the same platform, a SGX index is needed for BIOS to keep track of SINIT security version number (SVN), when SINIT ACM is not part of the BIOS code\*. This can be done by running 'Define\_SGX.nsh' script concurrently with TXT TPM provisioning scripts that can be located in the ACM package posted on VIP.

**Note:** Use the TPM provisioning scripts from the ACM package corresponding to the platform as the TXT TPM provisioning scripts are unique for each platform generation. TPM provisioning via scripts or BIOS needs to happen prior running SGX application.

Refer to Intel® Software Guard Extensions (Intel® SGX) Technology Overview and BIOS Support Summary for more information on SGX.

BIOS Based TPM Provisioning (# 550711) provides detail on how to provision the TPM through BIOS.

**Note:** This collateral is guidance, not a reference tool.

## 13.4 Tools

### 13.4.1 Validation Tools

The method described in this document uses the following development tools provided by Intel Corporation. Tools are provided as Intel® TXT Client Debug Toolkit, which contains 64-bit tools. Make sure user have access to these tools prior to checkout. The reader is advised to review the tool release notes for actual syntax.

**getsec64.efi** can be used to confirm that the systems' hardware and software components can support a measured/verified launch.

**txtinfo64.efi** is a tool that can be used to investigate common status of TXT capable platform. This tool is also available as part of the *Intel® TXT BIOS Development Kit*.

**secrets64.efi** a tool that can be used to set the secret flag in the Intel® TXT MLE. This tool is also available as part of the *Intel® TXT BIOS Development Kit*.

**DUET** boot disk or the UEFI **BIOS EFI-shell**. This shell environment is necessary since the core TXT tools are EFI shell based. Refer to [Section 13.12.1](#) for tool location.

**MLE** – A MLE such as Trusted Boot (**tboot**) LiveImage, which can be used to confirm that BIOS has properly configured Intel® TXT to launch the measured environment. Refer to [Section 13.12.1](#) for tool location.

**Trace Enabled ACMs** - Under certain debug scenarios it is important to use specially designed trace enabled BIOS ACM or SINIT ACM to capture the internal state of ACM execution during an erroneous condition. These engineering trace enabled ACMs are only provided for special debug purpose on case by case basis.

**Note:** ACM serial out debug message requires BIOS to explicitly use **0x3F8** port for capturing the serial log.





### 13.4.1.1 TXTINFO64 Log

For the EFI-shell environment, Intel provides the *txtinfo64.efi* tool. Execute *txtinfo64.efi* in an EFI-shell as follow:

```
EFI> txtinfo64 -c:a
*****
TXTINFO64 v1.5.18
Intel Corporation
Copyright (c) 2010-2017
*****
Collecting Chipset information...Done.
Collecting CPU...Done.
Collecting TXT Registers...Done.
Collecting ACM...Done.
Collecting VTd...Done.
Collecting Heap...Done.
Collecting TPM...Done.
Testing CPU...Done.
Testing TXT Reg...Done.
Testing Heap...Done.
Testing TPM...Done.
Testing VTd...Done.
-----
SUCCESS: TXT is enabled in the BIOS and platform appears ready for TXT.
```

```
*****
* CPU Information *
*****
CPU 00 -- ILP
-----
APIC ID = 0x0
CUID = 0x406E2
IA32_BIOS_SIGN_ID = 0xF
CUID.1.ECX[6] (SMX) = 1
CUID.1.ECX[5] (VMX) = 1
CUID.7.EBX[2] (SGX) = 1
IA32_MTRRCAP[11] (SMRR) = 1
IA32_PLATFORM_ID[52:50] = 0x7
TXT_CTRL_STS MSR[0] = 1

IA32_FEATURE_CONTROL 3Ah:
[15] SGX Enable = 0
[15] SENTER Global Enable = 1
[14:8] SENTER Local Function Enable = 0x7F
[3] SMRR Enable = 0
[2] Enable VMX outside SMX = 1
[1] Enable VMX inside SMX = 1
[0] Lock = 1

GETSEC[CAPABILITIES] = 0x1FD
Intel(R) TXT-capable chipset is present = 1
```

Confirm **all the processors** detected on the platform are capable and enabled for Intel® TXT. Key checks:

- SMX/VMX supported
- MSR must have SENTER enabled
- All getsec capabilities must be available



```
ENTERACCS is available          = 1
EXITAC is available             = 1
SENDER is available            = 1
SEXIT is available             = 1
PARAMETERS is available        = 1
SMCTRL is available            = 1
WAKEUP is available            = 1

CPU[01]...
CPU[02]...
CPU[03]...
-----
APIC ID                         = 0x3
CUID                            = 0x406E2
IA32_BIOS_SIGN_ID              = 0xF
CUID.1.ECX[6] (SMX)            = 1
CUID.1.ECX[5] (VMX)            = 1
CUID.7.EBX[2] (SGX)            = 1
IA32_MTRRCAP[11] (SMRR)        = 1
IA32_PLATFORM_ID[52:50]        = 0x7
TXT_CTRL_STS MSR[0]            = 1

IA32_FEATURE_CONTROL 3Ah:
[15] SGX Enable                = 0
[15] SENTER Global Enable      = 1
[14:8] SENTER Local Function Enable = 0x7F
[3] SMRR Enable                = 0
[2] Enable VMX outside SMX     = 1
[1] Enable VMX inside SMX      = 1
[0] Lock                       = 1

GETSEC[CAPABILITIES]           = 0x1FD
Intel(R) TXT-capable chipset is present = 1
ENTERACCS is available          = 1
EXITAC is available             = 1
SENDER is available            = 1
SEXIT is available             = 1
PARAMETERS is available        = 1
SMCTRL is available            = 1
WAKEUP is available            = 1
```

```
*****
*           Chipset Information           *
*****
MCH DID          = 0x190C
MCH RID          = 0x3
PCH DID          = 0x9D46
PCH RID          = 0x10
TXT Enable       = 1
MCHBAR + 0x50FC  = 0x8F
```

Chipset  
must also  
be Intel®  
TXT  
enabled



```

B0:D0:F0:0x5C          = 0xAC000047
B0:D0:F0:0xB8          = 0xAC000001
B0:D22:F0:0x6C         = 0x0

```

```

*****
*                      TXT Registers                      *
*****

```

```

TXT.STS
[16] LOCALITY2-OPEN.STS      = 0
[15] LOCALITY1-OPEN.STS      = 0
[14] LOCALITY3-OPEN.STS      = 0
[11] MEM-CONFIG-OK.STS       = 0
[7]  PRIVATE-OPEN.STS        = 0
[6]  MEM-CONFIG-LOCK.STS     = 0
[5]  BASE.LOCKED.STS         = 0
[4]  MEM.UNLOCK.STS          = 1
[1]  SEXIT.DONE.STS          = 1
[0]  SENTER.DONE.STS         = 0

```

```

TXT.ESTS
[6]  WAKE-ERROR.STS          = 0
[1]  ROGUE.STS               = 0
[0]  TXT_RESET.STS           = 0

```

```

TXT.ERRORCODE              = 0x0
[31]   Valid/Invalid        = 1
[30]   Processor/External    = 1
[14:10] ACM Error Code      = 0x0
[9:4]  ACM Progress Code     = 0x0 SINIT Exit Point
[3:0]  AC Module Type        = 0x1 SINIT
TXT.VER.EMIF[31]           = 0

```

```

TXT.DIDVID                  = 0xB0068086
TXT.SINIT.BASE               = 0xABED0000
TXT.SINIT.SIZE               = 0x00050000
TXT.HEAP.BASE                = 0xABF20000
TXT.HEAP.SIZE                = 0x000E0000
TXT.DPR                      = 0xAC000041
TXT.PUBLIC KEY:

```

```

12 CD 5D 03 4E 12 56 50 F1 CC 35 92 23 2E 8E A3
B7 F9 DE 4C 42 4D 5F AF BA 02 D9 CD FD 48 80 B1

```

```

*****
*                      Heap Structures                      *
*****

```

```

BIOS Data
-----

```

```

Size                        = 0x56
Version                     = 0x6
BiosSinitSize               = 0x0
LcpPdBase                   = 0x0

```

Confirm these registers are programmed according to the Intel® TXT BIOS Specification

If TXTINFO is invoked within an Intel® TXT measured environment, this area will display important heap information setup by the Intel® TXT MLE

Verify the LCP Version is as required by the SINIT ACM



```
LcpPdSize = 0x0
NumberOfLogicalProcessors = 0x4
SinitFlags = 0x0
MleFlags = 0x2
[0] TXT/VT-x/VT-d ACPI PPI specification = 0
ExtDataElements:
  HEAP_EXT_DATA_ELEMENT.Type = 1
  HEAP_EXT_DATA_ELEMENT.Size = E
  BIOS spec version element:
    Major = 2
    Minor = 1
    Revision = 0
  HEAP_EXT_DATA_ELEMENT.Type = 2
  HEAP_EXT_DATA_ELEMENT.Size = 14
  BIOS ACM element:
    NumAcms = 0x1
    BiosAcM #0 address = 0xFFFF89000
```

```
*****
*           TPM Information           *
*****
TPM Offsets from FED40000h:
-----
ACCESS 0h
[0] tpmEstablishment = 0
[5] activeLocality = 0
[7] tpmRegValidSts = 0

VID 0F00h = 0x1114
DID 0F02h = 0x3203
RID 0F04h = 0xFC

...

Platform Supplier 0x50000001 (PS Index)
02 02 00 01 13 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 02 00 00 00 00 00 00 00 00
00 00

...

AUX 0x50000003
FF FF FF FF 09 12 14 20 06 B0 00 80 00 01 FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
AF F1 65 2A FF 3C C7 3D 52 B2 9B 44 C5 A7 55 4A
BD 4F 1D 43 84 19 00 00 FF FF FF FF FF FF FF FF

...
```

TPM summary,  
confirm:

- AUX and PS indices are defined
- TPM Enabled and activated
- Indices are locked on production systems

**Note:** PS and Aux Index values will change depending on TPM 1.2 vs. 2.0, Provisioning process and ACM loaded to BIOS

Make sure the Intel® TXT checks are passing before proceeding measured launch

```
-----
SUCCESS: TXT is enabled in the BIOS and platform appears ready for TXT.
```



---

## 13.4.2 TPM 1.2 Requirements

### 13.4.2.1 TPM Compatibility Matrix

For TPM 1.2 based platform, Intel® TXT requires the TPM 1.2 to be compliant to the **TPM 1.2 Rev 116 Specification** (as per TCG Conformance Suite) and must adhere to the TCG PC Client Specific TPM Interface Specification (TIS) 1.21. Details of the requirements are specified in the Trusted Platform Module - Trusted Execution Technology Requirements document. The readiness of the TPM can be determined using the TPM Compliance Matrix listed in this document. The TPM Compliance Matrix is used by TPM vendors to determine Intel® TXT compliance for their TPMs.

Check with the TPM vendor(s) for their Intel® TXT Compliance Matrix results to determine Intel® TXT readiness.

### 13.4.2.2 AUX and PS Indices Provisioned

In addition to checking for a compliant TPM, user must also check that the Intel® TXT TPM NV indices are properly created in the TPM NV. For this platform, Intel® TXT requires the AUX and PS indices to be defined as specified in the *Intel® TXT TPM NV Requirement* for detail on the correct format. Refer to Appendix B for description of the expected TPM NV provisioning using the BIOS development reference code tools.

### 13.4.2.3 Checking AUX Index Accessibility

Use the **txtinfo64.efi** tool to verify this Index was created and is accessible.

Return code of zero indicates that the AUX index is created and accessible for Intel® TXT to use.

### 13.4.2.4 Checking PS Index Accessibility

Use the **txtinfo64.efi** to confirm that the PS index is created and properly provisioned.

### 13.4.2.5 Checking TPM NV Locking Status

As specified in the *Intel® TXT BIOS Specification* and *TPM NV Storage Interface Usage* documents, Intel® TXT requires that the AUX and the PS indices are locked by the platform supplier after these indices are defined. Locking the TPM NV before Intel® TXT feature is used on the platform prevents malicious software from corrupting the index area and compromising Intel® TXT integrity.

**TXINFO64.efi** can be used to determine the TPM NV locking status. Production SINIT ACM resets, if the TPM NV is not locked on the platform.



### 13.4.3 TPM 2.0 Requirements

#### 13.4.3.1 TPM Compatibility Matrix

For TPM 2.0 based platform, Intel® TXT requires the TPM 2.0 to be compliant to the **TPM 2.0 Rev 1.01 or latest specification** (as per TCG Conformance Suite). Details of the requirements are specified in the Trusted Platform Module - Trusted Execution Technology Requirements document. The readiness of the TPM can be determined using the TPM Compliance Matrix listed in this document. The TPM Compliance Matrix is used by TPM vendors to determine Intel® TXT compliance for their TPMs.

Check with the TPM vendor(s) for their Intel® TXT Compliance Matrix results to determine Intel® TXT readiness.

#### 13.4.3.2 AUX and PS Indices Provisioned

In addition to check for a compliant TPM, user must also check that the Intel® TXT TPM NV indices are properly created in the TPM NV. For this platform, Intel® TXT requires the AUX and PS indices to defined as specified in the *Intel® TXT TPM NV Requirement* for detail on the correct format. Refer to Appendix B for description of the expected TPM NV provisioning using the BIOS development reference code tools.

#### 13.4.3.3 Checking AUX and PS Index Accessibility

Use the **txtinfo64.efi** and the command **txtinfo64.efi -c:t** to confirm that the *INDEX\_AUX* and *PS Index* has been created.

```
*****
TXTINFO64 v1.5.10
Built: 10:04:24 Oct  3 2014
Intel Corporation
Copyright (c) 2010-2014
*****
Collecting Chipset information...Done.
Collecting CPU...Done.
Collecting TXT Registers...Done.
Collecting ACM...Done.
Collecting VTd...Done.
Collecting Heap...Done.
Collecting TPM...Done.
Testing CPU...Done.
Testing TXT Reg...Done.
Testing Heap...Done.
Testing VTd...Done.
*****
*                TPM Information                *
*****
TPM Offsets from FED40000h:
-----
ACCESS 0h
[0] tpmEstablishment          = 0
[5] activeLocality            = 0
```



```

[7] tpmRegValidSts                = 0

VID 0F00h                        = 0x1114
DID 0F02h                        = 0x3203
RID 0F04h                        = 0xFC

AUX Index:
FF FF FF FF 09 12 14 20 06 B0 00 80 00 01 FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
08 F9 9B C4 EC 4A 26 5B 54 08 7D C0 59 FF E6 E6
A1 52 6B C3 84 19 00 00 FF FF FF FF FF FF FF FF

PS Index:
00 03 0B 00 01 10 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 02 00 00 00 00 09 00 0C 00
00 00 08 00 00 00 01 02 03 04 05 06 07 08 09 0A
0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A
1B 1C 1D 1E 1F 20

```

## 13.5 BIOS-BIOS AC

### 13.5.1 Check BIOS-BIOS AC Integration

Once the key hardware and software components are confirmed to be Intel® TXT capable, the next step is to verify that the BIOS AC module integration is done correctly. Items to check are:

1. SCHECK has registered the ACM in the TPM.
2. Basic BIOS AC operation.

Details on BIOS requirements are out of scope for this document. For more information on BIOS AC module integration, refer to Chapter 2 of the *"Intel Trusted Execution Technology BIOS Specification"*.

#### 13.5.1.1 BIOS AC SCHECK

SCHECK verifies that the called AC module is registered in the TPM NVRAM for consumption by Intel® TXT software later in the boot sequence.

A method to check SCHECK completion is to confirm that the ACM is registered in the TPM. To do this, use the *aux2\_read.bat (TPM1.2)* or *TXTINFO64 (TPM2.0)* and observe the first 20 bytes to determine, if the ACM is registered. Use the same execution method described above in [Section 13.4.2.3](#).

#### 13.5.1.2 BIOS Memory Map

Confirm that the BIOS is properly setting up the memory map according to the *Intel® TXT BIOS Specification*. Some key mappings to be evaluated are SINIT space, Intel® TXT public space, Intel® TXT private space and heap memory region. These regions can be evaluated using **txtinfo64.efi**. Observe the Intel® TXT Memory Map settings for egregious overlaps. Refer to txtinfo.efi sample output in section The method described in this document uses the following development tools provided by Intel



Corporation. Tools are provided as Intel® TXT Client Debug Toolkit, which contains 64-bit tools. Make sure user have access to these tools prior to checkout. The reader is advised to review the tool release notes for actual syntax.

## 13.6 Measured Launch

With the BIOS dependency met, the next validation consideration is to launch an Intel® TXT MLE (measured launch environment). By launching a MLE, user can validate that the Intel® TXT platform components: processor, chipset, TPM and AC modules are working together as expected.

Measured Launch is a key Intel® TXT feature. Thorough evaluation of the process is recommended. This section describes a two-tier approach to checkout measured launching.

The first level checkout is a fundamental check to make sure the infrastructure components (processor, chipset, TPM and ACM) can collaborate to deliver the measure launch feature. This first level checkout allows better isolation of measured launch related issues. The second level checkout is to verify that the platform is capable of supporting the targeted MLE.

### 13.6.1 Fundamental Measured Launching with getsec64.efi

To facilitate fundamental Intel® TXT checkout, Intel Corporation makes available the **getsec64.efi** tool. To launch an MLE using **getsec.efi** perform the following steps:

1. Boot into the EFI-shell
2. Execute the following command:

```
Shell> getsec64.efi -l SENTER -a <SINIT AC-filename>
```

3. If the command above is failing on TGL platform, then use the following command line.

```
Shell> getsec64.efi -l SENTER -a <SINIT AC-filename> -i
```

<SINIT AC-filename> is the SINIT AC module to be released with the platform.

```
-s hashId: TPM2 hash algorithm <#> is (1 - SHA1, 2 - SHA256, 3 - Both)
-e PCR Extend Policy Control: <*> is (0 - Algorithm Agile Command set, 1
- Embedded hashing SW)
```

Measured launch failure can be diagnosed using the TXT.ERRORCODE register. This register can read from the EFI shell using **txtinfo64.efi**.

Error code description is distributed with the ACM package.

Measured launch Success can be seen after the Getsec64 command is launched as seen below:

```
*****
```





```
GETSEC64 v1.2.x
Built: Sep 16 2013 11:17:11
Intel Corporation
Copyright (c) 2010-2013
*****
GETSEC[SENTER] complete. System is now in TXT Environment.
```

### 13.6.2 Targeted Measured Launching

Once the fundamental checkout is completed, the next step is to validate that the BIOS has met all the requirements for targeted MLE. This verification is accomplished by configuring and installing the MLE.

At the time of this document, the publicly available MLE is Trusted Boot (tboot) is available at <http://www.bughost.org/repos.hg/tboot.hg>

MLE specific Intel® TXT checkout is dependent on architecture and capability of the targeted MLE. For the reference, Appendix B describes how Intel® TXT enabled Tboot can be used in the validation flow.

## 13.7 Verified Launch

Intel® TXT Verified Launch can be evaluated by installing a launch control policy (LCP) to restrict the platform to only launch the MLE that is allowed by policy. For more information on Intel® TXT LCP, refer to the “*Intel® Trusted Execution Technology: MLE Developer’s Guide*”.

Launch control policies are typically provided the by ISV for the corresponding MLE. If your ISV does not provide an LCP for the targeted MLE, LCP can be defined using the Intel® Trusted Execution Technology LCP Tools Reference Kit. Linux\* based reference code is available from Intel. Check with the Intel engineering representative for appropriate policy for test environment.

Once the policy is defined, confirm that launch environment successfully launched or not launched per the defined policy.

Platform Supplier (PS) default policy definition (PS\_ANY) is recommended to support a “boot-any” scenario.

This recommendation supports the platform owners to define the launch control policy per their business needs. This configuration is most representative of the Intel® TXT TTM configuration.

## 13.8 Measured Launch Environment

Once the measured environment is established and Intel® TXT has been confirmed as the launch mechanism, the last step is to validate that the MLE works as expected.

If the targeted virtual environment and applications, utilize the Intel® TXT security foundation, then those particular tools and features should be executed and validated for proper operation. Making the platform Intel® TXT ready for those ISVs is important.



In this context, the Intel® TXT measured launch environment can be validated with custom applications that make use of the trusted measurements in PCR17/18.

Here's a sample of PCR17/18 readout from TXTINFO64 tool:

```
PCR 17: 25 1E 8F B4 84 D1 7B 96 63 C2 69 E4 CE 5C CE D3
        D3 26 27 8A
```

```
PCR 18: FA 2D 64 7C 61 A8 29 1C 76 01 03 97 D1 82 D7 1A
        62 34 2F 35
```

```
System is in TXT Environment.
```

Without software that utilizes the Intel® TXT launched environment, validation should evaluate proper operation for a representative set of Intel® TXT-agnostic software.

Basically, validate that the software workload works the same in the Intel® TXT measured environment as it does in the non-measured environment.

This chapter highlights some focus areas that the validation software should stress.

### 13.8.1 Basic Stability

Define a workload that stresses the system broadly but not deeply. Select or develop applications that stress the SMP architecture, ALU operations, system memory management, file manipulation and networking. This test suite should validate the system for general robustness.

### 13.8.2 Functional Comprehensive

Define a workload that utilizes the Intel® TXT trusted environment, once it has been established. Currently, there is no generally available application or software that utilizes this security foundation. However an application can be developed to simulate an application utilizing the stored measurements to extend the trust boundary of the system.

### 13.8.3 Platform Stability

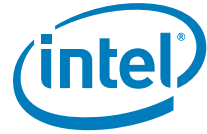
Define a workload that stresses the system as it would be used in the targeted platform. Software categories to include are: networking, virus scan, games, photo/video editing, content management, personal finance, business applications and web browsers.

### 13.8.4 BIOS/ACM Update Consideration

Once Intel® TXT has been used to launch an MLE, the TPM Establishment will be set to associate the system with the AC modules that were used to launch the environment.

TPM Establishment needs to be reset as per the *Intel® TXT BIOS Specification*. Improper update causes the ACM to be out of synchronous with the established environment.

This feature should be included in the validation plan. Suggested sequence to confirm that TPM Establishment is being reset by the BIOS update process:



1. Launch and exit a measured environment using one of the methods described above in [Section 13.7](#) or [Section 13.8](#).
2. Update the BIOS using the customer's method.
3. Run TXTINFO64 to confirm that TPM Establishment is cleared.

## 13.9 Secret Memory Protection Using SCLEAN

The last validation consideration is assuring the secret memory clean capability taking down of an Intel® TXT trusted environment is properly configured and ready for use by the application software.

Intel® TXT provides the ability to clean the memory in case of a planned or unexpected power loss using SCLEAN function. In proper operation, the measured launch environment take down is not perceptibly different from non-measured environment. For validation purpose, confirm that the MLE take down does not behave differently from a non-measured environment take down.

The special Intel® TXT validation consideration occurs, when a MLE is brought down improperly (Example: Sudden power loss) and the TXT.CMD.SECRETS flag is set to 1 by the MLE. In this scenario, at the next power up, Intel® TXT detects a potential security risk and scrub system memory using SCLEAN before resuming operation.

This Secret Memory Protection validation should be done on all memory configurations targeted for the platform. The following two scenarios can be used to confirm that BIOS and the BIOS AC (SCLEAN) are collaborating to deliver this protection.

### 13.9.1 Set Secret Scenario

Set the secret bit in the trusted environment and remove power to system. To simulate this memory protection scenario perform the following steps:

1. Launch an MLE using one of the methods described in [Section 13.7](#) or [Section 13.8](#).

**Note:**

*Tboot* automatically sets the secret flag upon successful launch, so step 2 is not necessary, if *tboot* is used to establish the measured launch environment.

2. Set the secret condition using one of the following methods:

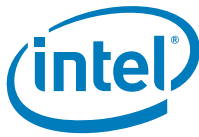
- a. With ITP/XDP with the following command:

Using ITP 1 'p[0]>ord4 0xfed208e0p=1' (data value not important)  
 Using ITP 2 '>>>itp.threads[0].mem("0xfed208e0p",4,1)' (data value not important)

- b. With **secrets64.efi** using:

```
EFI> secrets64.efi -s
```

3. Power-down the system.
4. Power-up the system.



### 13.9.2 Secret Status Unknown Scenario

Another way to trigger memory protection is by pulling down the RTESTB. This flags to Intel® TXT, the system was brought down improperly and may be at risk. To simulate this condition, do the following steps:

1. Launch an MLE using one of the methods described in [Section 13.7](#) or [Section 13.8](#).
2. Power down the system.
3. Short or Pull the RTC battery for a minute or more to dissipate any residual charge.
4. Power up the system.

### 13.9.3 System Behavior with SLCEAN

Depending upon the result of SLCEAN function and state of Boot Guard technology, execution of SCLEAN may result in warm reset or a cold reset. Refer below for more details:

1. If Boot Guard technology is Disabled and SCLEAN function scrubs the system memory successfully, control is passed from BIOS ACM to BIOS, which is responsible for power down (global) reset.
2. If Boot Guard technology is Enabled (Active) and SCLEAN function scrubs the system memory successfully, control is retained by BIOS ACM and BIOS ACM performs the system reset. Control is not passed to BIOS to allow for Boot Guard protection.
3. If SCLEAN function does not scrub the system memory successfully, control is retained by BIOS ACM and BIOS ACM performs a warm reset. Warm reset ensures that TXT.Errorcode corresponding to SCLEAN failure is preserved for the next boot.

#### 13.9.3.1 How to Verify SCLEAN Manually

1. Enter TXT Environment.
2. Run the command 'secrets64.efi -s' to set secrets bit.
3. Run the command 'secrets64.efi -m' to set seed value.
4. Run the command 'secrets64.efi -v' and will see seeded value.

```
SECRETS64 1.0.9, Copyright (c) 2010-2016 Intel Corporation
DEBUG - After First Call -- GetMemoryMap() -- Size = 0x29A0
DEBUG - After Second Call -- GetMemoryMap() -- Size = 0x27F0
Seed Value: 0xDEADBEEF
Scanning address range: 0x0 - 0x57FFF
Scanning address range: 0x59000 - 0x9DFFF
First Seed value 0xDEADBEEF found at address 0x59000
Number of Seed Values 0xDEADBEEF found: 70656
Scanning address range: 0x100000 - 0x87A80FFF
First Seed value 0xDEADBEEF found at address 0x100000
Number of Seed Values 0xDEADBEEF found: 568722432
Scanning address range: 0x87AB8000 - 0x88BDDFFF
First Seed value 0xDEADBEEF found at address 0x87AB8000
Number of Seed Values 0xDEADBEEF found: 4495360
Scanning address range: 0x88CBC000 - 0x88D9AFFF
First Seed value 0xDEADBEEF found at address 0x88CBC000
Number of Seed Values 0xDEADBEEF found: 228352
```



```
Scanning address range: 0x88F2B000 - 0x88F6EFFF
First Seed value 0xDEADBEEF found at address 0x88F2B000
Number of Seed Values 0xDEADBEEF found: 59394
Scanning address range: 0x88F84000 - 0x88F84FFF
Scanning address range: 0x100000000 - 0x16DFFFFFFF
First Seed value 0xDEADBEEF found at address 0x100000000
Number of Seed Values 0xDEADBEEF found: 461373440
-----
Total Number of Seed Values 0xDEADBEEF found: 1034949634
```

5. Enter EFI shell after SLCEAN and run 'secrets64.efi -v', then user will see that seed value is not found. This verifies that clean occurred.

```
SECRETS64 1.0.9, Copyright (c) 2010-2016 Intel Corporation
Seed Value: 0xDEADBEEF
Scanning address range: 0x0 - 0x57FFF
Scanning address range: 0x59000 - 0x9DFFF
Scanning address range: 0x100000 - 0x87A80FFF
Scanning address range: 0x87AB8000 - 0x88BDDFFF
Scanning address range: 0x88CBC000 - 0x88D9AFFF
Scanning address range: 0x88F2B000 - 0x88F85FFF
Scanning address range: 0x88F8A000 - 0x88F8AFFF
Scanning address range: 0x100000000 - 0x16DFFFFFFF
Seed value 0xDEADBEEF was not found!
```

## 13.10 Trusted Platform Module (TPM) Establishment Management

Trusted Platform Module (TPM) Establishment, when set to "0" indicates that either currently or at some point in the past, a MLE is established; therefore, either currently or at some point in the past, the contents of memory may have contained secrets that were protected by the MLE. Because of its key role in triggering Intel® TXT secret memory protection, proper management of this indicator is required to ensure the Intel® TXT enabled platform delivers the appropriate protection.

An Intel® TXT validation plan should include checks to make sure TPM Establishment is only set, when appropriate.

### 13.10.1 Checking TPM Establishment

The TPM Establishment can be checked by reading 0xFED40000[0].

Bit 0 sets to "0" means TPM Establishment is set. Bit 0 set "1" means TPM Establishment is not set. Bit 31 is the valid bit.

The TXTINFO64 tool will show user in TPM section the TPM Establishment status.



### 13.10.2 Recommended TPM Establishment Behavior

Scenario	TPM Establishment Status
Shipped system default	Not set
Intel® TXT is enabled in the BIOS before measured launch is ever invoked	Not set
Intel® TXT is enabled in the BIOS and measured launch completed	Set
Intel® TXT is disabled in the BIOS	Not set
BIOS updates	Not set
BIOS ACM updates	Not set
System memory configuration changes	Not set

### 13.10.3 Resetting Trusted Platform Module (TPM) Establishment

Once the checkout process is completed, it is recommended that the TPM Establishment be reset. If the BIOS being evaluated does not provide a mechanism to reset the TPM Establishment explicitly or when Intel® TXT is disabled, user can manually reset the TPM Establishment using the **getsec64.efi** tool.

Use the following command:

```
Shell> getsec64.efi -l ENTERACCS -a <BIOS AC-filename> -fn Est
```

## 13.11 Summary

Complete validation of an Intel® TXT enabled client platforms can be done by focusing on the key security feature, *Intel® TXT Verified Launch*. Verified launch effectively exercises all the key Intel® TXT hardware/software components and validates that the components work correctly and are configured properly to deliver this platform feature.

This validation guide describes a strategy to validate verified launch from a bottom-up approach. This bottom-up strategy starts with validating the hardware and software components for compliance and proper operations. Then the validation consideration is brought up to the next Intel® TXT intercept, the BIOS-BIOS AC integration. Then, key SINIT-AC integration checks are considered. Then, user looked at the expected behavior of the measured launch environment. Lastly, controlled take-down of the measured launch environment was considered, with particular focus on the secret memory protection.

## 13.12 Intel® TXT Test Plan

This sections describes sample Intel® TXT checkout plans and the tools that can be used to evaluate the platform for Intel® TXT measured launch and secret protection.

For the development environment, where a quick evaluation of implementation is desired, the test plan described in [Section 13.12.2, "Intel® TXT Baseline Coverage Summary,"](#) does a minimal check of the key Intel® TXT features. To further reduce testing time, the test iteration specified in test cases can be minimize to fit allotted time.



**Note:** Passing the test cases in the Intel® TXT Baseline Coverage Summary only establishes key TXT functionality/features and is not considered adequate for complete Intel® TXT checkout.

The test plan in [Section 13.12.3](#), “Test Plan,” is targeted for complete validation and compliance determination. It includes a number of test cases that evaluates platform robustness. Intel recommends that platform suppliers refer to this test plan for more thorough validation of the Intel® TXT implementation on the platforms.

## 13.12.1 Test Prerequisite

Prerequisite Checklist	Location
<b>Intel Provided Tools</b>	
<b>getsec64.efi, txtinfo64.efi, secrets64.efi, pcrdump64</b> – “Intel® Trusted Execution Technology: Intel® TXT Client Debug Toolkit”	VIP# 125920
<b>aux2_read.bat, aux2_cap.bat, ps_read, ps_cap.bat</b>	Distributed with ACM package
<b>TPM Provisioning tool for use with Intel® Trusted Execution Technology (TPM 1.2)</b> - DOS based TPM Provisioning development only tool	Distributed with ACM package (in zip folder called “BIN”)
<b>TPM Provisioning tool for use with Intel® Trusted Execution Technology (TPM 2.0)</b> - EFI based TPM Provisioning development only tool	Distributed with ACM package (in zip folder called “TPM2ProvTool”)
<b>TPM Provisioning tool for use with Intel® Trusted Execution Technology (TPM 2.0) with System Guard</b> - EFI based TPM Provisioning development only tool	Distributed with ACM package (in zip folder called “System Guard PS2”)
<b>BIOS EFI Shell or DUET</b>	<a href="http://sourceforge.net/apps/mediawiki/tianocore/index.php?title=EDK">http://sourceforge.net/apps/mediawiki/tianocore/index.php?title=EDK</a>
<b>Tboot</b> – Trusted boot module	<a href="http://www.bughost.org/repos/hg/tboot.hg/">http://www.bughost.org/repos/hg/tboot.hg/</a>
<b>Intel® TXT Trusted Boot (tboot) Usage LiveImage</b>	Posted on VIP
<b>BIOS Requirement</b>	
Intel® VT, Intel® VT-d enabled	
BIOS AC integration complete	
Support for TPM Establishment reset in BIOS or BIOS update	
System restore flash image to use with SCLEAN check	
TPM1.2 or TPM2.0 support	
<b>System Requirement</b>	
Representative sample of production memory configuration	
TPM NV indices created and locked (production version)	
If platform is targeted to support multiple TPM	
• TPM swapping capability	
• Sample of targeted TPM	
ITP or Intel® Debug Tool hooks (desired)	
<b>ACM</b>	
SINIT ACM - compatible to targeted chipset	Posted on VIP



### 13.12.2 Intel® TXT Baseline Coverage Summary

This section describes a short test plan that can be used to verify basic Intel® TXT functionality. This test plan is a minimal set of test cases that exercise the platform's capability to support measured launch and secret protection.

**Note:** Passing the test cases in the Intel® TXT Baseline Coverage Summary only establishes key TXT functionality/features and is not considered adequate for complete Intel® TXT checkout.

For a comprehensive Intel® TXT validation plan that is targeted for the validation environment, refer to [Section 13.12.3](#).

Test ID Number	Test Case Title	PETS/Manual
TXT_TC0001A	Check for Intel® TXT Components	Manual
TXT_TC0002A	Check AUX Index	Manual
TXT_TC0002B	Check PS Index	Manual
TXT_TC0002C	Verify indices are locked in TPM NV	Manual
TXT_TC0004A	SINIT, when Intel® TXT is enabled	Manual
TXT_TC0004D	Power loss after SINIT without secret	Manual
TXT_TC0004E	Power loss after SINIT with secret	Manual
TXT_TC0004G	Power loss after SINIT and RTC battery pulled	Manual
TXT_TC0004I	TPM Establishment set when the secret is undetermined	Manual
TXT_TC0004N	PCR17/18 Integrity	Manual
TXT_TC0005A	SCLEAN with targeted memory configurations	Manual
TXT_TC0006C	Tboot with Intel® TXT	Manual
TXT_TC0006D	S3 Tboot with Intel® TXT	Manual
TXT_TC0007A	Factory Default TPM Establishment Setting	Manual
TXT_TC0007B	TPM Establishment when Intel® TXT is disabled	Manual

### 13.12.3 Test Plan

This section describes a comprehensive test plan for the validation environment and compliance determination. Extending on the Baseline test plan, listed above in [Section 13.12.2](#), "Intel® TXT Baseline Coverage Summary," this test plan includes additional test cases to evaluate the platform's robustness. Robustness in this context refers to:

1. How well the platform functions with various configurations, such as different memory sizes;
2. How well it handles repeated invocation. This test plan can be used as a framework and can be customized to define a Intel® TXT test plan appropriate for the validation environment and coverage objective.

Test ID Number	Test Case Title	PETS/Manual
TXT_TC0001A	Check for Intel® TXT Components	Manual
TXT_TC0002A	Check AUX Index	Manual
TXT_TC0002B	Check PS Index	Manual





Test ID Number	Test Case Title	PETS/Manual
TXT_TC0002C	Verify that indices are locked in the TPM NV	Manual
TXT_TC0003A	SMX Disabled	Manual
TXT_TC0003B	SINIT when Intel® TXT is disabled	Manual
TXT_TC0003C	SMX when Intel® TXT is enabled	Manual
TXT_TC0004A	SINIT when Intel® TXT is enabled	Manual
TXT_TC0004B	Cold boot after SINIT	Manual
TXT_TC0004C	Warm boot after SINIT	Manual
TXT_TC0004D	Power loss after SINIT without secret	Manual
TXT_TC0004E	Power loss after SINIT with secret	Manual
TXT_TC0004G	Power loss after SINIT and RTC battery pulled	Manual
TXT_TC0004H	Power loss after SINIT with secret	Manual
TXT_TC0004I	TPM Establishment set when the secret is undetermined	Manual
TXT_TC0004J	TPM Establishment not set	Manual
TXT_TC0004K	SINIT cycle testing	Manual
TXT_TC0004L	SINIT cycle testing with cold boot	Manual
TXT_TC0004M	SINIT cycle testing with warm boot	Manual
TXT_TC0004N	PCR17/18 Integrity	Manual
TXT_TC0005A	SCLEAN with targeted memory configurations	Manual
TXT_TC0006A	Windows* with Intel® TXT	Manual
TXT_TC0006B	Windows* S3 with Intel® TXT	Manual
TXT_TC0006C	Tboot with Intel® TXT	Manual
TXT_TC0006D	S3 Tboot with Intel® TXT	Manual
TXT_TC0007A	Factory Default TPM Establishment Setting	Manual
TXT_TC0007B	TPM Establishment when Intel® TXT is disabled	Manual
TXT_TC0007C	TPM Establishment after BIOS Update	Manual
TXT_TC0008A	Intel® TXT and Intel® AMT Interoperability	Manual
TXT_TC0008B	Tboot with Intel® VT-d enabled Linux* or Xen*	Manual
TXT_TC0008C	Intel® TXT when CSME is disabled	Manual
TXT_TC0008D	Intel® TXT when CSME is enabled	Manual

Test ID	TXT_TC0001A
Test Case Title	Check for Intel® TXT Components
Mandatory/Optional	Mandatory
Description	Verify that platform has Intel® TXT enabled processor, chipset and TPM required for Intel® TXT execution
Objective	This test to determine that the HW and SW components are required on the targeted test platform
Procedure	<b>For TPM1.2/2.0:</b> EFI: Run "TXTINFO64 -c:a -p" at the prompt
Test Pass/Fail Criteria	Test passes, if all the components required for TXT are present as reported by the tools



Test ID	TXT_TC0002A
Test Case Title	Check AUX Index
Mandatory/Optional	Mandatory
Description	Checks existence of the Intel® TXT Aux index
Objective	This test to determine that the TPM NV has been properly provisioned for Intel® TXT with the AUX index defined as specified
Procedure	<b>For TPM1.2:</b> DOS: Run "aux2_read.bat" or "aux2_cap.bat" EFI: Run "TXTINFO64 -c:a -p" at the prompt  <b>For TPM2.0:</b> EFI: Run "TXTINFO64 -c:a -p" at the prompt
Test Pass/Fail Criteria	The test pass, if the aux2_read.bat, TXTINFO64 shows that the AUX index is defined, accessible and locked.

Test ID	TXT_TC0002B
Test Case Title	Check PS Index
Mandatory/Optional	Mandatory
Description	Check the existence of the PS index as required by the platform
Objective	This test to determine that the PS is properly provisioned for Intel® TXT execution on the targeted platform
Procedure	<b>For TPM1.2:</b> DOS: Run "ps_read.bat" EFI: Run "TXTINFO64 -c:t -p" at the prompt  <b>For TPM2.0:</b> EFI: Run "TXTINFO64 -c:t -p" at the prompt
Test Pass/Fail Criteria	The test pass, if the ps_read.bat, TXTINFO64 shows that the PS is defined as specified by the Intel® TXT BIOS Specification. <b>NOTE:</b> Use latest TPM Provisioning scripts that are included in the ACM kit that user is using. If older TPM scripts are used, then user gets system reset upon enabling TXT.

Test ID	TXT_TC0002C
Test Case Title	Verify that the indices are locked in the TPM NV
Mandatory/Optional	Mandatory only for production systems
Description	Verify that the AUX index is locked in the TPM NV
Objective	This test verifies that AUX index is locked in the TPM NV as required by the SINIT ACM
Procedure	<b>For TPM1.2/TPM2.0:</b> EFI: 1. Boot to EFI-Shell 2. Run "TXTINFO64 -c:t -p" at the prompt
Test Pass/Fail Criteria	Test passes, if TXTINFO64 indicates the TPM NV indices are properly locked in the TPM NV



Test ID	TXT_TC0003A
Test Case Title	SMX Disabled
Mandatory/Optional	Mandatory
Description	With Intel® TXT and supporting options disabled in BIOS, verify SMX is properly disabled
Objective	Verify the BIOS is properly managing the SMX feature control in the processor
Procedure	1. Disable TXT in the BIOS. 2. Confirm using TXTINFO 64 that the platform is not ready for TXT. EFI: Run "TXTINFO64 -c:a -p" at the prompt
Test Pass/Fail Criteria	Test passes, if the <i>SENTER enable</i> and <i>control</i> bits are deasserted in the IA32_FEATURE_CONTROL MSR

Test ID	TXT_TC0003B
Test Case Title	SINIT, when Intel® TXT is disabled
Mandatory/Optional	Optional
Description	Verify SINIT does not run, when Intel® TXT is disabled in BIOS with GetSec
Objective	Ensure the BIOS is properly configuring the platform to disallow Intel® TXT measured launch when Intel® TXT is disabled in the BIOS
Procedure	1. Disable TXT in the BIOS. 2. Boot to EFI-Shell. 3. Run "GETSEC64 -l SENTER -a SINIT.BIN" at the prompt. 4. Run "GETSEC64 -l SEXIT" at the prompt. <b>NOTE:</b> If this test case fails or hangs at step 3, run the test again with "GETSEC64 -l SENTER -a SINIT.BIN -i".
Test Pass/Fail Criteria	Test passes, if user is not able to complete the SENTER. The following error messages will appear error message saying: "Error: SINIT base register is not programmed" leaf = 0x20 "Error: System is NOT in TXT environment."

Test ID	TXT_TC0003C
Test Case Title	SMX, when Intel® TXT is enabled
Mandatory/Optional	Mandatory
Description	With Intel® TXT option enabled in BIOS, verify SMX is properly enabled
Objective	Determine that the BIOS is properly configuring the processor for SMX execution, when Intel® TXT is enabled in the BIOS
Procedure	1. Enable Intel® TXT in the BIOS. 2. Verify with either TXTINFO64. EFI: 1. Boot to EFI-Shell. 2. Run "TXTINFO64 -c:a -p" at the prompt.
Test Pass/Fail Criteria	Test passes, if the <i>SENTER enable</i> and <i>control</i> bits are asserted in the IA32_FEATURE_CONTROL MSR



Test ID	TXT_TC0004A
Test Case Title	SINIT, when Intel® TXT is enabled
Mandatory/Optional	Mandatory
Description	Verify successful SINIT with GETSEC64
Objective	Verify that the BIOS has properly configured the platform to support a basic measured launch with SINIT
Procedure	1. Enable Intel® TXT in the BIOS. 2. Boot to EFI-Shell. 3. Run "GETSEC64 -I SENTER -a SINIT.BIN". 4. Run "GETSEC64 -I SEXIT". 5. Repeat steps 2-3, three times.
Test Pass/Fail Criteria	Test passes, if the platform successfully enters and exits the Intel® TXT trusted environment
Note	To run System Guard on this platform the PO TPM Index is created. To run this test in EFI shell, delete the PO Index first then run this test. Recommend that these compliance tests are run before testing System Guard

Test ID	TXT_TC0004B
Test Case Title	Cold boot after SINIT
Mandatory/Optional	Mandatory
Description	Verify system shutdown and cold boot after SENTER, GetSec Wakeup, SMCONTROL then SEXIT (three times)
Objective	Ensure that platform can be shutdown and booted after post Intel® TXT measured launch
Procedure	1. Enable Intel® TXT in the BIOS. 2. Boot to EFI-Shell. 3. Run "GETSEC64 -I SENTER -a SINIT.BIN". 4. Run "GETSEC64 -I SEXIT". 5. Do a cold boot. 6. Repeat all steps three times.
Test Pass/Fail Criteria	Test passes, if the platform can shutdown and boot after the trusted environment had been established

Test ID	TXT_TC0004C
Test Case Title	Warm boot after SINIT
Mandatory/Optional	Mandatory
Description	Verify system reboot after SENTER, GetSec Wakeup, SMCONTROL then SEXIT (three times)
Objective	Ensure that platform can be shutdown and boot post Intel® TXT measured launch
Procedure	1. Enable Intel® TXT in the BIOS. 2. Boot to EFI-Shell. 3. Run "GETSEC64 -I SENTER -a SINIT.BIN". 4. Run "GETSEC64 -I SEXIT". 5. Do a warm boot, for example, "reset -w". 6. Repeat all steps three times.
Test Pass/Fail Criteria	Test passes, if the platform can shutdown and booted after the trusted environment had been established



Test ID	TXT_TC0004E
Test Case Title	Power loss after SINIT with secret
Mandatory/Optional	Mandatory
Description	<p>Verify power loss with secrets and verify it causes SCLEAN (then reboot) and then boot (three times).</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. In order to observe SCLEAN, watch power LED or post code read out to make sure after SCLEAN happens: system shuts down and restarts to scrub memory, shuts down again followed by a restart, returning to normal state.</li> <li>2. Time taken to run SCLEAN (scrub system memory) is dependent upon how much memory is populated. If the memory in the system is 16 GB or 32 GB, it will take more time than, if the system only has 1 GB or 2 GB.</li> </ol>
Objective	Validate that the platform can support repetitive secret protection
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® TXT in the BIOS</li> <li>2. Boot to EFI-Shell</li> <li>3. Run "GETSEC64 -I SENTER -a SINIT.BIN"</li> <li>4. Run "SECRETS64 -S" at the prompt.</li> <li>5. Restart system</li> <li>6. Watch SCLEAN occur</li> <li>7. Repeat steps 2-6, three times</li> </ol>
Test Pass/Fail Criteria	<p>The test passes, if SCLEAN is invoked on each improper shutdown with secret set.</p> <p><b>NOTE:</b> Refer <a href="#">Section 13.9.3.1</a> for SCLEAN Manual Check steps</p>

Test ID	TXT_TC0004G
Test Case Title	Power loss after SINIT and RTC battery pulled
Mandatory/Optional	Mandatory
Description	Verify total power loss without secrets (coin cell battery failure) after SENTER, GetSec Wakeup, SMCONTROL and verify it will cause SCLEAN and then boot (three times)
Objective	Validate that the platform provides secret protection, when the secret status is undetermined
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® TXT in the BIOS</li> <li>2. Boot to EFI-Shell</li> <li>3. Run "GETSEC64 -I SENTER -a SINIT.BIN"</li> <li>4. Turn off power supply</li> <li>5. Clear the CMOS by means of jumper or remove backup battery (coin) for 5 seconds</li> <li>6. Put backup battery (coin) back, if it is removed</li> <li>7. Turn on power supply and press the power button</li> <li>8. Watch SCLEAN occur</li> <li>9. Repeat steps 1 - 8 two more times (totaling three times)</li> </ol>
Test Pass/Fail Criteria	<p>The test passes, if the platform invokes an SCLEAN and boot as expected on each iteration.</p> <p><b>NOTE:</b> Refer <a href="#">Section 13.9.3.1</a> for SCLEAN Manual Check steps</p>

Test ID	TXT_TC0004H
Test Case Title	Power loss after SINIT with secret
Mandatory/Optional	Mandatory
Description	Verify total power loss with secrets (coin cell battery failure) after SENTER, GetSec Wakeup, SMCONTROL and verify it causes SCLEAN and then boot (three times)
Objective	Validate that the platform provides secret protection in spite of the powerloss



Test ID	TXT_TC0004H
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® TXT in the BIOS.</li> <li>2. Boot to EFI-Shell</li> <li>3. Run "GETSEC64 -I SENTER -a SINIT.BIN"</li> <li>4. Run "SECRETS64 -S" at the prompt.</li> <li>5. Turn off power supply</li> <li>6. Clear the CMOS by means of jumper or remove backup battery (coin) for 5 seconds</li> <li>7. Put backup battery (coin) back if it is removed</li> <li>8. Turn on power supply and press the power button</li> <li>9. Watch SCLEAN occur</li> <li>10. Repeat steps 1–9, two more times (totaling three times)</li> </ol>
Test Pass/Fail Criteria	<p>The test passes, if the platform invokes an SCLEAN and boot as expected on each iteration.</p> <p><b>NOTE:</b> Refer <a href="#">Section 13.9.3.1</a> for SCLEAN Manual Check steps</p>

Test ID	TXT_TC0004I
Test Case Title	TPM Establishment set, when the secret is undetermined
Mandatory/Optional	Mandatory
Description	Verify total power loss with establishment bit asserted (0) in TPM (coin cell battery failure), verify it causes SCLEAN and then boot (three times)
Objective	Confirm that the platform provides secret protection, when the secret status on the platform is undetermined
Procedure	<p>Establish TPM Establishment to enable TXT protection by:</p> <ol style="list-style-type: none"> <li>1. Enable Intel® TXT in the BIOS</li> <li>2. Boot to EFI-Shell</li> <li>3. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li> <li>4. Run "GETSEC64 -I SEXIT" at the prompt</li> <li>5. Put the secret flag in an undetermined status by:</li> <li>6. Turn off power supply</li> <li>7. Clear CMOS by means of jumper or remove backup battery (coin) for 5 seconds</li> <li>8. Put backup battery (coin) back, if removed</li> <li>9. Turn on power supply and press the power button</li> <li>10. Watch SCLEAN occur</li> <li>11. Repeat steps 1–8, two more times (total three times)</li> </ol>
Test Pass/Fail Criteria	<p>Test passes, if the platform successfully boots in each iteration</p> <p>On successful SCLEAN, system resets, and boot again normally.</p> <p><b>NOTE:</b> Refer <a href="#">Section 13.9.3.1</a> for SCLEAN Manual Check steps</p>

Test ID	TXT_TC0004J
Test Case Title	TPM Establishment not set
Mandatory/Optional	Mandatory
Description	Verify total power loss with establishment bit not asserted (1) in TPM (coin cell battery failure) verify it does not cause SCLEAN and then boot
Objective	Validate that the Intel® TXT protection does not unnecessarily get invoked on platform that has opted out
Procedure	<ol style="list-style-type: none"> <li>1. Disable Intel® TXT in the BIOS</li> <li>2. Boot to EFI-Shell</li> <li>3. Run "GETSEC64 -I ENTERACCS -a [BIOSAC.BIN] -fn EST" at the prompt</li> <li>4. Turn off power supply</li> <li>5. Clear the CMOS by means of jumper or remove backup battery (coin) for 5 seconds</li> <li>6. Put backup battery (coin) back, if it is removed</li> <li>7. Turn on power supply and press the power button</li> <li>8. Verify SCLEAN does NOT occur</li> </ol>
Test Pass/Fail Criteria	The platform boot as expected without invoking SCLEAN



Test ID	TXT_TC0004K
Test Case Title	SINIT cycle testing
Mandatory/Optional	Mandatory
Description	Verify the platform and Intel® TXT is functional and stable by running SENTER, GetSec Wakeup, SMCONTROL then SEXIT repeatedly 1000 times
Objective	Stress test measured launching on the platform
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® TXT in the BIOS</li> <li>2. Boot to EFI-Shell</li> <li>3. Run Test to loop SENTER and SEXIT 1000 times</li> </ol>
Test Pass/Fail Criteria	The platform successfully completes the SENTER cycle without issue

Test ID	TXT_TC0004L
Test Case Title	SINIT cycle testing with cold boot
Mandatory/Optional	Mandatory
Description	Verify the platform and Intel® TXT is functional and stable by executing cold boots after SENTER, GetSec Wakeup, SMCONTROL then SEXIT repeatedly 50 times
Objective	Stress test cold boot measured launching on the platform
Procedure	<ol style="list-style-type: none"> <li>1. Boot to EFI-Shell</li> <li>2. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li> <li>3. Run "GETSEC64 -I SEXIT" at the prompt.</li> <li>4. Run "reset" to perform a cold boot.</li> <li>5. Repeat steps 1-4, 50 times.</li> </ol>
Test Pass/Fail Criteria	The platform successfully completes the SENTER cycle without issue

Test ID	TXT_TC0004M
Test Case Title	SINIT cycle testing with warm boot
Mandatory/Optional	Mandatory
Description	Verify the platform and Intel® TXT is functional and stable by executing warm boots after SENTER, GetSec Wakeup, SMCONTROL then SEXIT repeatedly 50 times
Objective	Stress test warm boot measured launching on the platform
Procedure	<ol style="list-style-type: none"> <li>1. Boot to EFI-Shell</li> <li>2. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li> <li>3. Run "GETSEC64 -I SEXIT" at the prompt.</li> <li>4. Run "reset -w" to perform a warm boot.</li> <li>5. Repeat steps 1-4, 50 times.</li> </ol>
Test Pass/Fail Criteria	The platform successfully completes the SENTER cycle without issue



Test ID	TXT_TC0004N
Test Case Title	PCR17/18 Integrity
Mandatory/Optional	Mandatory
Description	PCR17/18 measured value correctness
Objective	Ensure that the measured value of the launch environment is correctly recorded in PCR17
Procedure	<ol style="list-style-type: none"><li>1. Boot to EFI-Shell</li><li>2. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li><li>3. Run "TXTINFO64 -c:a -p" at the prompt</li><li>4. Check that the PCR17/18 value matches the expected value</li><li>5. Run "GETSEC64 -I SEXIT" at the prompt.</li><li>6. Do a cold boot</li><li>7. Repeat steps 1-6, 10 times.</li></ol>
Test Pass/Fail Criteria	TXTINFO reports that PCR17/18 contains the expected measured value

Test ID	TXT_TC0005A
Test Case Title	SCLEAN with targeted memory configurations
Mandatory/Optional	Mandatory
Description	Verify SCLEAN functions with on all platform supported memory configurations
Objective	Validate that secret protection works on all targeted platforms
Procedure	<ol style="list-style-type: none"><li>1. Setup the platform to the desired memory configurations: test with all supported memory speeds (1333 MHz, 1600 MHz), slot combinations, sizes (4 GB, 8 GB, 16 GB, 32 GB), and max memory supported - 16/32/64 GB (using up to 8 Gb DRAM in dual channel, 2 DIMMs/channel)</li><li>2. Boot to EFI-Shell</li><li>3. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li><li>4. Run "SECRETS64 -S" at the prompt.</li><li>5. Turn off power supply</li><li>6. Turn on power supply and press the power button</li><li>7. Watch SCLEAN occur</li><li>8. Reset all BIOS settings (save and reset)</li><li>9. Repeat steps 1-8 two more times with different memory configurations, as suggested in Step 1.</li></ol>
Test Pass/Fail Criteria	SCLEAN completes and the platform boots as expected in a secret protection scenario. <b>NOTE:</b> Refer <a href="#">Section 13.9.3.1</a> for SCLEAN Manual Check steps

Test ID	TXT_TC0006A
Test Case Title	Microsoft* Windows with Intel® TXT
Mandatory/Optional	Optional
Description	Verify Windows* loads without issue with Intel® TXT options enabled in BIOS
Objective	Validate that the Intel® TXT implementation does not affect standard OS
Procedure	<ol style="list-style-type: none"><li>1. Preload Windows*</li><li>2. Enable Intel® TXT in the BIOS</li><li>3. Boot Windows*</li></ol>
Test Pass/Fail Criteria	Test passes, if the Windows* boot is not affected by TXT being enabled in the BIOS. The platform boots Windows* as normal.





Test ID	TXT_TC0006B
Test Case Title	Microsoft* Windows S3 with Intel® TXT
Mandatory/Optional	Optional
Description	Verify Windows* S3 works without issue, when Intel® TXT options enabled in BIOS
Objective	Validate that the Intel® TXT implementation does not affect standard OS
Procedure	<ol style="list-style-type: none"> <li>1. Preload Windows*</li> <li>2. Enable Intel® TXT in the BIOS</li> <li>3. Boot Windows*</li> <li>4. Put the platform into S3</li> <li>5. Bring the platform out of S3</li> <li>6. Shutdown the platform</li> <li>7. Repeat steps 1–6, two more times (totaling three times)</li> </ol>
Test Pass/Fail Criteria	The platform performs Windows* S3 as normal

Test ID	TXT_TC0006C
Test Case Title	Tboot with Intel® TXT
Mandatory/Optional	Mandatory
Description	Verify Tboot is capable of loading Linux*/Xen* without issue with Intel® TXT enabled in BIOS
Objective	Validates that the platform can support launching a TXT measured environment
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® TXT in the BIOS</li> <li>2. Preload a Intel® TXT enabled Linux* (Fedora Tboot LiveImage) or Xen* environment</li> <li>3. Boot Linux* or Xen* using tboot</li> </ol>
Test Pass/Fail Criteria	Test passes, if Tboot log/serial/screen shows that Intel® TXT launch was successful.

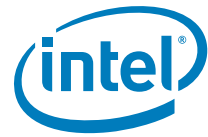
Test ID	TXT_TC0006D
Test Case Title	S3 Tboot with Intel® TXT
Mandatory/Optional	Mandatory
Description	Verify the platform can successful go into S3 and restore to a TXT measured
Objective	Validate that the platform can successful go into S3 and restore back into a TXT measured environment.
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® TXT in the BIOS</li> <li>2. Preload a TXT enabled Linux* or Xen* environment</li> <li>3. Boot Tboot-Linux*/Xen*</li> <li>4. Put the platform into S3</li> <li>5. Bring the platform out of S3</li> <li>6. Shutdown the platform</li> <li>7. Repeat steps 1–6, two more times (totaling three times)</li> </ol>
Test Pass/Fail Criteria	The test passes, if the platform restores from S3 and puts the system back into the measured environment



Test ID	TXT_TC0007A
Test Case Title	Factory Default TPM Establishment Setting
Mandatory/Optional	Mandatory
Description	TPM Establishment is not set in the default shipping configuration
Objective	Verify that the TPM establishment is not set in the manufacturing process
Procedure	1. Make sure the system in factory default state 2. Read memory location 0xFED40000[0] 3. The Establishment Bit can be found using TXTINFO64
Test Pass/Fail Criteria	0xFED40000[0] = 1

Test ID	TXT_TC0007B
Test Case Title	TPM Establishment when Intel® TXT is disabled
Mandatory/Optional	Mandatory
Description	TPM Establishment is not set, when Intel® TXT is disabled in BIOS
Objective	TPM Establishment is not set, when Intel® TXT disabled in the BIOS
Procedure	1. Disable Intel® TXT in the BIOS 2. Read memory location 0xFED40000[0] 3. The Establishment Bit can be found using TXTINFO64
Test Pass/Fail Criteria	0xFED40000[0] = 1

Test ID	TXT_TC0007C
Test Case Title	TPM Establishment after BIOS update
Mandatory/Optional	Mandatory
Description	TPM Establishment is not set, when the BIOS is updated
Objective	TPM Establishment is not set, when Intel® TXT and the BIOS is being updated
Procedure	1. Updated BIOS using the normal process 2. Read memory location 0xFED40000[0] 3. The Establishment Bit can be found using TXTINFO64
Test Pass/Fail Criteria	0xFED40000[0] = 1



Test ID	TXT_TC0008A
Test Case Title	Intel® TXT and Intel® AMT Interoperability
Mandatory/Optional	Optional
Description	Run measured launch on a platform that running Intel® AMT
Objective	Validate that the platform will support Intel® TXT and Intel® AMT concurrency
Procedure	<ol style="list-style-type: none"> <li>1. Enable CSME as instructed in the CSME section</li> <li>2. Enable Network Activation in Intel® MEBX AMT menu</li> <li>3. Boot to EFI-Shell</li> <li>4. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li> <li>5. Run "SECRETS64 -S" at the prompt.</li> <li>6. Turn off power supply</li> <li>7. Turn on power supply and press the power button</li> <li>8. Watch SCLEAN occur</li> </ol>
Test Pass/Fail Criteria	Success, if SCLEAN completes as expected

Test ID	TXT_TC0008B
Test Case Title	Tboot with Intel VT-d enabled Linux* (Tboot LiveImage) or Xen
Mandatory/Optional	Optional User can skip this, if do not have Intel® VT-d capable Xen* MLE. Alternatively, user may use the TXT Tboot LiveImage that also uses VT-d.
Description	Verify Intel® VT-d is functional within a Intel® TXT measured environment.
Objective	Validate that the Intel® TXT implementation does not affect standard VMM
Procedure	<ol style="list-style-type: none"> <li>1. Preload tboot to launch a Intel® VT-d Enabled Linux* or Xen* (that is, Xen* with VT-d patches and grub command line switch "iommu=1").</li> <li>2. Enable Intel® TXT and Intel® VT-d in the BIOS.</li> <li>3. Tboot Intel® VT-d enabled Linux* or Xen*.</li> <li>4. Assign a bus-device-fn of a device to guest.</li> </ol> (Refer to the Intel® VT-d section and the Tboot usage kit for additional detail).
Test Pass/Fail Criteria	Success criteria is the guest can access the device after assignment

Test ID	TXT_TC0008C
Test Case Title	Intel® TXT, when CSME is Disabled
Mandatory/Optional	Optional - If this option is provided by the BIOS
Description	Invoke measured launch and SCLEAN, when the platform has CSME disabled
Objective	Validate that the platform supports Intel® TXT independent of ME
Procedure	<ol style="list-style-type: none"> <li>1. Disable CSME as instructed in the CSME section</li> <li>2. Boot to EFI-Shell</li> <li>3. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li> <li>4. Run "SECRETS64 -S" at the prompt.</li> <li>5. Turn off power supply</li> <li>6. Turn on power supply and press the power button</li> <li>7. Watch SCLEAN occur</li> </ol>
Test Pass/Fail Criteria	Success, if SCLEAN completes as expected. <b>NOTE:</b> Refer to <a href="#">Section 13.9.3.1</a> for SCLEAN Manual Check steps.



<b>Test ID</b>	<b>TXT_TC0008D</b>
<b>Test Case Title</b>	Intel® TXT when CSME is Enabled
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	Invoke measured launch and SCLEAN, when the platform has CSME enabled
<b>Objective</b>	Validate that the platform supports Intel® TXT independent of ME
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Enable CSME as instructed in the CSME section</li><li>2. Boot to EFI-Shell</li><li>3. Run "GETSEC64 -I SENTER -a [SINIT.BIN]" at the prompt</li><li>4. Run "SECRETS64 -S" at the prompt.</li><li>5. Turn off power supply</li><li>6. Turn on power supply and press the power button</li><li>7. Watch SCLEAN occur</li></ol>
<b>Test Pass/Fail Criteria</b>	Success, if SCLEAN completes as expected. <b>NOTE:</b> Refer to <a href="#">Section 13.9.3.1</a> for SCLEAN Manual Check steps.

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# 14 Integrated Clock Control Compliance

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This chapter covers details of ICC test cases supported by all TGL platforms across different segments.

## Intel® ICC feature support:

ICC feature support is based on a PCH used on the platform. Refer to below table for more details.

PCH Supported	ICC Feature/Configuration Supported
TGL-LP SKUs	<ul style="list-style-type: none"><li>Standard</li><li>Adaptive</li></ul>
TGL-H SKUs	<ul style="list-style-type: none"><li>Standard</li><li>Adaptive</li></ul>

## ICC Profile and parameters configuration recommendation:

- Review the FW Bringup Guide to get familiar with supported frequency and SSC configurations for above features.
- OEMs are recommended to configure ICC Boot profile and parameters for the profile via Intel® FIT > ICC tab. Make sure to choose appropriate profile and configure parameters to meet platform and HW requirements.

## CCT Tool usage:

- For manual testing, ICC SDK is located at: .../System\_Tools/ICC Tools/.

## ICC PETS test package details:

The test cases supported by platforms using Intel® Platform Enablement Test Suite (Intel® PETS) are defined as a part of Compliance\_ICC\_\*.xml. Select the respective ICC package since this version of PETS supports different PCHs.

- For TGL-LP SKUs, select xml file from:../TGL/./**Compliance\_ICC\_TGL-LP**
- For TGL-H SKUs, select xml file from:../TGL/./**Compliance\_ICC\_TGL\_H**

**Note:** Pets automation will available in future releases.



## 14.1 Test Coverage Summary for TGL-LP and TGL-H

Test ID	Test Case Title	Mandatory	PETS/ Manual	Applicable to PCH SKU	Network Factor
ICC_TST_01	Test default settings for Standard configuration	Yes (Only mandatory when SUT's boot profile is selected based on standard profile under FIT or by means of BIOS)	PETS /Manual using ICC SDK embedded	<ul style="list-style-type: none"><li>• TGL- LP</li><li>• TGL-H</li></ul>	LAN+WLAN; WLAN only
ICC_TST_02	Test default settings for Adaptive configuration	Yes (Only mandatory when SUT's boot profile is selected based on adaptive profile under FIT or by means of BIOS)	PETS/Manual using ICC SDK embedded	<ul style="list-style-type: none"><li>• TGL-LP</li><li>• TGL-H</li></ul>	LAN+WLAN; WLAN only
ICC_TST_04	Test Get and Set of MPHY setting	Yes	PETS/Manual using ICC SDK embedded	<ul style="list-style-type: none"><li>• TGL-LP</li><li>• TGL-H</li></ul>	LAN+WLAN; WLAN only



## 14.2 Test Cases

### 14.2.1 Test Default Settings for Standard Configuration

<b>Test ID</b>	<b>ICC_TST_01</b>
<b>Test Case Title</b>	Test default settings for Standard configuration
<b>Mandatory/Optional</b>	<p>Mandatory.</p> <p><b>Note:</b> Only for SUTs with boot profile that to "standard" profile under FIT &gt; ICC &gt; Boot Profile or by means of BIOS</p> <p><b>Note:</b> For FIT Tool, Check parameter under FIT  Integrated Clock Controller   Boot Profile selection. if Boot profile selection is based on Standard profile, then this test is mandatory otherwise it can be skipped.</p> <p><b>Note:</b> For BIOS, Check parameter using the request to HECI: <a href="#">ICC_GET_PROFILE_REQ</a> if Boot profile selection is based on Standard profile, then this test is mandatory otherwise it can be skipped.</p>
<b>Description</b>	Verify if the current ICC registers setting in the SUT are set correctly based on standard configuration
<b>Objective</b>	Ensure that critical ICC register values are configured correctly for standard configuration.
<b>Procedure</b>	<p>Get BCLK PLL Settings:</p> <ul style="list-style-type: none"> <li>API: <code>ICC_GET_CLOCK_SETTINGSEX</code></li> <li>library method: <code>EXTERNAL_API UINT32IccLibGetCurrentClockSettingsWrapper(const ICC_HECI_CLOCK_ID clockId, ICC_GET_CLOCK_SETTINGSEX * const clockSettings);</code></li> </ul> <p>An error should be returned in case the test has failed</p>
<b>Test Pass/Fail Criteria</b>	<p>Pass if the critical ICC registers values read are set correctly based on the standard configuration.</p> <p>Frequency= 400 MHZ</p> <p>SSC = 0.5</p> <p><b>Note:</b> For FIT, Check parameter under Flash Image Tool  Integrated Clock Controller   Boot profile selection. If Boot profile is not based on standard profile then this test is expected to fail.</p> <p><b>Note:</b> For BIOS, check parameter using the request to HECI : <a href="#">ICC_GET_PROFILE_REQ</a> if Boot profile is not based on standard profile then this test is expected to fail.</p>

## 14.2.2 Test Default Settings for Adaptive Configuration

Test ID	ICC_TST_02
Test Case Title	Test default settings for Adaptive configuration
Mandatory/Optional	<p>Mandatory</p> <p><b>Note:</b> Only for SUTs with boot profile set to "Adaptive" profile under FIT &gt; ICC &gt; Boot Profile or by means of BIOS.</p> <p><b>Note:</b> For FIT Tool, Check parameter under FIT   Integrated Clock Controller   Boot profile selection. if boot profile selection is based on Adaptive profile, This test is mandatory else the user can skip to execute it.</p> <p><b>Note:</b> For BIOS check parameter using the request to HECI : <a href="#">ICC_GET_PROFILE_REQ</a> if Boot profile selection is based on Adaptive profile, then this test is mandatory otherwise it can be skipped.</p>
Description	Verify if the current ICC registers setting in the SUT are set correctly based on Adaptive configuration
Objective	Ensure that critical ICC register values match defaults for Adaptive configuration
Procedure	<p>Get BCLK PLL Settings:</p> <ul style="list-style-type: none"> <li>API: <code>_ICC_SET_CLOCK_SETTINGSEX</code></li> <li>Library method: <code>EXTERNAL_API UINT32IccLibGetCurrentClockSettingsWrapper(const ICC_HECI_CLOCK_ID clockId, ICC_GET_CLOCK_SETTINGSEX * const clockSettings);</code></li> </ul> <p>An error should be returned in case the test has failed</p> <p>Set the BCLK PLL settings:</p> <ul style="list-style-type: none"> <li>API: <code>_ICC_SET_CLOCK_SETTINGSEX</code></li> <li>Library method: <code>EXTERNAL_API UINT32IccLibSetCurrentClockSettingsWrapper(const ICC_HECI_CLOCK_ID clockId, ICC_SET_CLOCK_SETTINGSEX * clockSettings);</code></li> </ul> <p>An error should be returned in case the test has failed</p>
Test Pass/Fail Criteria	<p>Pass if the critical ICC registers values read are set correctly based on the Adaptive configuration.</p> <p><b>Note:</b> For FIT, Check parameter under Flash Image Tool   Integrated Clock Controller   Boot profile selection. If Boot profile is not based on Adaptive profile, then this test is expected to fail.</p> <p><b>Note:</b> For BIOS check parameter using the request to HECI : <a href="#">ICC_GET_PROFILE_REQ</a> if Boot profile selection is based on Adaptive profile, then this test is mandatory otherwise it can be skipped.</p> <p><b>Note:</b> Default frequency and SSC supported for Adaptive is 97.5MHz with 0.50%. Supported Min.-Max. frequency range is [97.5- 100 MHz]. This test checks default configuration for Adaptive clocking. Test may fail if customer change SSC or frequency from default value; however make sure to check if settings are within the expected range supported for Adaptive clocking.</p>

## 14.2.3 GET and SET MPHY Settings

Test ID	ICC_TST_04
Test Case Title	Get and Set of MPHY setting
Mandatory/Optional	Mandatory, This is informative test.
Description	<p>This test output consists of high level detail like CRC count into a bin file, Version, and product detail of chipset initialization settings.</p> <p>This test applies to a new version of chipset.</p> <p>User to manually verify data is correct or not.</p>





<b>Test ID</b>	<b>ICC_TST_04</b>
<b>Objective</b>	<p>Verify if correct version of chipset initialization settings are applied or not. In case issue is seen, detail like CRC count, Version and product detail can be used for debug purpose.</p> <p>Apply a new version of chipset initialization settings</p>
<b>Procedure</b>	<p>GET MPHY Version:  API: _GET_MPHY_VERSION  library method: EXTERNAL_API UINT32  IccLibGetMphyVersion(GET_MPHY_VERSION *survTable);</p> <p>GET MPHY table:  library method: EXTERNAL_API UINT32  IccLibGetMphySettingsWrapper(UINT32 length, UINT32 offset, UINT8 *buffer,UINT32 *bytesRead);</p> <p>Set MPHY table:  library method: EXTERNAL_API UINT32  IccLibSetMphySettingsWrapper(char *mphyFileName);</p> <p><b>Note:</b> Retrieving Chipset Initialization file and information can be blocked by some restrictions enforced with End-of-Post being issued. Tester may require to disable End-of-Post message from BIOS menu for the test to successfully pass.</p> <p><b>Note:</b> This test currently displays the command result only.</p>
<b>Test Pass/Fail Criteria</b>	This is informative test and displays details like CRC count, Version, and product detail. User to manually confirm if data looks correct or not.

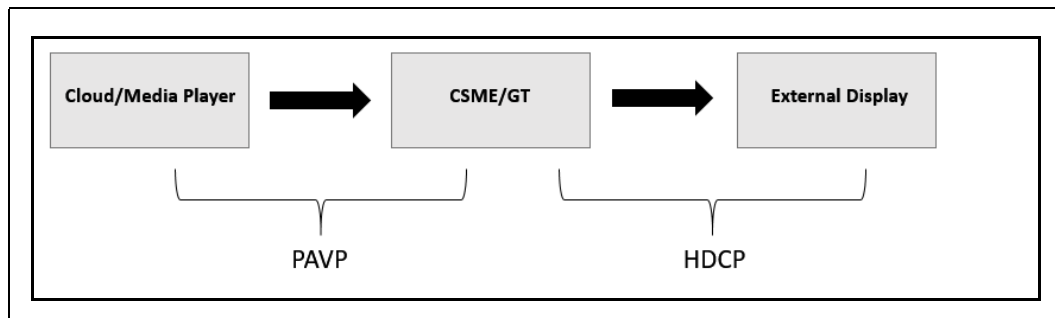
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# 15 Protected Media Playback

## 15.1 Overview

Protected Media Playback is supported by Intel® CSME Firmware. Intel® ME employs the following content protection mechanism to safe guard premium content from copy:

- Intel® Protected Audio Video Path
- High-bandwidth Digital Content Protection



The Protected Audio/Video Path (PAVP) is an Intel-specific collection of content protection features in the Intel “Gen” graphics products. The purpose of PAVP is to support premium content video playback including Blu-ray discs and provide a protected path from the media player application to the GPU HW. PAVP ensures that computers supporting hardware-based decode acceleration are properly utilized in order to deliver smooth playback.

Protection of the data, as it leaves the GPU and goes to an external display is typically done using industry standard HDCP.

## 15.2 Scope

This chapter describes a validation strategy for protected content Protected Media Playback. This chapter is intended for validation purposes. The objective is to provide validation professionals with additional insight into Media Playback protection offered by Intel® CSME by highlighting validation considerations. This chapter is not a technology overview. The reader is expected to be familiar with Protected Media Playback or Content Protection and to use this document as a validation supplement to develop his own validation plan.



## 15.3 Pre-requisite

This Protected Media Playback evaluation plan documented in this chapter requires the following components and tools for execution.

- Intel® Flash Image Tool (fit.exe)
- Intel® Flash Programming Tool (Intel® FPT) is available in Windows\* 32-bit (fptw.exe), Windows\* 64-bit (fptw64.exe) operating systems, EFI 32-bit and EFI 64-bit.

## 15.4 Test Environment Setup

The System under Test (SUT) is to be configured in manual configuration mode a with wired LAN or wireless LAN dynamic IP address. The DHCP server connecting the SUT and Management Console (MC) must be configured to ensure that the wired LAN and wireless LAN addresses reside on separate subnets. The MC could be a laptop or desktop system running a version of Windows\* supported by PETS. The network configuration consists of a hub or switch, network cables, and a wireless Access Point (AP).

## 15.5 Media Playback Test Coverage Summary

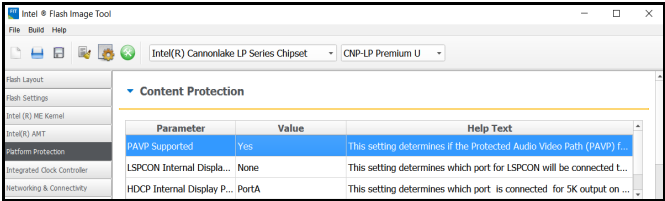
Platform, Operating System Support, How? Column describes the test methodology.


OS Support: W = Microsoft\* Windows, WI = Microsoft\* Windows\* InstantGo\*, AOS = Android\* OS

How?: A = Fully Automated using Intel® PETS, I = Interactive using Intel® PETS and M = Manual.

Test ID	Test Case Title	PETS/Manual	OS Supported	Form Factor
Media_001	Verify default configuration settings for Protected Audio Video Path [PAVP] in Firmware Image Tool [FIT]	Manual	W WI	DT/MB/HE-DT
Media_004	Verify PAVP Enabled in BIOS <i>(Only, if the SUT BIOS menu displays PAVP Mode)</i>	Manual	W WI	DT/MB/HE-DT



Test ID	Media_001
Test Case Title	Verify default configuration settings for Protected Audio Video Path [PAVP] in Firmware Image Tool [FIT]
Platform	TGL
Mandatory/Optional	Mandatory
Mobile Only	No
Firmware SKU	Consumer/Corporate
Description	Intel® CSME initiates PAVP secure session in firmware for key exchange and encryption for Content from Media player or cloud. PAVP can be enabled or disabled using FIT Tool.  In this test, user verify the PAVP is enabled in the SUT SPI image using FIT.
Objective	Verify, if the PAVP control in Intel® FIT are set correctly
Procedure	<ol style="list-style-type: none"> <li>1. Open customer image in FIT tool.</li> <li>2. Got to <b>Platform Protection</b> tab.</li> <li>3. Verify and ensure, if the 'PAVP Supported Parameter' is set to 'Yes'.</li> </ol> 
Test Pass/Fail Criteria	Test passes, if FIT PAVP parameter is set to 'Yes', when SPI image is opened in FIT.

Test ID	Media_004
Test Case Title	Verify PAVP Enabled in BIOS
Platform	TGL
Mandatory/Optional	Mandatory (Only, if the SUT BIOS menu displays PAVP Mode)
Mobile Only	No
Firmware SKU	Consumer/Corporate
Description	PAVP can be configured in the BIOS. In this test, user verifies what the PAVP mode is enabled in SUT BIOS.
Objective	Verify PAVP configuration in BIOS
Procedure	<ol style="list-style-type: none"> <li>1. Boot system to BIOS menu.</li> <li>2. Navigate to BIOS menu, where user have PAVP Option [Example: In Intel® BIOS, goto - <i>Intel Advance Menu &gt; System Agent (SA) Configuration &gt; Graphics Configuration &gt; PAVP Enable</i>].</li> <li>3. Verify the PAVP mode setup.</li> </ol> 
Test Pass/Fail Criteria	Test passes, if user PAVP is enabled in SUT BIOS.

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# 16 Intel® Dynamic Application Loader (Intel® DAL)

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## 16.1 Introduction

Intel® Dynamic Application Loader (Intel® DAL) is an Intel® CSME infrastructure for applications, such as Intel® Identity Protection Technology (Intel® IPT).

The following table documents compliance tests to verify Intel® Dynamic Application Loader (Intel® DAL) is working on the platform.

This Test plan is targeted at all OEMs.

**Note:** Intel® IPT testing is out of this compliance guide scope. Intel® IPT has a dedicated kit, which includes validation and collateral (available on VIP).

## 16.2 Test Environment

**Note:** No OEM implementation is required on the board/BIOS or EC level. Intel® CSME should be set to Enabled in FIT, when creating the firmware image.

The Management console could be a laptop or a desktop a version of Windows\* supported by Intel® Platform Enablement Test Suite. The network to use is a hub/switch and network cables.

The Intel® DAL tests should not be conducted in Windows\* Server 2008 as Intel® DAL currently does not supports this OS.

**Note:** DAL Applet needs to be signed with RSA 3K due to CSE signing method upgrade.

### 16.2.1 Tools for Testing

**Intel® Platform Enablement Test Suite**—Latest version of the tool from the Intel® CSME Compliance kit release. Refer to the Intel® Platform Enablement Test Suite (Intel® PETS) user guide available in the Intel® Compliance kit for exact instructions on how to load and setup the Intel® Platform Enablement Test Suite software.

Package DAL.xml should be loaded to Intel® PETS in order to compete the tests in this section

### 16.2.2 Verifying If Required Software is Installed on Host

The following software components need to be available in the platform OS:

**Intel® MEI Driver:**

This is the interface used for communication between the host OS components and the Intel® CSME components (included in the general Intel® CSME installer kit).



**Intel® Dynamic Application Loader (Intel® DAL) host software components:**  
Exposes an API that allows communication between the host client and the application (included in the general Intel® CSME installer kit).

## 16.3 Test Coverage Summary and Details

Test ID	Test Case Title	PETS/Manual	Form Factor
DAL_001	Intel® DAL applications cleanup	PETS	DT/MB/AIO/WS-Server
DAL_002	Intel® DAL test application installation and load	PETS	DT/MB/AIO/WS-Server
DAL_003	Intel® DAL communication channel exercise	PETS	DT/MB/AIO/WS-Server

**Note:** DT = Desktop, MB = Mobile, AIO = All In One, WS-Server = WS-Server

**Note:** OS test runs on Microsoft\* Windows\* 7/8.x/10.

Test ID	DAL_001
Test Case Title	Intel® DAL applications cleanup
Mandatory/Optional	Mandatory for those, who implement Intel® IPT
Firmware SKU	All Consumer and Corporate SKUs (Desktop, Mobile, and Workstation)
Description	Intel® DAL applications cleanup mechanism test
Objective	To test that the Intel® Dynamic Application Loader (Intel® DAL) clean-up mechanism works properly, and no application is currently running in Intel® DAL
Procedure	<p>Start test DAL_001 in the Intel® Platform Enablement Test Suite from management console.</p> <p><b>Intel® Platform Enablement Test Suite will perform the following steps:</b></p> <ol style="list-style-type: none"> <li>1. Confirm the Intel® Dynamic Application Loader (Intel® DAL) is enabled in firmware.</li> <li>2. Confirm needed Host software components are available (Intel® MEI driver and Intel® Dynamic Application Loader (Intel® DAL) host software).</li> <li>3. Perform cleanup of all Intel® DAL applications.</li> </ol>
Test Pass/Fail Criteria	All steps return the value "Passed".

Test ID	DAL_002
Test Case Title	Intel® DAL test application installation and load
Mandatory/Optional	Mandatory for those who implement Intel® IPT
Firmware SKU	All Consumer and Corporate SKUs (Desktop, Mobile, and Workstation)
Description	Intel® DAL test application will be installed and loaded, verifying basic functionality of Intel® DAL applications execution capability.

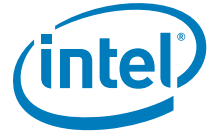


Test ID	DAL_002
Objective	To test that the Intel® Dynamic Application Loader (Intel® DAL) basic functionality works properly.
Procedure	<p>Start test DAL_002 in the Intel® Platform Enablement Test Suite from management console.</p> <p><b>Intel® Platform Enablement Test Suite performs the following steps:</b></p> <ol style="list-style-type: none"><li>1. Confirm the Intel® Dynamic Application Loader (Intel® DAL) is enabled in firmware.</li><li>2. Confirm that the needed Host software components are available (Intel® MEI driver and Intel® Dynamic Application Loader (Intel® DAL) host software).</li><li>3. Confirm test application can be installed and loaded to Intel® Dynamic Application Loader.</li><li>4. Unload the test application.</li></ol>
Test Pass/Fail Criteria	All steps return the value "Passed".

Test ID	DAL_003
Test Case Title	Intel® DAL communication channel exercise
Mandatory/Optional	Mandatory for those who implement Intel® IPT
Firmware SKU	All Consumer and Corporate SKUs (Desktop, Mobile, and Workstation)
Description	Intel® DAL test application is installed and loaded, followed by a communication channel exercise between application and host side application.
Objective	To test that the Intel® Dynamic Application Loader (Intel® DAL) application can communicate successfully with a host application.
Procedure	<p>Start test DAL_003 in the Intel® Platform Enablement Test Suite from management console.</p> <p><b>Intel® Platform Enablement Test Suite will perform the following steps:</b></p> <ol style="list-style-type: none"><li>1. Confirm the Intel® Dynamic Application Loader (Intel® DAL) is enabled in firmware.</li><li>2. Confirm needed Host software components are available (Intel® MEI driver and Intel® Dynamic Application Loader (Intel® DAL) host software).</li><li>3. Exercise basic communication channel between test application and host to verify connectivity flow</li><li>4. Unload the test application.</li></ol>
Test Pass/Fail Criteria	All steps return the value "Passed".

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# 17 Intel® Platform Trust Technology (Intel® PTT) Compliance

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Intel® Platform Trust Technology (Intel® PTT) is the Intel implementation of TCG TPM 2.0 standard in firmware. For more information about Intel® PTT integration with BIOS, refer BIOS Writers Guide and Intel® PTT Overview documentation.

The purpose of this section is to describe the tests required to verify PTT is functional, main PTT end to end use cases are working and platform meets Windows\* 10 requirements for TPM 2.0 support.

The scope of this section is end to end testing and is not intended to provide TPM command level testing.

**Note:** Intel Boot Guard testing with Intel® PTT is out of scope of this chapter and should be done as part of Intel Boot Guard testing.

## Test Environment for PTT Compliance Section:

- Tiger Lake Platform with Intel® PTT enabled.
- Windows\* 10 Professional or Enterprise installed in UEFI mode.
- Intel® CSME firmware and Intel® PTT enabled.

## Tools for Testing:

- Intel® Platform Enablement Test Suite (Intel® PETS)—Latest version of the tool from the Intel® CSME Compliance kit release. Refer to the Intel® Platform Enablement Test Suite (Intel® PETS) user guide available in the Intel Compliance kit for exact instructions on how to load and setup the Intel® Platform Enablement Test Suite (Intel® PETS) software.
- Windows\* 10 HLK Testing Environment.
- manage-bde.exe (Windows\* command line tool for BitLocker Driver Configuration).
- bdehdcfg.exe (Windows\* command line tool for BitLocker Drive Encryption).
- makecert.exe (command line tool, part of Windows\* 10 SDK).
- pvk2pfx.exe (command line tool, part Windows\* 10 SDK).
- CertUtil.exe (Windows\* 10 Command line tool).



## 17.1 Test Coverage Summary

Test ID	Test Case Title	PETS/Manual
PTT_001	CRB Interface Communication Test	PETS
PTT_002	Intel® PTT Windows* 10 Basic Functionality	PETS
PTT_003	TPM Clear and Physical Presence	PETS
PTT_004	Windows* 10 BitLocker Integration	PETS
PTT_005	Windows* 10 BitLocker TPM Protection	PETS
PTT_006	Windows* 10 Virtual Smart Card (VSC) Tests	PETS
PTT_007	Microsoft* Windows HLK TPM Tests	Manual <b>Note:</b> This test is not required for Intel® CSME compliance but may be required for Microsoft* logo certification. For any questions or support issues, when running this test, refer to Microsoft* support.
PTT_008	Intel® PTT Enable/Disable from BIOS	Manual
PTT_009	Power Transition Testing with Intel® PTT Enabled	PETS
PTT_010	Dictionary Attack Lockout After Coin Battery Removal with EOM Commit	Manual

## 17.2 Verification of BIOS and Intel® PTT Communication Over CRB Interface



Test ID	PTT_001
Test Case Title	CRB Interface Communication Test
Mandatory/Optional	Mandatory <b>Note:</b> This test uses CRB access and therefore needs to run with disabled driver to ensure elimination of false failures.
Description	The test confirms that BIOS correctly implements the CRB protocol for communication with Intel® PTT
Objective	Verify BIOS is able to successfully send commands to Intel® PTT
Procedure	<ol style="list-style-type: none"> <li>1. Confirm Intel® PTT is enabled in the SPI image.</li> <li>2. Disable the Microsoft* TPM driver: From an Elevated Command Window issue the following command: <code>reg add HKLM\SYSTEM\CurrentControlSet\Services\TPM /f /v ImagePath /t REG_EXPAND_SZ /d \SystemRoot\system32\drivers\tpm.sys</code></li> <li>3. Reboot the system</li> <li>4. Relinquish locality 0: Write 1 to TPM_LOC_CTRL_0.Relinquish (0xfed40008, bit 1).</li> <li>5. Request locality 0: Write 1 to TPM_LOC_CTRL_0.RequestAccess (0xfed40008, bit 0).</li> <li>6. Verify TPM_LOC_STATE_x.locAssigned field (0xfed40000, bit 1) is set to 1 and that TPM_LOC_STATE_x.activeLocality field (0xfed40000, bits 2-4) is set to 000.</li> <li>7. Write 1 to TPM_CRB_CTRL_REQ_0.cmdReady (0xfed40040, bit 0).</li> <li>8. Poll TPM_CRB_CTRL_REQ_0.cmdReady every 5 ms for 500 ms, until it is 0.</li> <li>9. Verify TPM_CRB_CTRL_STS_0.tpmIdle (0xfed40044, bit 1) is 0.</li> <li>10. Write a TPM command, such as TPM2_SelfTest to TPM_CRB_DATA_BUFFER register (0xfed4_0080).</li> <li>11. Write "1" to the TPM_CRB_CTRL_START register (0xFED4_004C).</li> <li>12. Poll the TPM_CRB_CTRL_START register (0xfed4_004C), until its value becomes "0".</li> <li>13. Write 1 to TPM_CRB_CTRL_REQ_0.goIdle (0xfed40040, bit 1).</li> <li>14. Poll TPM_CRB_CTRL_REQ_0.goIdle for 500ms until it is 0.</li> <li>15. Relinquish locality 0: Write 1 to TPM_LOC_CTRL_0.Relinquish (0xfed40008, bit 1).</li> <li>16. Verify TPM_LOC_STATE_x.locAssigned field (0xfed40000, bit 1) is set to 0 and TPM_LOC_STATE_x.activeLocality field (0xfed40000, bits 2-4) is set to 000.</li> <li>17. Request locality 0: Write 1 to TPM_LOC_CTRL_0.RequestAccess (0xfed40008, bit 0).</li> <li>18. Re-enable the Microsoft* TPM driver: From an Elevated Command Window issue the following command: <code>reg add HKLM\SYSTEM\CurrentControlSet\Services\TPM /f /v ImagePath /t REG_EXPAND_SZ /d \SystemRoot\system32\drivers\tpm.sys</code> Reboot the system</li> </ol> <p><b>Note:</b> For detailed information on how to send a TPM command, refer to the PC client specific platform TPM profile for TPM 2.0.</p>
Test Pass/Fail Criteria	<p>If TPM_CRB_CTRL_START register returns 0x00 after the duration listed in Table 15 of the TCG specification for the test command sent and before the listed timeout, the TPM command is received by PTT through HCI, the test passes, else fails. Test fails also, if a timeout occurs at any other stage.</p> <p><b>Note:</b> HCI reference code provides serial output status of whether or not TPM command is received by PTT. Check PttHciReceive function for more details.</p>



## 17.3 Intel® PTT Basic Functionality Under Windows\* 10

Test ID	PTT_002
Test Case Title	Intel® PTT Basic Functionality Under Windows* 10
Mandatory/Optional	Mandatory
Description	Verify Intel® PTT has been enabled on the platform and Intel® PTT is functional on Windows* 10
Objective	Windows* can successfully communicate with Intel® PTT
Procedure	<ol style="list-style-type: none"><li>1. Boot to Windows* 10 UEFI installation.</li><li>2. Open Device Manager (devmgmt.msc) and verify a "Trusted Platform Module 2.0" device exists in "Security Devices".</li><li>3. Open Trusted Platform Module (TPM) Management Page (tpm.msc).</li><li>4. Verify Manufacturer Name = <b>INTC</b>, TPM Specification Version = <b>2.0</b>.</li><li>5. Verify Status is "The TPM is ready for use."</li><li>6. Open an elevated command prompt with admin privileges and enter powershell (type powershell at prompt).</li><li>7. Prepare the WMI object for querying Intel® PTT information by typing: <code>\$ptt = get-wmiobject -namespace "root/cimv2/security/microsofttpm" win32_tpm</code>.</li><li>8. Check different Intel® PTT parameters by typing the following at the PS prompt:<ol style="list-style-type: none"><li>a. <code>\$ptt.IsEnabled()</code></li><li>b. <code>\$ptt.IsActivated()</code></li><li>c. <code>\$ptt.IsAutoProvisioningEnabled()</code></li><li>d. <code>\$ptt.IsOwned()</code></li><li>e. <code>\$ptt.IsReadyInformation()</code></li></ol></li></ol>
Test Pass/Fail Criteria	No "yellow bang" in device manager, Intel® PTT is the TPM device and all TPM queries return "true". <b>Note:</b> Manufacturer version matches the firmware version.



## 17.4 Trusted Platform Module (TPM) Clear and Physical Presence

<b>Test ID</b>	<b>PTT_003</b>
<b>Test Case Title</b>	TPM Clear and Physical Presence
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	TPM Clear command erases user data on the TPM. TPM Clear requires BIOS to check for physical presence to authorize the TPM Clear operation. User saves the SrkPublicKey and verify that new/old SRK keys differ after TPM Clear.
<b>Objective</b>	Verify TPM clear and take ownership flows work correctly under Windows* 10 OS and physical presence asserted.
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Save the current SrkPublicKey by performing the following actions: <ol style="list-style-type: none"> <li>Open elevated command prompt and enter PowerShell by typing "powershell" at the prompt and type:</li> <li><code>\$ptt = get-wmiobject -namespace "root/cimv2/security/microsofttpm" win32_tpm.</code></li> <li><code>\$ret = \$ptt.GetSrkPublicKeyModulus().</code></li> <li><code>\$ret.SrkPublicKeyModulus &gt; SrkPubModOld.txt.</code></li> </ol> </li> <li>Run "tpm.msc" to open TPM Management Console.</li> <li>Click 'Clear TPM...' in the Actions pane on right.</li> <li>In the pop-up window, click 'Restart' to invoke TPM Clear flow.</li> <li>Upon reboot, a physical presence authorization message may be displayed (BIOS setting dependent) requiring the user to press a key to authorize the TPM clear or abort. In CRB, F12 authorizes, ESC rejects the operation.</li> <li>Upon booting to Windows*, pop-up window shows up indicating OS is taking ownership of the TPM.</li> <li>After ownership operation completes, press OK.</li> <li>Save the new SrkPublicKey by performing the following actions: <ol style="list-style-type: none"> <li>Open elevated command prompt and enter PowerShell by typing "powershell" at the prompt and type:</li> <li><code>\$ptt = get-wmiobject -namespace "root/cimv2/security/microsofttpm" win32_tpm</code></li> <li><code>\$ret = \$ptt.GetSrkPublicKeyModulus()</code></li> <li><code>\$ret.SrkPublicKeyModulus &gt; SrkPubModNew.txt</code></li> </ol> </li> <li>Compare the old and new keys</li> </ol>
<b>Test Pass/Fail Criteria</b>	OS takes ownership of TPM, new/old keys differ



## 17.5 Windows\* 10 BitLocker Integration

Test ID	PTT_004
Test Case Title	Windows* 10 BitLocker Integration
Mandatory/Optional	Mandatory
Description	BitLocker uses Intel® PTT to store and retrieve keys securely in addition Windows* BitLocker confirms system components did not change by checking system load measurements saved to TPM. The test verifies BitLocker can be activated, BitLocker can encrypt, decrypt, and restart encryption after reboot.
Objective	Test BitLocker integration with Intel® PTT
Procedure	<ol style="list-style-type: none"><li>1. In elevated permissions command line run: "bdehdcfg.exe -driveinfo" and check system drive is configured to support BitLocker</li><li>2. Set BitLocker to use TPM for measuring boot devices in Windows* Group Policy by:<ol style="list-style-type: none"><li>a. Run "gpedit.msc" to open Group Policy Editor</li><li>b. Open "Local Computer Policy" &gt; "Computer Configuration" &gt; "Administrative Templates" &gt; "Windows Components" &gt; BitLocker Drive Encryption" &gt; "Operating System Drives"</li><li>c. On the right pane double click "Configure TPM platform profile for native UEFI firmware configuration"</li><li>d. Check the enabled radio button. Verify PCR 0, PCR2, PCR4 and PCR11 are checked in the "Options" pane.</li><li>e. Click Apply and OK.</li><li>f. Commit the group policy change by typing "gpupdate /force" in an elevated command prompt</li></ol></li></ol> <p><b>Note:</b> This action is required once per OS installation.</p> <ol style="list-style-type: none"><li>3. Set up tpm as a bitlocker protector with recovery password and turn-on BitLocker by typing the following at the command prompt<ol style="list-style-type: none"><li>a. Manage-bde -protectors -add c: -tpm</li><li>b. Manage-bde -protectors -add c: -rp 000000-000000-000000-000000-000000-000000-000000-000000</li><li>c. Manage-bde -on c:</li><li>d. Shutdown -r -t 0</li></ol></li><li>4. After OS completes reboot, verify no error messages displayed. Wait for "Encryption in Progress" notification or type "manage-bde -status" to check on encryption status</li><li>5. After encryption reaches 10%, restart system, and verify encryption continues without error message after reboot completes.</li><li>6. Turn off BitLocker by typing "manage-bde -off c:" at the command line, decryption process should start</li><li>7. After decryption process ends, reboot and verify system boots into OS without error message. BitLocker should be off</li></ol>
Test Pass/Fail Criteria	All system boots complete successfully and OS loads



## 17.6 BitLocker TPM Protection

<b>Test ID</b>	<b>PTT_005</b>
<b>Test Case Title</b>	BitLocker TPM Protection
<b>Mandatory/Optional</b>	Optional
<b>Description</b>	When BitLocker is set to use TPM protection, BitLocker enters recovery mode, if any protected component changed during boot. By disabling Intel® PTT, check BitLocker is indeed using TPM as key protector.
<b>Objective</b>	Verify BitLocker is using Intel® PTT as a key protector
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Encrypt the OS drive using BitLocker with TPM protection (follow instructions in PTT_004 steps 1 through 5, and wait till drive encryption reaches 10%).</li> <li>2. Run manage-bde -status and verify drive is "protected".</li> <li>3. Create a measured boot failure in order to trigger Bitlocker Recovery. <ol style="list-style-type: none"> <li>a. In BIOS, choose disable Intel® PTT or send a TPM_Clear command. <b>Note:</b> Clearing TPM by means of the OS disables Bitlocker and is not prompt the user for his recovery password. The TPM must be cleared by the BIOS.</li> <li>b. System should boot into BitLocker recovery screen. Provide the recovery password to continue boot.</li> <li>c. Verify boot completes successfully.</li> </ol> </li> <li>4. Disable BitLocker by typing "manage-bde -off c:" at the command line, decryption process should start.</li> <li>5. After decryption process ends, reboot and verify system boots into OS without error message. BitLocker should be off.</li> </ol>
<b>Test Pass/Fail Criteria</b>	BitLocker completes drive encryption successfully and reboots. System displays BitLocker recovery screen after choosing Disable Intel® PTT or Clear TPM in BIOS setup.



## 17.7 Virtual Smart Card Tests

Test ID	PTT_006
Test Case Title	Virtual Smart Card (VSC) Tests
Mandatory/Optional	Optional
Description	Virtual Smart Card is a new Microsoft* use case for TPMs. More information on VSC can be found on Microsoft* web site. This test verifies a VSC can be created and certificate installed, so VSC is accessible.
Objective	Intel® PTT can be used to support VSC use case
Procedure	<ol style="list-style-type: none"><li>1. Create a VSC running the following command on an elevated command line: <code>tpmvscmgr.exe create /name TPM2VSC /adminkey random /PUK default /pin default /generate</code></li><li>2. Verify that TPM2VSC smart card reader is created in "Smart card readers" in device manager.</li><li>3. Restart Windows*, and check the device is not yellow banded in device manager.</li><li>4. Create and import a self-signed certificate into the VSC.<ol style="list-style-type: none"><li>a. Ensure the following registry keys exist under [HKEY_LOCAL_MACHINE\SOFTWARE\Microsoft\Cryptography\Defaults\Provider\Microsoft Base Smart Card Crypto Provider]:<ul style="list-style-type: none"><li>— "AllowPrivateSignatureKeyImport"=DWord:00000001</li><li>— "AllowPrivateExchangeKeyImport"=DWord:00000001</li></ul></li><li>b. Open an elevated command prompt</li><li>c. Type: <code>MakeCert.exe -sky exchange -r -n "CN=TPM2VSCCert" -pe -a sha1 -len 2048 -ss My -m 36 -sv "TPM2VSCCert.pvk" "TPM2VSCCert.cer"</code></li><li>d. When requested, create a password. When asked for the password, provide the password created (Example: Using "123" as the password).</li><li>e. Convert certificate to PFX format using the following command: <code>pvk2pfx.exe -pvk "TPM2VSCCert.pvk" -pi 123 -spc "TPM2VSCCert.cer" -pfx "TPM2VSCCert.pfx" -f</code></li><li>f. Import the certificate into the smart card using the following command: <code>CertUtil.exe -p 123 -csp "Microsoft* Base Smart Card Crypto Provider" -pin 12345678 -importpfx TPM2VSCCert.pfx AT_KEYEXCHANGE</code>.</li></ol></li><li>5. Verify import was successful by examining the certificate in the VSC using the following command: <code>CertUtil.exe -scinfo -pin "12345678"</code>. Window allowing to view the certificate will pop up, click OK to close.</li><li>6. Restart the platform, and run step 5 again to verify certificate persists after reboot.</li><li>7. Remove the key from the VSC using the following commands.<ol style="list-style-type: none"><li>a. Retrieve the name of the container to use by typing: <code>CertUtil.exe -key -csp "Microsoft Base Smart Card Crypto Provider" -pin "12345678" -v -privatekey -user</code>.</li><li>b. Use the container name returned in the previous command prefixed to the "[Default Container]" and replace the text in bold: <code>CertUtil.exe -delkey -csp "Microsoft Base Smart Card Crypto Provider" -pin "12345678" -v -privatekey "TPM2VSCCert-0d6e6c94-9bd6-4640-aa-63900"</code></li></ol></li><li>8. Destroy the VSC by running: <code>TpmVscMgr.exe destroy /instance ROOT\SMARTCARDREADER\0000</code>, making sure to use the correct index of the smartcard created</li></ol>
Test Pass/Fail Criteria	VSC created successfully, certificate can be loaded and is persistent across reboot. VSC can be removed after key is deleted.

## 17.8 Windows\* Hardware Lab Kit (HLK) TPM Testing

Test ID	PTT_007
Test Case Title	Microsoft* Windows Hardware Lab Kit (HLK) TPM Testing
Mandatory/Optional	Optional





Test ID	PTT_007
Description	Windows* 10 Logo requires TPM device to pass all TPM related tests in the HLK
Objective	Ensure Intel® PTT passes all required platform HLK test for TPM device. <b>Note:</b> This test is not required for Intel® CSME compliance but may be required for Microsoft* logo certification. For any questions or support issues, when running this test, refer to Microsoft* support.
Test Pass/Fail Criteria	All HLK tests must pass. Ensure that all latest Errata filters are downloaded from the Microsoft* HLK web site. Refer to the Windows* Hardware Lab Kit Step-by-Step Guide found at the link below for detailed instructions: <a href="https://msdn.microsoft.com/en-us/library/windows/hardware/dn915002(v=vs.85).aspx">https://msdn.microsoft.com/en-us/library/windows/hardware/dn915002(v=vs.85).aspx</a>

## 17.9 Intel® Platform Trust Technology (Intel® PTT) Disable/Enable from BIOS

Test ID	PTT_008
Test Case Title	Intel® PTT Disable/Enable from BIOS
Mandatory/Optional	Optional
Description	BIOS may implement option to disable/enable Intel® PTT, or switch between Intel® PTT and a discrete TPM 1.2
Objective	Ensure BIOS can enable and disable Intel® PTT successfully and that BIOS clears the TPM during disable
Procedure	Can be run on Windows* 10 or Windows* 8.1. 1. Boot to Windows*, verify PTT_002 passing. 2. Reboot, enter BIOS and disable Intel® PTT through BIOS. 3. Boot to Windows*, enter TPM Management Console (tpm.msc) and verify that either TPM is not available, or if TPM is available it is not Intel® PTT. 4. Reboot, enter BIOS and enable Intel® PTT through BIOS. 5. Boot to Windows*, verify PTT_002 passing. 6. Intel® PTT enable/disable interface in BIOS is dependent on implementation and therefore not described.
Test Pass/Fail Criteria	When Intel® PTT is disabled; Intel® PTT does not show up in TPM management console. (It is possible for dTPM to show up pending on the platform design).



## 17.10 Intel® Platform Trust Technology (Intel® PTT) and Power Flows

Test ID	PTT_009
Test Case Title	Power Flow Testing
Mandatory/Optional	Mandatory
Description	System with Intel® PTT enabled must pass all platform power flow testing. Intel® PTT must also be able to support all power flows, when BitLocker is enabled and using Intel® PTT as a protector
Objective	Verify Intel® PTT does not interfere with system power operations
Procedure	<ol style="list-style-type: none"><li>1. Perform all platform power flow tests with Intel® PTT enabled.</li><li>2. Encrypt the OS drive using BitLocker with TPM protection (follow instructions in PTT_004 steps 1 through 5, and wait till drive encryption reaches 10%).</li><li>3. Perform the following power transitions during encryption phase and after encryption has reached 10%:<ol style="list-style-type: none"><li>a. OS Restart</li><li>b. OS Shutdown/Power up</li><li>c. Hibernation/Resume</li><li>d. Cold Reset (boot to internal EDK shell and type mm cf9 e -io)</li><li>e. G3 (complete power off)</li><li>f. Connected Standby (Windows* 8 CS)</li></ol></li></ol>
Test Pass/Fail Criteria	All power flow tests pass, BitLocker does not enter into recovery mode.

## 17.11 Dictionary Attack Lockout After Coin Battery Removal with EOM Commit

Test ID	PTT_010
Test Case Title	Dictionary Attack Lockout Mechanism with coin battery removal
Mandatory/Optional	Optional for systems that do not have RPMC enabled in the image. <b>Note:</b> This test is not relevant to platforms that do not include a coin battery.
Description	<p>Intel® PTT keeps monotonic counters for Dictionary Attack (DA) under RTC power well. When RTC power is lost, Intel® PTT will enter lockout period to avoid Dictionary Attack for 2 hours. This is only after the coin battery has been removed 10 times and after EOM. Before that, Intel® PTT will not enter the lockout period of 2 hours.</p> <p><b>Note:</b> During the 2 hour lockout period, no other Intel® PTT tests can be executed; even if correct credentials are provided. Execution of this test does not impact other non-Intel® PTT related testing.</p> <p><b>Note:</b> This test can be run only once on a specific part. After this test is run, all FPF bits related to the feature will be blown. With such parts, test consistently enters dictionary attack scenario after every RTC clear operation.</p>



Test ID	PTT_010
Objective	Allows OEM to validate the dictionary attack scenario after first coin battery removal, causing the counters to be reset.
Procedure	<ol style="list-style-type: none"> <li>1. System must be after the EOM procedure, as DA lockout will not occur during manufacturing mode.</li> <li>2. Set up a VSC with certificate (Instructions can be found in test PTT_006 steps 1 through 6).</li> <li>3. Shutdown system, and perform RTC clear operation by removing all power and RTC battery from the board and close the RTC jumper. Repeat this procedure 11 times.</li> <li>4. Return RTC battery and power, boot system to Windows* 10.</li> <li>5. Try to view the certificate in VSC by running: CertUtil.exe -scinfo -pin "12345678".</li> <li>6. The command should fail due to Dictionary Attack lockout.</li> <li>7. Wait 2 hours for lockout to pass, and try again, it should be possible to access the certificate.</li> <li>8. Remove the certificate and VSC (Instruction can be found in test PTT_006 steps 8 and 9).</li> </ol> <p><b>Note:</b> At step#3, the Intel® PTT is expected to enter a lockout period to avoid Dictionary Attack for 2 hours. This period cannot be adjusted.</p> <p><b>Warning:</b> This flow is irreversible, the part is permanently fused causing every RTC clear to cause a 2 hour TPM lockout.</p>
Test Pass/Fail Criteria	<p>Intel® PTT will not allow access to user data (VSC) during lockout period post coin battery removal.</p> <p><b>Note:</b> In this test Field Programmable Fuses (FPF) is blown on every battery removal and there is no recovery for it. Only select few processors to be used for this test and track them.</p>

§ §



# 18 Intel® Virtualization Technology (Intel® VT)

Throughout this chapter, the Intel® VT covers both Intel® VT-x and Intel® VT-d, unless otherwise specified.

**Note:** Intel® VT-x refers to Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64, and Intel® Architecture (Intel® VT-x).

**Note:** Intel® VT-d refers to Intel® Virtualization Technology (Intel® VT) for Directed I/O.

## 18.1 Introduction

### 18.1.1 Purpose and Scope

The purpose of this document is to provide OEMs guidance on the steps necessary to successfully validate the Intel® Virtualization Technology (Intel® VT) with Virtualization and Intel® VT-d enabled BIOS on Intel client (desktop and mobile) platforms. This document defines the purpose and value of each validation aspect in the validation process.

The intent of this document is to outline the ideal validation sequence for Intel® VT in this platform and provide an overview of the collateral that is available to provide OEMs the framework to define their own validation strategy for Intel® VT.

This document is not a technology overview and does not supplant the existing Intel® VT collateral (refer [Section 1.6](#)). The readers are expected to be familiar with Intel® VT-x and Intel® VT-d and to use this document as a validation supplement to develop their own Intel® VT validation plan.

### 18.1.2 Platforms Applicable

This validation guide is applicable to the following Client platforms and their corresponding chipsets:

**Table 18-1. Applicable Platforms**

Platform Name
8 <sup>th</sup> Generation Intel® Core™ and Intel® Core™ M Processors Platforms
Tiger Lake Platforms

### 18.1.3 Terminology

**Table 18-2. Terminology (Sheet 1 of 2)**

Term	Description
DMA	Direct Memory Access
GPA	Guest Physical Address

**Table 18-2. Terminology (Sheet 2 of 2)**

Term	Description
HPA	Host Physical Address
HVM	Hardware Virtual Machine (Virtual Machine using Intel® VT)
MMIO	Memory Mapped I/O Address Space
OS	Operating System
TXT	Trusted Execution Technology
VM	Virtual Machine
VMM	Virtual Machine Monitor

### 18.1.4 Prerequisites

**Table 18-3. Virtualization Testing Prerequisites**

Prerequisite Checklist	Location
Client VT Info Tool	# 551893
Fedora Live USB Creator (Optional)	Open Source
OpenSUSE	Open Source

## 18.2 Intel® Virtualization Technology (Intel® VT) Test Plan and Details

**Table 18-4. Intel® Virtualization Technology (Intel® VT) Test Overview**

ID	Test Case Description	Tool/ Manual	Mandatory /Optional	Result
<b>EFI Shell Environment Tests</b>				
VT_TC01	Intel® VT Capable and Enabled as measured by Passing ALL Test Assertions	Client VT Info Tool	Mandatory	Pass
<b>Windows* Environment Tests</b>				
VT_TC02A	Verify Intel® VT-x with Microsoft* Client Hyper-V* Manager Boots on Windows* 10	Manual	Mandatory	Pass
VT_TC02B	Verify that the Virtual Machine Boots in Microsoft* Client Hyper-V* Manager	Manual	Mandatory	Pass
VT_TC02C	Verify that the Virtual Machine Correctly Resumes during Sleep and Hibernate Cycles on Host OS	Manual	Mandatory	Pass
<b>Xen*/Linux* Environment Tests</b>				
VT_TC03A	Xen* Hypervisor Boots (Xen* Environment)	Manual	Optional	Pass
VT_TC03B	Intel® VT-x and VT-d Enabled (Xen* Environment)	Manual	Optional	Pass
VT_TC03C	Intel® VT-d Functionality—Virtual Machine (VM) Boots (Xen* Environment)	Manual	Optional	Pass
VT_TC03D	Intel® VT-d Functionality—Pass Through with No VT-d Error (Xen* Environment)	Manual	Optional	Pass
VT_TC04	Intel® VT-d Functionality—IOMMU Exercise (Xen* Environment)	Manual	Optional	Pass



## 18.2.1 Intel® VT Tests in EFI Shell

### 18.2.1.1 Test Environment

A system under test is needed, which has an Intel® VT-x and Intel® VT-d capable Processor and stable BIOS with support for VT-x and VT-d technologies. Prior to tests **enable Virtualization (or VT-x)** and **Intel® VT-d** in BIOS and make sure **TXT is Disabled. Skip POSTBOOT SAI Setting** must be selected as true under Advanced Debug Settings.

**Note:** Disabling TXT is just for test purposes.

Tools for Testing:

- **Client VT Info Tool** - Get the latest version of the tool from PC Design Center VT Technology page or Document #551893.

### 18.2.1.2 Verify Processor is Intel® VT Capable and Enabled

Test ID	VT_TC01
Test Case Title	Intel® VT Capable and Enabled as measured by Passing ALL Test Assertions
Mandatory/Optional	Mandatory
Description	This test checks that the Processor has VT-x/VT-d capability, that VT-x/VT-d are enabled correctly in BIOS.
Objective	Verify Processor and BIOS is Intel® VT-x/VT-d Capable and Enabled
Procedure	<ol style="list-style-type: none"><li>1. Enable Intel® Virtualization Technology (VT-x) and Intel® VT-d in BIOS.</li></ol> <p><b>Note:</b> Make Sure TXT is disabled (for test purposes only).</p> <ol style="list-style-type: none"><li>2. Download Client VT Info Tool #551893 and save to a EFI bootable USB drive.</li><li>3. Unzip the Client VT Info Tool in the USB drive.</li><li>4. Boot to EFI Shell (Called Internal EDK Shell for Intel Reference BIOS).</li><li>5. Move to Folder with unzipped Client VT Info tool using <b>cd [folder_name]</b></li><li>6. Run ALL Test Assertions using Client VT Info tool by entering <b>vtinfo -t</b> or <b>vtinfo_vxx.xx.xx -t</b> where xx.xx.xx is the version number.</li><li>7. Record score. (Make a note of how many tests PASS and how many FAIL). Refer example outputs below in <a href="#">Section 18.2.1.2.1</a>, <a href="#">Section 18.2.1.2.2</a>, and <a href="#">Section 18.2.1.2.3</a>.</li></ol> <p><b>Note:</b> For additional information on VT Status, use <b>vtinfo -h</b> to display other command line options</p>
Test Pass/Fail Criteria	<p>Test passes, when:</p> <ol style="list-style-type: none"><li>1. Tool returns <b>VT Test Status: PASS.</b></li><li>2. <b>No Errors</b> are reported in test results.</li></ol>

#### 18.2.1.2.1 Sample Output for Client VT Info Tool Results—Passing All Tests

**This example is generated using the -t option with Client VT Info Tool:**

```
*****
VtInfo vXX.XX.XX
Built: XXX X 2014 XX:XX:XX
Intel Corporation
Copyright (c) 2014
*****
-----
VT Test Status: PASS
-----
Pass | 52
Fail | 00
Warn | 00
```



```
NA | 05
Total | 57
-----
```

**Note:** Tests, which do not apply to the system under test is not shown in results.

### 18.2.1.2.2 Sample Output for Client VT Info Tool Results—Failing Some Tests

**This example is generated using the -t option with Client VT Info Tool:**

```
*****
VtInfo vXX.XX.XX
Built: XXX X 2014 XX:XX:XX
Intel Corporation
Copyright (c) 2014
*****
```

**VT Test Status: FAIL**

```
Pass | 50
Fail | 02
Warn | 00
NA | 05
Total | 57
-----
```

**Errors:**

40) Verify 4k granularity of RMRR regions.  
 -- RMRR Base Address(0xAD800000) Limit Address(0xFFFFFFFF) is not marked as reserved in system memory map.

62) VTd Support for Large Pages (2MB and 1GB) on DEFAULT and GFX VTd Unit.  
 -- Remapping Engine 0xFED91000 Capability Register BIT56 must be set.

**Note:** Tests, which do not apply to the system under test is not shown in results.

### 18.2.1.2.3 Sample Output for Client VT Info Tool Results—Obtaining Test Result Details

**This example was generated using the -v -t options with Client VT Info Tool:**

```
...
-----
Platform Information
-----
CPUID1.EAX      0x000306D3
CPUID1.EBX      0x00100800
CPUID1.ECX      0x77FAFBFF
[6] SMX         1
[5] VMX         1
CPUID1.EDX      0xBFEBFBFF
IA32_FEATURE_CONTROL 0x000000000000FF07
[2] En VMX outside SMX 1
[1] En VMX inside SMX 1
[0] Lock bit     1
...
-----
```

**Test Assertions**

01) Check DMAR table presence.  
 Result : PASS

61) Each ACPI device number in ANDD structure must have a corresponding enumeration ID in Device Scope.  
 Result : PASS

62) VTd Support for Large Pages (2 MB and 1 GB) on DEFAULT and GFX VTd Unit.  
 Result : FAIL  
 : Remapping Engine 0xFED91000 Capability Register BIT56 must be set.

63) Graphics VTd Unit Support for SVM (Shared Virtual Memory).  
 Result : PASS

**VT Test Status: FAIL**

```
Pass | 50
```



Fail | 02  
Warn | 00  
NA | 05  
Total | 57  
-----

**Errors:**

40) Verify 4k granularity of RMRR regions.  
-- RMRR Base Address(0xAD800000) Limit Address(0xFFFFFFFF) is not marked as reserved in system memory map.

62) VTd Support for Large Pages (2MB and 1GB) on DEFAULT and GFX VTd Unit.  
-- Remapping Engine 0xFED91000 Capability Register BIT56 must be set.

**Note:** Tests, which do not apply to the system under test are not shown in results.

## 18.2.2 Intel® VT-x Tests with Microsoft\* Client Hyper-V\* on Windows\* 10

### 18.2.2.1 Test Environment

A system under test is needed which has an Intel® VT-x and Intel® VT-d capable Processor and stable BIOS with support for VT-x and VT-d technologies. Prior to tests **enable Virtualization (or VT-x)** and **Intel® VT-d** in BIOS and make sure **TXT is Disabled**

**Note:** Disabling Intel®TXT is just for test purposes.

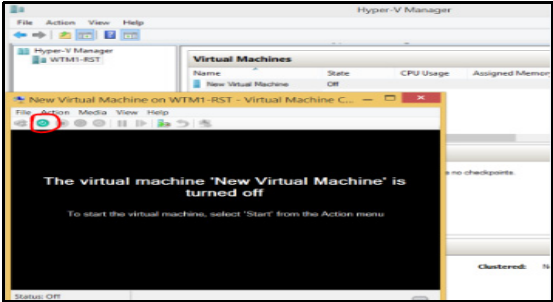
Tools for Testing:

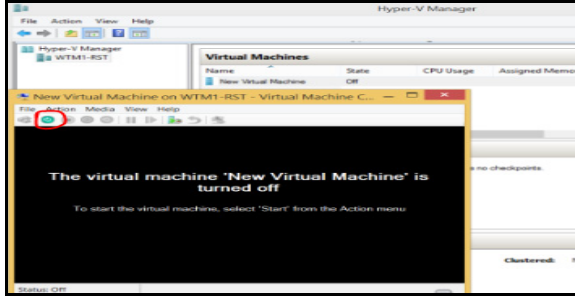
- **Microsoft\* Windows 10 or higher**

Test ID	VT_TC02A
Test Case Title	Verify Microsoft* Client Hyper-V* Manager Boots
Mandatory/ Optional	Mandatory
Description	Microsoft* Client Hyper-V* uses Intel® VT to create a Hypervisor based on Windows* 10
Objective	Verify Intel® VT-x implementation at platform level
Procedure	1. Enable Intel® Virtualization Technology (VT-x) in BIOS. 2. Boot to Windows* 10 and open Client Hyper-V* Manager. <b>Note:</b> Refer to <a href="#">Section 18.2.2.2</a> for instructions on how to enable Client Hyper-V*
Test Pass/Fail Criteria	Test passes, when Microsoft* Client Hyper-V* Manager Boots.





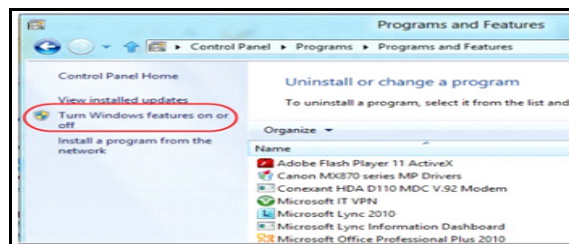
Test ID	VT_TC02B
Test Case Title	Verify Virtual Machine Boots in Microsoft* Client Hyper-V* Manager
Mandatory/Optional	Mandatory
Description	Microsoft* Client Hyper-V* uses Intel® VT to launch a virtual guest OS in Windows* 10 host OS.
Objective	Verify Intel® VT-x implementation at platform level
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® Virtualization Technology (VT-x) in BIOS.</li> <li>2. Boot to Windows* 10 and open Client Hyper-V* Manager.</li> <li>3. Open virtual machine by double clicking on it. If it is not running, user can click the start button.</li> </ol>  <p><b>Note:</b> Refer to <a href="#">Section 18.2.2.2.2</a> for instructions on how to enable Microsoft* Client Hyper-V*.</p>
Test Pass/Fail Criteria	Test passes, when Virtual Machine Guest boots within Client Hyper-V* (when Intel® VT is enabled in BIOS).

Test ID	VT_TC02C
Test Case Title	Verify Virtual Machine Correctly Resumes during Sleep and Hibernate Cycles on Host OS
Mandatory/Optional	Mandatory
Description	While performing Sleep and Hibernate cycles on the Host Machine, the Virtual Machine should correctly resume and remain stable.
Objective	Verify Intel® VT-x implementation at platform level.
Procedure	<ol style="list-style-type: none"> <li>1. Enable Intel® Virtualization Technology (VT-x) in BIOS.</li> <li>2. Boot to Windows* 10 and open Client Hyper-V* Manager.</li> <li>3. Open virtual machine by double clicking on it. If it is not running, user can click on the start button.</li> </ol>  <p><b>Note:</b> If Client Hyper-V* on a laptop is running and close the lid, the VMs that are running is placed into a saved state, and can be resumed when the machine wakes, <b>as long as lid close action is set to sleep or hibernate.</b></p> <ol style="list-style-type: none"> <li>4. While Virtual Machine is running, put the system (from Windows* 10 Host OS) to <b>Sleep mode</b> and then bring it back out of sleep. Check that Virtual machine is still alive and working. Repeat 3-5 cycles.</li> <li>5. While Virtual Machine is running, put the system (from Windows* 10 Host OS) to <b>Hibernate</b> and then bring it back out of hibernate. Check that Virtual machine is still alive and working. Repeat 3-5 cycles.</li> </ol>
Test Pass/Fail Criteria	Test passes, when: <ul style="list-style-type: none"> <li>• Virtual machine is alive and working <i>after system Sleep cycle.</i></li> <li>• Virtual machine is alive and working <i>after Hibernate cycle.</i></li> </ul>

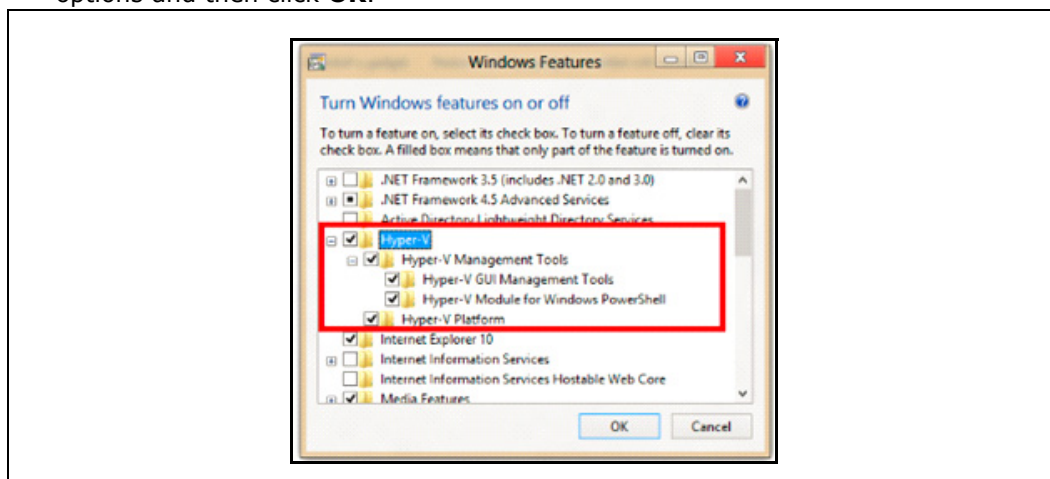
## 18.2.2.2 User Guide – Microsoft\* Client Hyper-V\* and Virtual Machine Enabling and Installation Instructions

### 18.2.2.2.1 Enabling Microsoft\* Client Hyper-V\*

1. In the Windows\* 10 Control Panel, tap or click **Programs**, and then tap or click **Programs and Features**.
2. Tap or click **Turn Windows\* features on or off**.



3. In the **Windows\* Features** dialog box, select the check-boxes for **Hyper-V\*** options and then click **OK**.



Windows\* searches for and installs the required files.

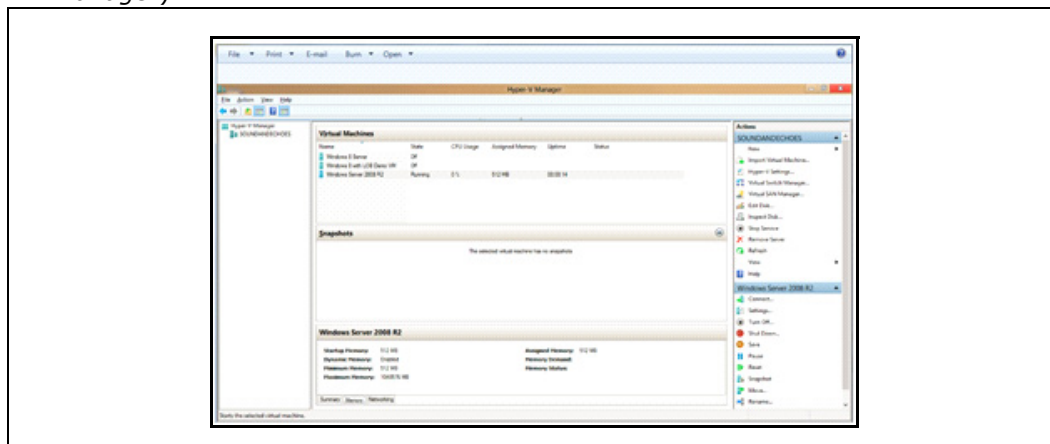
4. **Restart After Enabling or Disabling Microsoft\* Client Hyper-V\***  
Enabling Client Hyper-V\* installs Hyper-V\* Manager. Use Hyper-V\* Manager to create and manage the virtual machines.

For more information on the Hyper-V\* Manager user interface, go to <http://technet.microsoft.com/library/cc770494.aspx>.

#### 18.2.2.2.2 Creating a New Virtual Machine in Client Hyper-V\*

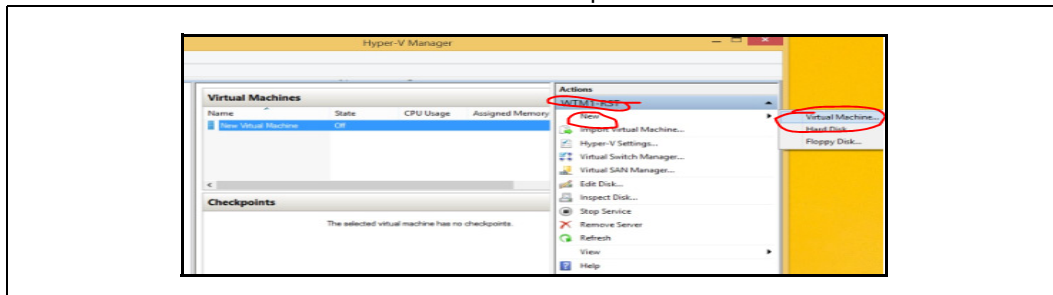
**Skip this page, if user already have a Virtual Machine in Client Hyper-V\* Manager**

1. Open Hyper-V\* Manager from Windows\* Start screen (In Windows\* 10, go to *Start screen* > *Click arrow at bottom left* > *Hyper-V Management tools* > *Hyper-V Manager*).

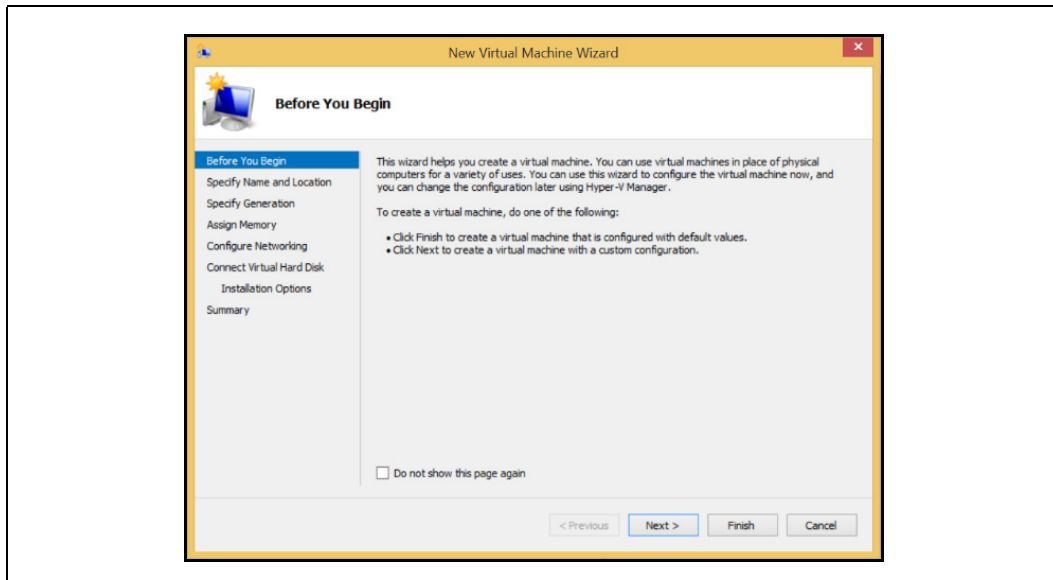


2. From the navigation pane of Hyper-V\* Manager, select the computer name.

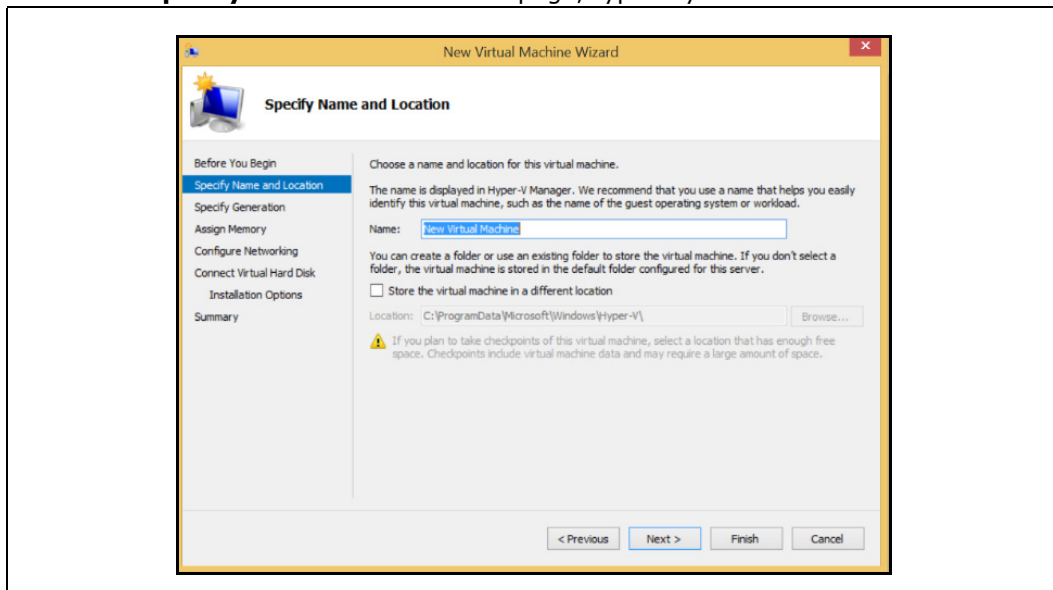
- From the **Action** pane on the right side, click **New**, and then click **Virtual Machine**. The New Virtual Machine wizard opens.



- Click **Next**.



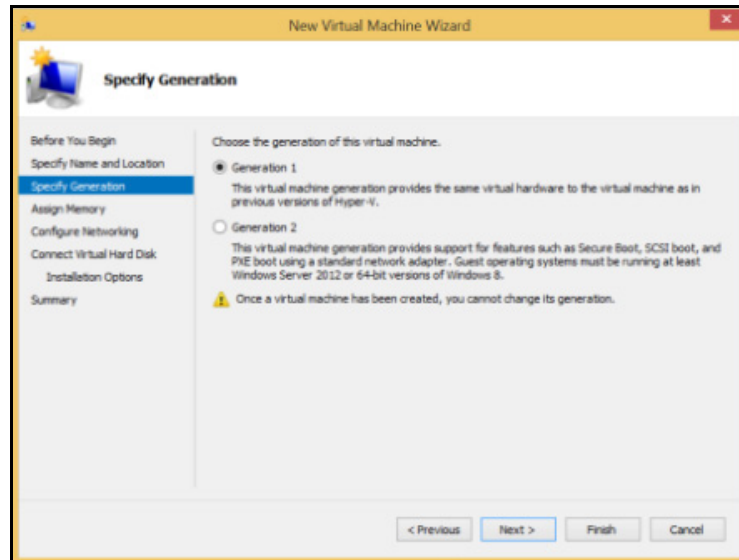
- On the **Specify Name and Location** page, type any name.



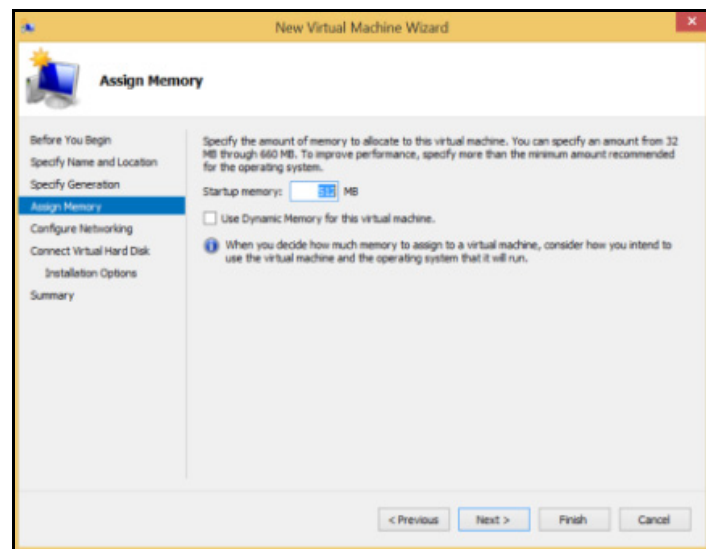


6. On the **Specify Generation** page, leave the default, Generation 1.

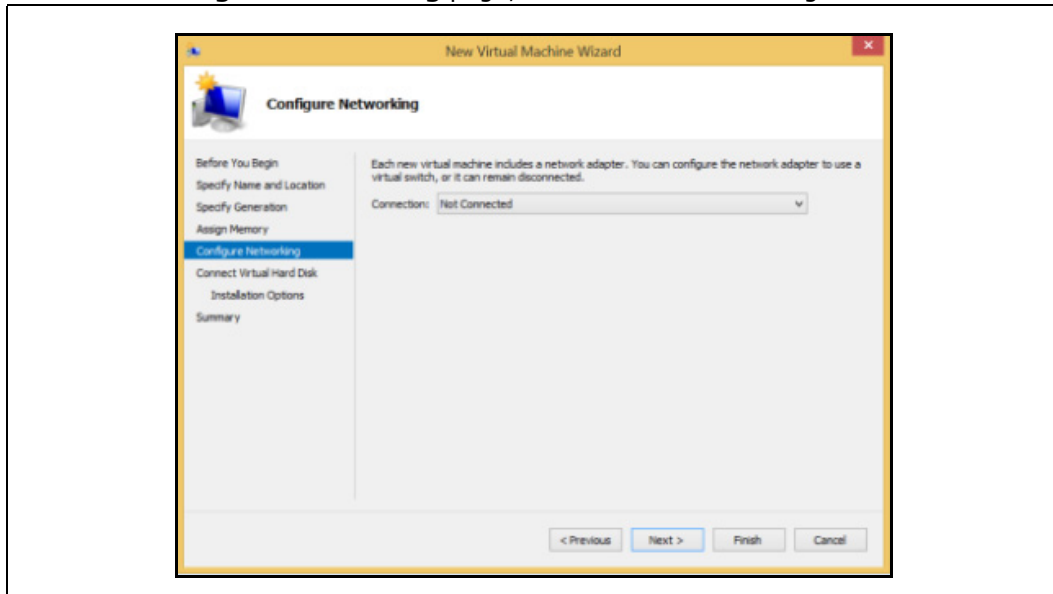
**Note:** Earlier versions of Client Hyper-V\* may not have this step.



7. On the **Assign Memory** page, specify enough memory to start the guest operating system.

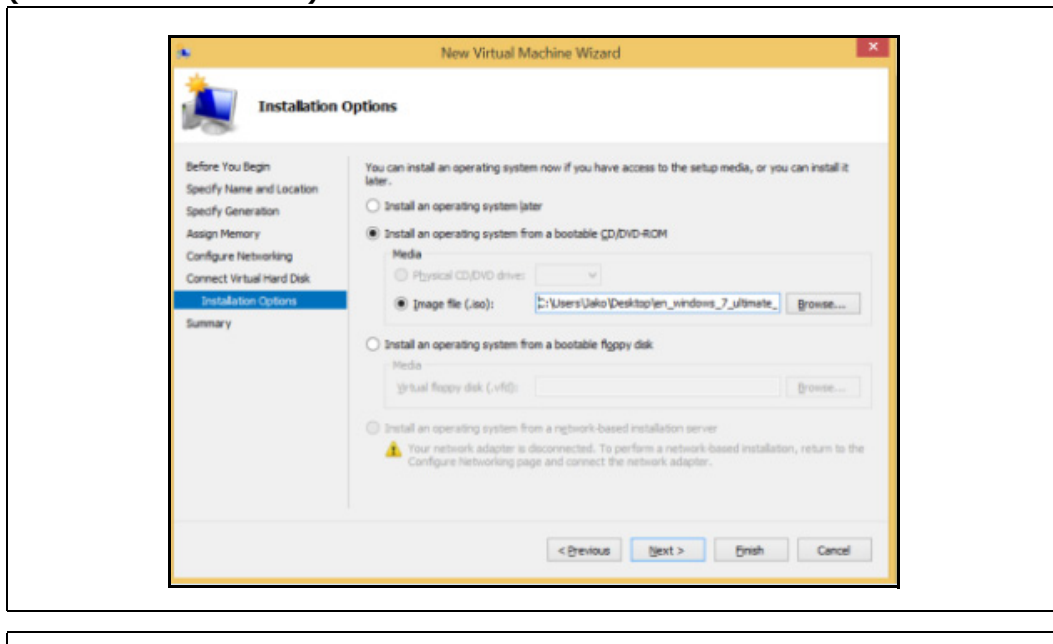


8. On the **Configure Networking** page, leave the default settings.



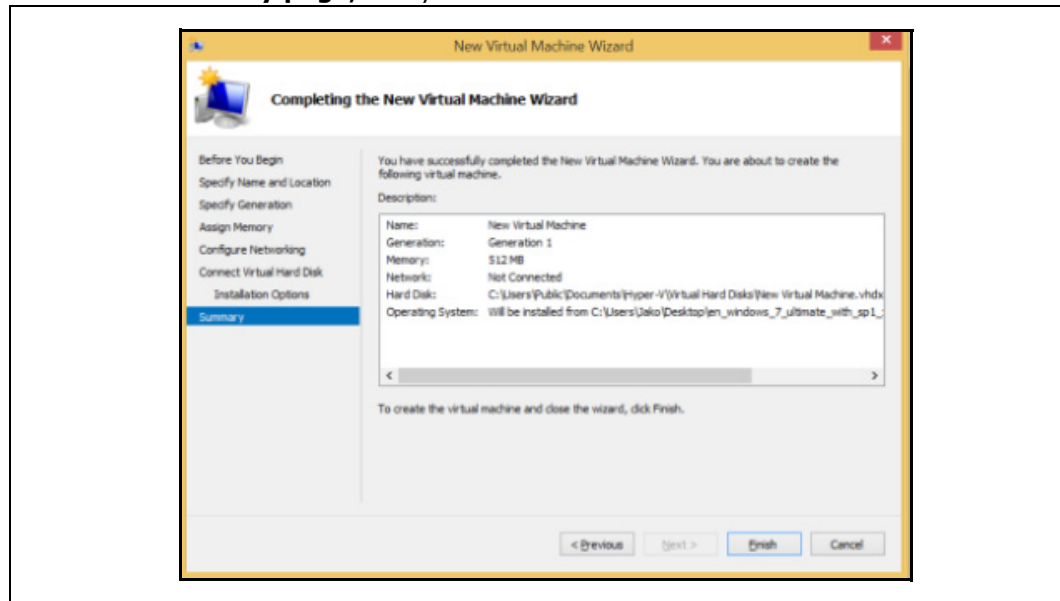
On the **Connect Virtual Hard Disk** and **Installation Options** pages, choose the option that is appropriate to install the guest operating system:

If the guest operating system is installed from a DVD or an image file (an .ISO file), choose **Create a virtual hard disk**. Click **Next**, and then click the option that describes the type of media you will use. For example, to use an .iso file, click **Install an operating system from a boot CD/DVD** and then specify the path to the .iso file. **(This is recommended)**

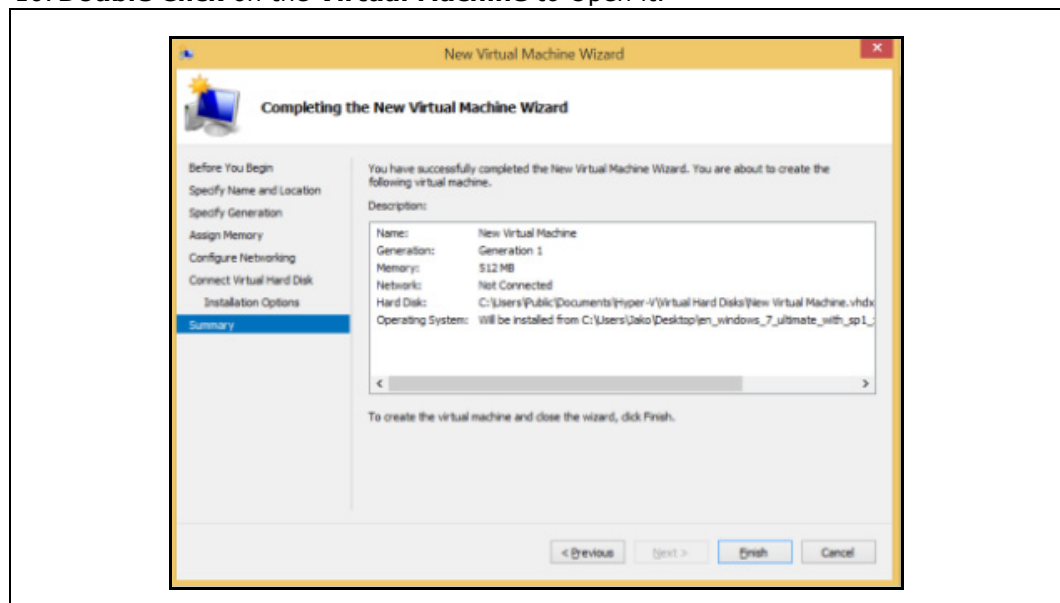


- g. If the guest operating system is already installed in a virtual hard disk, choose **Use an existing virtual hard disk** and click **Next**. (Refer figure at top of page). Then, choose **Install an operating system later**.

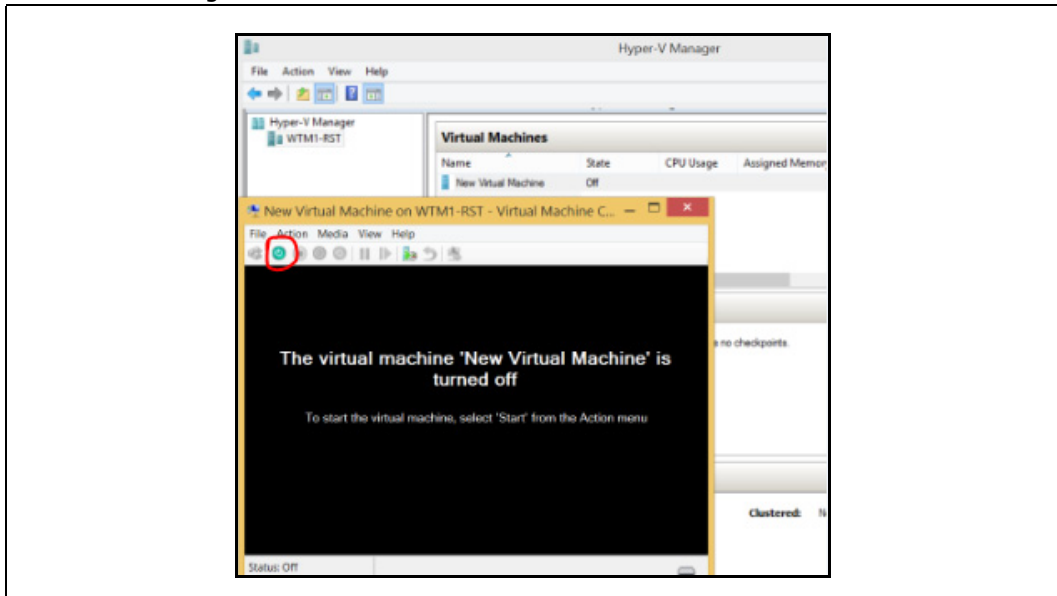
9. On the **Summary** page, verify the selections and then click **Finish**.



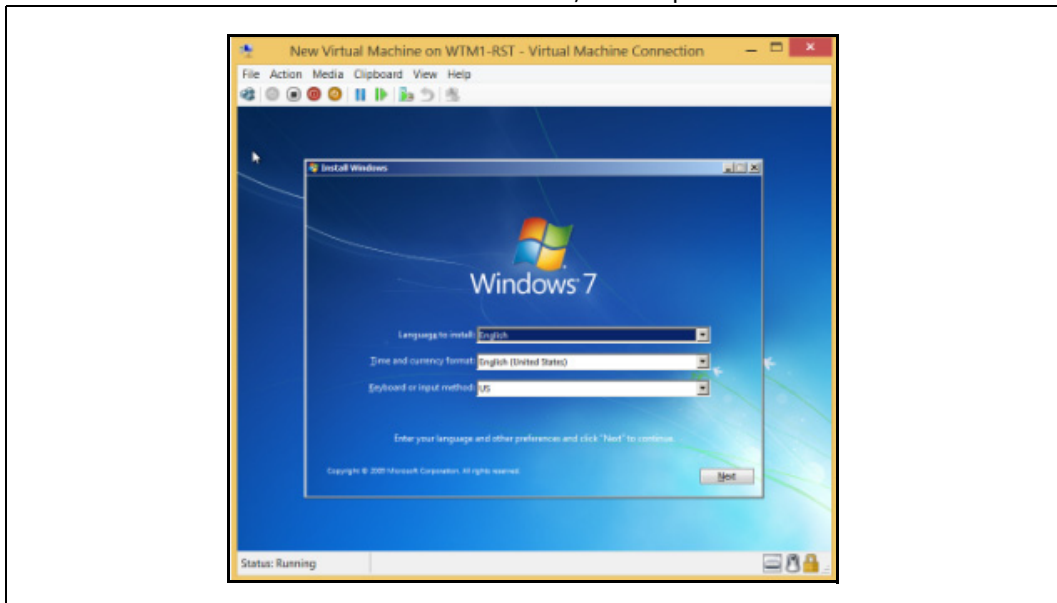
10. **Double Click** on the **Virtual Machine** to Open it.



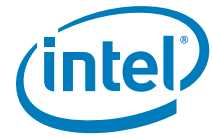
11. Click on the green **Start** button to run Virtual Machine.



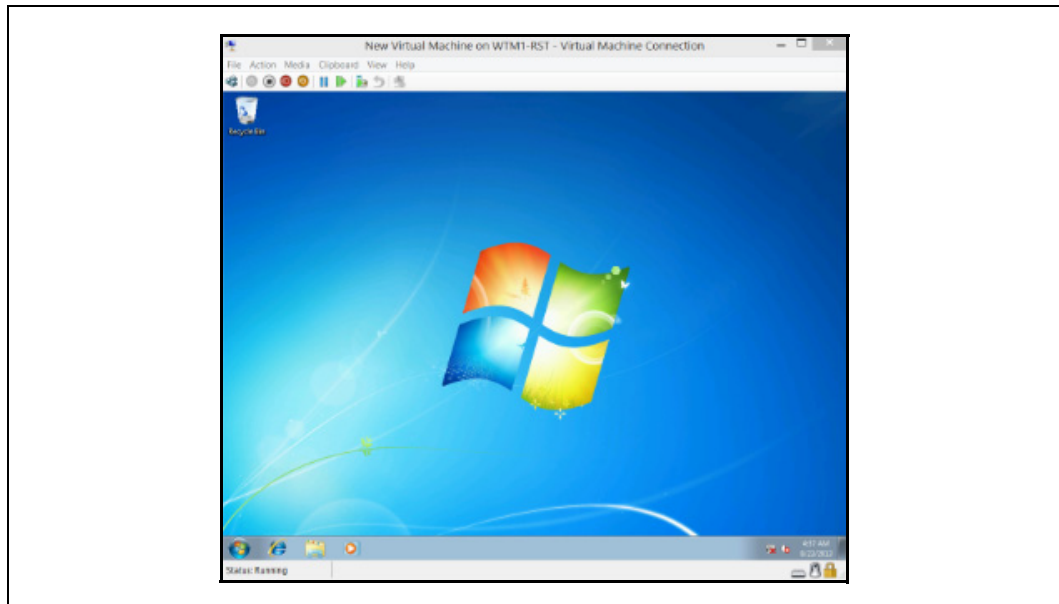
12. **Follow** normal OS Installation Instructions, this depends on OS chosen.







13. Once this is complete, then Virtual Machine resembles as a normal System inside the Virtual Machine Window.





### 18.2.3 Intel® VT Tests in Xen\*/Linux\* Environment

#### Test Environment:

A system under test is needed, which has an Intel® VT-x and Intel® VT-d capable Processor, a stable BIOS with support for VT-x and VT-d technologies. Prior to tests **enable Virtualization (or VT-x)** and **VT-d** in BIOS and make sure **TXT is Disabled**.

#### Tools for Testing:

- Open source openSUSE\* 42.1 or Open source Fedora\* 17.
- Xen\* open source VMM.

#### 18.2.3.1 Verifying If System Under Test (SUT) Boots Xen\* Mode/VMM

Test ID	VT_TC03A
Test Case Title	Xen* Hypervisor Boots (Xen* Environment)
Mandatory/Optional	Optional
Description	Ensures that Test cases VT_TC13, VT_TC14 and VT_TC15 can be executed.
Objective	Verify platform can boot to Xen* Hypervisor/VMM
Preparation	<ol style="list-style-type: none"><li>1. Install Xen* OS (for example openSUSE* 42.1 or Fedora* 17 or equivalent).</li><li>2. Enable Intel® Virtualization Technology (VT-x) and VT-d in BIOS.</li><li>3. Build/Install Xen* VMM.</li></ol> <b>Installation steps are explained in Section 18.3.</b>
Procedure	<ol style="list-style-type: none"><li>1. Boot to Xen* drive.</li><li>2. Choose Xen* Hypervisor option.</li><li>3. When system boots, login as root.</li><li>4. To login as root: Change user to root and use password: linux123.</li><li>5. Enter "xl info" into terminal. Result should give Xen version number and no error message.</li></ol>
Test Pass/Fail Criteria	Test passes, when the following occurs: System successfully boots to Xen* Hypervisor with no error messages.



### 18.2.3.2 Verifying Intel® VT-x and VT-d Enabled (Xen\* Mode)

Test ID	VT_TC03B
Test Case Title	Intel® VT-x and VT-d Enabled (Xen* Environment)
Mandatory/Optional	Optional
Description	Ensures that VT-d is enabled and supported. This test is in Xen* Hypervisor.
Objective	Verify Intel® VT Functionality is enabled on the SUT.
Preparation	<p>Install Xen* OS (for example openSUSE* 42.1 or Fedora* 17)  Download and build/Install Xen*.  <b>Installation steps are explained in Section 18.3.</b></p>
Procedure	<ol style="list-style-type: none"> <li>1. Boot to Xen* Mode.</li> <li>2. Open terminal.</li> <li>3. Enter <b>xl dmesg   grep -i Virt</b>  This should yield:  (XEN) I/O virtualisation enabled</li> <li>4. Enter <b>xl dmesg   grep -i VT</b>  This should yield:  (XEN) Intel VT-d iommu 0 supported page sizes: 4 kB, 2 MB, 1 GB.  (XEN) Intel VT-d iommu 1 supported page sizes: 4 kB, 2 MB, 1 GB.  (XEN) Intel VT-d Snoop Control not enabled.  (XEN) Intel VT-d Dom0 DMA Passthrough not enabled.  (XEN) Intel VT-d Queued Invalidation enabled.  (XEN) Intel VT-d Interrupt Remapping enabled.  (XEN) Intel VT-d Shared EPT tables enabled.</li> </ol> <p><b>Note:</b> "dmesg" is Xen* command, run from a terminal. Depending on the version of Xen kernel, "xl" might be replaced with "xl -f" or "xm"</p>
Test Pass/Fail Criteria	<p>Test passes when all the following occur:</p> <ol style="list-style-type: none"> <li>1. "xl dmesg   grep -i virtual" results in:  (XEN) I/O virtualisation</li> <li>2. "xl dmesg   grep -i VT" results in:  (XEN) Intel VT-d iommu 0 supported page sizes: 4 kB, 2 MB, 1 GB.  (XEN) Intel VT-d iommu 1 supported page sizes: 4 kB, 2 MB, 1 GB.  (XEN) Intel VT-d Snoop Control not enabled.  (XEN) Intel VT-d Dom0 DMA Passthrough not enabled.  (XEN) Intel VT-d Queued Invalidation enabled.  (XEN) Intel VT-d Interrupt Remapping enabled.  (XEN) Intel VT-d Shared EPT tables enabled.</li> </ol> <p><b>Note:</b> There may be additional results too; if above results are shown on test system, this test is passing.</p>



### 18.2.3.3 Verifying Intel® VT-d Functionality VM Boots (Xen\* Mode)

Test ID	VT_TC03C
Test Case Title	Intel® VT-d Functionality - Virtual Machine (VM) Boots (Xen* Environment)
Mandatory/Optional	Optional
Description	Verifies VT_TC14 can be executed.
Objective	Verify Intel® VT implementation at platform level.
Preparation	Enable Intel® Virtualization Technology (VT-x) and VT-d in BIOS. 1. Install Xen* OS (for example openSUSE* 42.1 or Fedora* 17). 2. Install/Build Xen* VMM onto Xen* OS. <b>Instructions are explained in Section 18.3.</b>
Procedure	1. Boot to Xen* Hypervisor Mode 2. Open Virtual Machine Manager 3. Create a Virtual Machine. Instructions are explained in <a href="#">Section 18.3.2.3</a> . 4. Launch Hardware Virtual Machine (HVM) for example Windows* XP, Windows* 7 or other OS as a Virtual Machine. 5. Verify that no VT faults are reported using <b>dmesg   grep -i VT</b> .
Test Pass/Fail Criteria	Test passes, when all the following occur: 1. A Virtual Machine (VM) is open and working. 2. Verify that no VT faults are reported in serial log messages and "dmesg" log. <b>Note:</b> "dmesg" is Xen* command, run from a terminal. You may need to use xm dmesg (prior to Xen* 4.1.0) or xl dmesg (if you are using Xen* 4.1.0 and later).



#### 18.2.3.4 Verifying Intel® VT-d Functionality Pass Through (Xen\* Mode)

Test ID	VT_TC03D
Test Case Title	Intel® VT-d Functionality—Pass through with No VT-d Error (Xen* Environment)
Mandatory/Optional	Optional
Description	<p>Verifies Intel® VT-d Functionality by Assigning Devices to Guest OS and checking for errors by output log messages.</p> <ul style="list-style-type: none"> <li>Validates Intel® VT BIOS implementation by using Intel® VT hardware as exposed by BIOS through ACPI table.</li> <li>Creates Address translation tables as per Intel® VT Specification</li> <li>Exercises Intel® VT-d functionality by assigning devices to guest OS – outputs log messages</li> <li>Outputs debug messages on serial port. (Intel® VT messages have a keyword “Intel VT” or “Intel VT-d” on the lines)</li> </ul>
Objective	Verify Intel® VT implementation at platform level.
Preparation	Required to test VT_TC13.
Procedure	<p>If already user have an open Virtual Machine, skip to step 3.</p> <ol style="list-style-type: none"> <li>Boot to Xen* Hypervisor (with Intel® VT and Intel® VT-d enabled in BIOS setup options).</li> <li>Launch Hardware Virtual Machine (HVM) for example Windows* XP or Windows* 7.</li> <li>Directly assign one or more I/O devices to guest HVM, for example Ethernet Controller, Integrated Network device, Audio, Firewire, USB controller and so forth. Refer <a href="#">Section 18.3.2.4</a> for instructions.</li> <li>Verify that no VT faults are reported in serial log messages.</li> <li>Verify that no VT faults are reported using <b>dmesg   grep -i VT</b></li> </ol>
Test Pass/Fail Criteria	<p>Test passes, when all the following occur:</p> <ol style="list-style-type: none"> <li>Directly assign one or more I/O devices to guest HVM, for example Integrated Network device, Audio, Firewire, USB controller and so forth.</li> <li>Verify that directly assigned I/O device is visible only in HVM.</li> <li>Verify that no VT faults are reported in serial log messages and “dmesg” log.</li> </ol> <p><b>Note:</b> “dmesg” is Xen* command, run from a terminal. User may need to use <code>xm dmesg</code> (prior to Xen* 4.1.0) or <code>xl dmesg</code> (if using Xen* 4.1.0 and later.)</p>



### 18.2.3.5 Verifying Intel® VT-d Functionality Through IOMMU Exercise

Test ID	VT_TC04
Test Case Title	Intel® VT-d Functionality - IOMMU Exercise (Xen* Environment)
Mandatory/Optional	Optional
Description	Runs in Xen* Environment. Enable Intel® Virtualization Technology (VT-x) and VT-d in BIOS. Dynamically creates Intel® VT-d address translation tables by running concurrent workloads on integrated I/O devices like graphics, network device, HD audio, FireWire or USB device. Since, Xen* IOMMU does page invalidation on each I/O transaction, it stresses the Intel® VT-d at system level in a unique way.
Objective	Verify Intel® VT-d functionality through the IOMMU driver.
Preparation	Install openSUSE* 42.1. The latest stable Xen* includes Intel® VT-d IOMMU driver. <b>Xen* installation steps are explained in Section 18.3.</b>
Procedure	<ol style="list-style-type: none"><li>1. Boot openSUSE* Xen* with Intel® Virtualization Technology (VT-x) and VT-d enabled in BIOS.</li><li>2. Run concurrent workloads like TTCP or disk copy, <b>while</b> playing audio to stress these I/O devices, and/or playing video clips from internet (for example YouTube* and so forth) at same time.</li><li>3. Check for error messages. IOMMU driver forwards faults in the DMESG log or the RS232 port.</li></ol>
Test Pass/Fail Criteria	Test passes, when IOMMU messages appear in DMESG log or on RS232 port, and no VT-d faults are reported in DMESG log or serial port log. <b>Note:</b> "dmesg" is Xen* command, run from a terminal. You may need to use xm dmesg (prior to Xen* 4.1.0) or xl dmesg (if you are using Xen* 4.1.0 and later).

## 18.3 User Guide—Installing and Using Linux\* (openSUSE\* 42.1, Fedora\* 17) and Xen\* VMM for Intel® VT Testing

### 18.3.1 Platform Setup Requirements

The system/platform on which the Linux\*/Xen\* is to be installed is System Under Test (SUT). The following are the SUT setup requirements:

System needs to be stable and booting to DOS\*/Windows\* OS:

- Add Intel® PRO100 Network PCI card. This is needed as Linux\*/Xen\* installation requires a working network connection. If the system is based on Intel® 5 Series Express Chipsets or previous generation chipsets, the onboard wired network is sufficient.
- Add DVD ROM drive for booting Linux\* from CD or DVD.
- BIOS setup options:
  - **Optional: Disable** "Intel Virtualization Technology" and "Intel® VT-d" in BIOS setup options (prior to OS installation, then **Enable after installation** is complete).
  - Set SATA disk drive mode to **AHCI mode**.

### 18.3.2 Using openSUSE\* 42.1 (64-Bit)

For a video on [openSUSE\\* 11.3 Xen Hypervisor Installation](#), refer the Videos Section on Broadwell Platform PCDC VT page.



**Note:** openSUSE\* 11.3 installation is very similar to openSUSE\* 42.1 installation.

### 18.3.2.1 Standard Linux\* Installation for openSUSE\* 42.1

View instructions below or refer [openSUSE\\* Installation Instructions](#). Make sure to also follow **step 8** below.

1. Download openSUSE\* 42.1 (64-bit) and burn it on a DVD. Examples and references used in this procedure are based on installing openSUSE\* 42.1 on an Intel® CRB.
2. After booting the openSUSE\* DVD, choose Installation.
3. Select Language and Keyboard Layout. Click Next
4. Choose New Installation. Click Next.
5. Choose region and Time Zone. Click Next.
6. Select preferred desktop environment. Click Next.
7. Choose Partition based or LVM based. Click Next.
8. Enter Username and Password. Click Next **(Un-check the option to automatically sign in, during installation)**.
9. Review settings, modify any if necessary, and Click Install.
10. After Installation, the configuration is automatically created.

### 18.3.2.2 Xen\* Hypervisor Installation on openSUSE\* 42.1

1. Choose the default option on boot options menu, and log in using root as the username.
2. Ensure the openSUSE\* 42.1 installation disk is loaded.
3. In the Applications Menu go to *System > Install Hypervisor and Tools* (Or search for YaST2).
4. Choose Xen\* and Accept.
5. When asked to configure a default network bridge, choose Yes.
6. Reboot Machine.
7. To verify, if Xen\* Hypervisor is installed:
  - a. Boot up machine.
  - b. Choose Xen\* – openSUSE\* 42.1.
  - c. Log in as root user.
  - d. Open terminal and type **uname -r**
  - e. User should see “xen” along with the kernel version number.

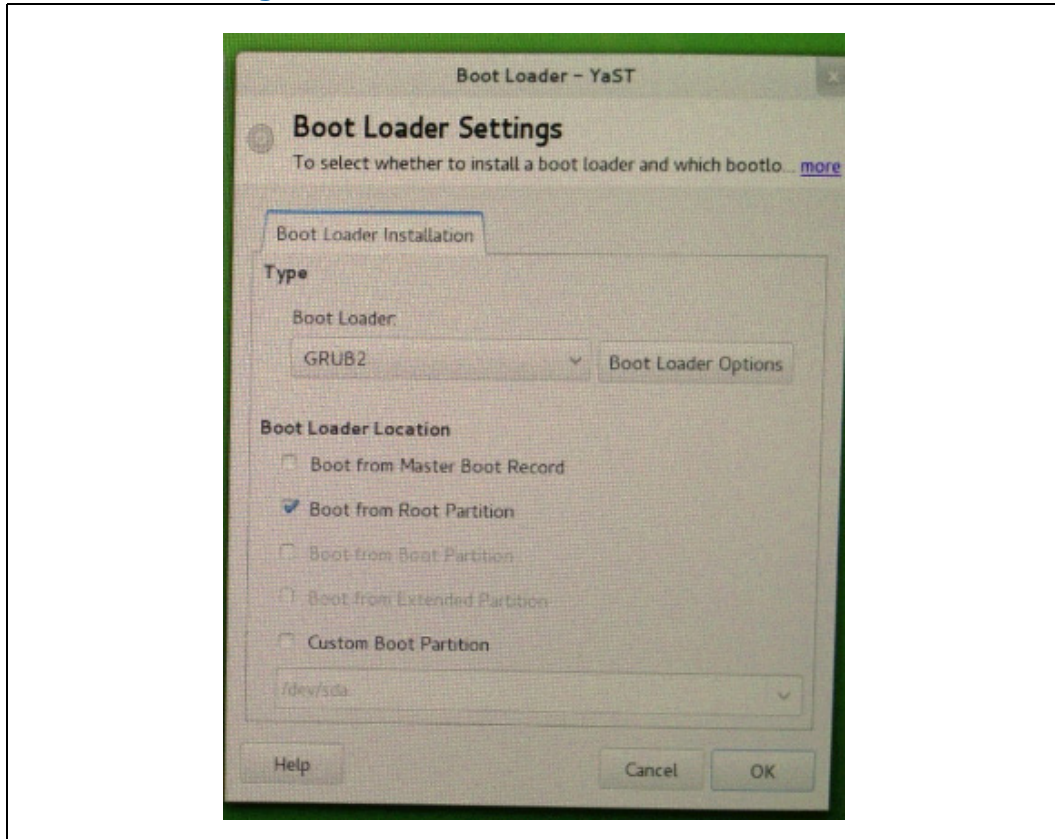
#### 18.3.2.2.1 Tip: What to do, if Xen Hypervisor Option Does Not Show Up

After Xen Installation, if Xen Hypervisor does not show up in the boot loader menu, user may need to change its boot loader configuration file after Xen Installation:

1. Reboot the system after installation.
2. Use Desktop boot option (the first option).
3. Find the Yast Boot Loader Settings: **Computer > Yast > System > Boot Loader** or **Administrator Settings > Boot Loader**

4. Enter Boot loader type: **GRUB2**. Choose **Boot from Root Partition**. Click **Ok**.
5. After a reboot, user will see the hypervisor in the boot loader menu.

**Figure 18-1. Boot Loader Settings**



### 18.3.2.3 Creating a Virtual Machine on openSUSE\* 42.1

1. Choose Xen\* Hypervisor boot option and log in using root as username.
2. In Applications Menu go to *System > Virtualization > Create Virtual Machines*.
3. Click **Forward**.
4. Insert Guest OS Installation disk.
5. Choose to install an operating system. Click **Forward**.
6. Choose, Guest OS user would like to use and click **Forward**.
7. Review Summary of Virtual Machine.
  - a. To change the Name of Virtual Machine. Click **Apply**.
  - b. Also in Hardware section, ensure that user must have at least 1024 MB of Initial Memory and Maximum Memory. Click **Apply**.
  - c. In Disks option, add CD-ROM by clicking on CD-ROM and Move CD-ROM to the top option using the arrows. Click **Apply**.
  - d. In Network Adapters delete any default adapters. Click **Apply**.
  - e. Then click **OK**.





- f. Follow the on screen instructions for installing the Guest OS in the Virtual Machine.

### 18.3.2.4 Testing Intel® VT Using Xen\* VMM in openSUSE\* 42.1

The Intel® VT can be tested by assigning PCIe\* I/O device(s) to the guest OS. When Intel® VT-d is used to directly assign an I/O device to a guest, the guest OS has direct access to I/O device hardware and guest VM owns the physical driver for that I/O device.

The test is considered to be passing when all of the following occur:

1. An I/O device can be successfully assigned to guest VM ([Section 18.3.2.4.1](#)).
2. Xen\* VMM does not report any VT faults. Xen\* VMM reports no VT faults in “dmesg” log. User need to search for VT faults by executing the following and search for VT messages:

```
dmesg | grep -i fault
--OR--
xm dmesg | grep -i fault (if using Xen earlier than 4.1)
--OR--
xl dmesg | grep -i fault (if using Xen 4.1.0 or later)
```

3. Guest VM detects the presence of new hardware (In a Windows\* OS, this can be determined through the VM device manager.)
4. If the physical driver for the newly assigned I/O device is present in the guest OS, check that the device is functional.

#### 18.3.2.4.1 Assigning an I/O Device Using PCISTUB Method

1. First obtain the Bus, Device, Function (BFD) ID of the device using:

```
lspci --OR-- lspci | grep -i Ethernet
```

Example result:

```
...
00:19.0 Ethernet controller: Intel Corporation 82566DM Giga-
bit Net...
...
BDF = "00:19.0"
```

2. Enter the following, in order to unbind and attach the device:

- a. `echo -n 0000:00:19.0 > /sys/bus/pci/devices/0000:00:19.0/driver/unbind`
- b. `echo 0000:00:19.0 > /sys/bus/pci/devices/0000:00:19.0/driver/unbind`
- c. `echo 0000:00:19.0 > /sys/bus/pci/drivers/pciback/new_slot`
- d. `echo 0000:00:19.0 > /sys/bus/pci/drivers/pciback/bind`
- e. `ls -l /sys/bus/pci/devices/0000:00:19.0/driver`  
this verifies the binding
- f. `xl pci-attach Guest 0:0:19.0`  
where *Guest* is the name of virtual machine

**Note:** In Xen\* 4.1 or earlier, use “xm” instead of “xl”

To find version of Xen\* are using, use **xl info** or **xm info** command.



### 18.3.2.5 Special Instructions to Obtain Serial Log on openSUSE\* 42.1

User will need to modify the serial device parameters in the grub file to receive kernel information on a serial port.

1. Open /boot/grub/menu.lst.
2. Add the changes highlighted in red below:

#### Original

```
title Desktop -- openSUSE 42.1 - 2.6.37.1-1.2.Original
    root (hd0,0)
    kernel /vmlinuz-2.6.37.1-1.2-desktop root=/dev/system/root
    resume=/dev/system/swap splash=silent showopts vga=0x31a
    initrd /initrd-2.6.37.1-1.2-desktop
```

#### New

```
title Desktop -- openSUSE 42.1 - 2.6.37.1-1.2
    root (hd0,0)
    kernel /vmlinuz-2.6.37.1-1.2-desktop com6=115200,8n1 con-
sole=com6L root=/dev/system/root resume=/dev/system/swap
    splash=silent console=tty0 console=ttyS0,115200 showopts
    vga=0x31a
    initrd /initrd-2.6.37.1-1.2-desktop
```

**Note:** In this example, com6/com6L is used, however COMM ports may vary.

## 18.3.3 Using Fedora\* 17 (64-Bit)

For a video on Installing Fedora\* and Xen\*, refer [VT Training Series Videos](#) on PC Design Center.

### 18.3.3.1 Standard Linux\* Installation for Fedora\* 17 (64-Bit)

Prior to OS Installation, refer [Section 18.3.1](#). Download Fedora\* 17 (64-bit) and burn it on a DVD. Examples and references used in this procedure are based on installing Fedora\* 17 on this platform (using Intel CRB). After booting the Fedora\* DVD, follow the installation instructions below, (also, refer to Fedora\* installation guide on web).

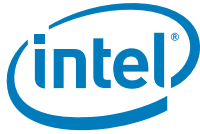
1. Select Language and Keyboard Layout. Click Next after each page is complete.
2. Choose "Basic Storage Devices" in Installation Options. Click Next.
3. Choose system name, desired time zone, and password. Click Next after each.
4. Choose what type of Installation to use (It is recommended to Use All Space), also check Use LVM. Click Next and Write Changes to Disk.
5. When prompted, choose "Software Development" and "Customize Now" option (at bottom of page) to install additional packages. Click Next. The recommended packages to install are:
  - a. Applications > Office and Productivity
  - b. Development > Development Tools
  - c. Development > Development Libraries
  - d. Base System > System Tools
  - e. Base System > Virtualization Client



- f. Base System > Virtualization Hypervisor
- g. Servers > Network Server
6. Click Next and continue the installation
7. The system prompts for reboot after installing Fedora\*, so that the changes can be made.
8. After the reboot follow the instructions to create an account, when prompted. Click Forward.
9. Alter login settings from user account:
  - a. Log on with the personal account created.
  - b. Move to root permissions (using Linux\* command "su").
  - c. When prompted for a password, make sure to use the root password.
  - d. Edit files for root login:
    - i. Change to root directory using **cd /**
    - ii. Edit "gdm-password" file in: **/etc/pam.d/gdm-password**
    - iii. Comment out the following line:  
Auth required pam\_succeed\_if.so user !=root quiet
    - iv. Save the file and log out of system
10. Log back in as root user.
11. **Optional:** If user need to enable Ethernet access on boot:
  - a. Edit the following file: **/etc/sysconfig/network-scripts/ifcfg-eth0**.
  - b. Change **ONBOOT=no** to **ONBOOT=yes**.
  - c. Reboot system.
  - d. Log in as root after system reboot.

#### 18.3.3.1.1 Installing Additional Packages for use with Fedora\* 17

1. Open a web browser or terminal window and check again that user have a good internet connection (using "ifconfig", look for an assigned IP address in terminal).
2. Optional: If the environment uses a proxy to connect to the internet, open a terminal window and type the command (as an example).  
**export http\_proxy=http://proxy.yourcompany.com:port#**
3. Install the following packages using yum:
  - a. **yum -y update yum**
  - b. **yum -y install bridge-utils**
  - c. **yum -y install mkinitrd**
  - d. **yum -y install iasl**
  - e. **yum -y install dev86**
  - f. **yum -y install unifdef**
  - g. **yum -y install mercurial**
  - h. **yum -y install xfig**
  - i. **yum -y install tigervnc-server**
  - j. **yum -y install git**



k. `yum -y install mesa-demos` (this is for glxgears)

**Note:** If user receive the following error: **"Error: Cannot retrieve metalink for repository: Fedora. Verify its path and try again"** Do the following to fix it:

1. CD to `/etc/yum.repos.d`.
2. Open `fedora.repo` in a text editor.
3. Mask each instance of `"#mirrorlist="` and unmask each instance of `"baseurl="`.
4. Save file and do the same (steps 2 and 3) for `fedora-updates.repo`.

**Note:** If user have difficulty installing from CD-ROM, try using an ISO file. Make sure to first copy the ISO file over to the local system (Using right click > Copy To > Home) and then use the local file.

### 18.3.3.2 Xen\* Hypervisor Installation on Fedora\* 17

First log into system as root user and ensure that the system is connected to the internet. To install and configure Xen\* Hypervisor:

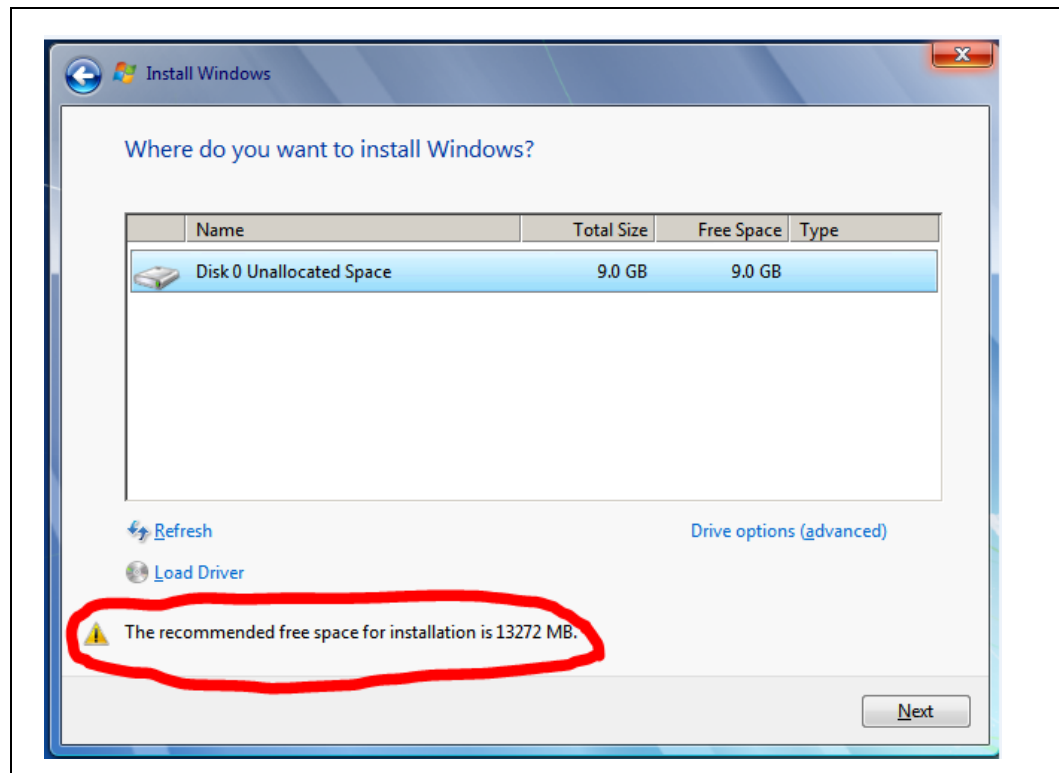
1. Enter **`yum install xen and/or yum install xen kernel-xen`**, or Download from **`http://xen.org/products/xen_source`** (This downloads latest Xen\* Hypervisor available on the xen.org website).

### 18.3.3.3 Creating a Virtual Machine on Fedora\* 17

For a video on [Creating a virtual machine on Fedora\\* 14](#), refer the Videos Section on Broadwell Platform PCDC VT page.

**Note:** This process in Fedora\* 14 is very similar to Fedora\* 17.

1. Go to *Applications > System Tools > Virtual Machine Manager*. (if user is not logged in as root user, user needs to provide root password to continue).
2. Go to *File > Add Connection > Choose Xen* and Click Connect.
3. Click on localhost (xen).
4. Click **Create a new virtual machine** icon and enter Name. Choose Xen\* as connection type. Select Local installation media (ISO image or CD-ROM).
5. Select the Installation Source (If using an ISO file, it is best to copy the file directly to the system), choose OS type and version. Click Forward.
6. Choose 2048 MB RAM or more and 1 Processor. Click Forward.
7. Choose Enable storage for this virtual machine, allocate atleast 14 GB (This number may vary. If no enough space is allocated, user may get an error that communicates user for how much to allocate. Refer [Figure 18-2](#)), and check allocate entire disk now.
8. Optional: In Final step, open Advanced options, use default Virtual network, change Virtual Type to xen, set architecture as x86\_64 and Click Finish.
9. Follow the installation instructions for the OS.

**Figure 18-2. Example Warning—Allocating Space for Windows\* 7/Virtual Machine**


#### 18.3.3.4 Testing Intel® VT Using Xen\* VMM in Fedora\* 17

The Intel® VT can be tested by assigning PCIe\* I/O device(s) to the guest OS. When Intel® VT is used to directly assign an I/O device to a guest, the guest OS has direct access to I/O device hardware and guest VM owns the physical driver for that I/O device.

The test is considered to be passing, when all of the following occur:

1. An I/O device can be successfully assigned to guest VM ([Section 18.3.3.4.1](#)).
2. Xen\* VMM does not report any VT faults. Xen\* VMM reports no VT faults in "dmesg" log. User need to search for VT faults by executing the following and search for VT messages:
 

```
dmesg | grep -i fault
--OR--
xm dmesg | grep -i fault (if using Xen earlier than 4.1)
--OR--
xl dmesg | grep -i fault (if using Xen 4.1.0 or later)
```
3. Guest VM detects the presence of new hardware. (In a Windows\* OS, this can be determined through the VM device manager).
4. If the physical driver for the newly assigned I/O device is present in the guest OS, check that the device is functional.



#### 18.3.3.4.1 Assigning an I/O Device Using PCISTUB Method

1. First obtain the Bus, Device, Function (BDF) ID of the device using:

```
lspci --OR-- lspci | grep -i "Ethernet"
```

Example result:

```
...  
00:19.0 Ethernet controller: Intel Corporation 82566DM Giga-  
bit Net...  
...  
BDF = "00:19.0"
```

2. Now obtain device ID

```
lspci -n
```

Example Result:

```
...  
00:19.0 0200: 8086:153a (rev 01)  
00:16.0 0200: 8086:8c3a (rev 01)  
...  
Use the BDF to find Device ID  
Device ID = "8086 153a"
```

3. Enter the following, in order to unbind and attach the device

```
echo -n 0000:00:19.0 > /sys/bus/pci/devices/0000:00:19.0/  
driver/unbind
```

```
echo "8086 153a" > /sys/bus/pci/drivers/pci-stub/new_id
```

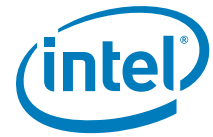
```
echo -n 0000:00:19.0 > /sys/bus/pci/drivers/pci-stub/bind
```

```
ls -l /sys/bus/pci/devices/0000:00:19.0/driver  
this verifies the binding
```

```
xm pci-attach Guest 0:0:19.0
```

where *Guest* is the name of virtual machine

xl pci-assignable-add/remove



#### **18.3.3.5 Special Instructions to Obtain Serial Log on Fedora\* 17**

To be added in a future revision.

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# 19 Intel® Device Protection Technology with Intel® Boot Guard

## 19.1 Overview

Intel® Boot Guard (BtG) formerly Anchor Cove (AnC) is an Intel platform boot integrity protection technology. Intel® Boot Guard can protect the platform boot integrity by preventing execution of unauthorized boot block. With Intel® Boot Guard, the OEM can create a platform boot policies, such that invocation of an unauthorized (or compromised) boot block triggers the platform protection per the OEM policies. Based on the hardware, Intel® Boot Guard also extends the trusted boundary of the platform boot process down to the hardware. A benefit of this protection is that Intel® Boot Guard can help OEM maintains platform integrity by preventing reuse of the OEM hardware to run unauthorized software stack.

**Note:** The terms Intel® Boot Guard and Anchor Cove may be used interchangeably in this chapter.

## 19.2 Scope

This chapter describes a validation strategy for Intel® Boot Guard. This chapter is intended for validation purposes. The objective is to provide validation professionals with additional insight into Intel® Boot Guard by highlighting validation considerations. This chapter is not a technology overview and does not replace the existing Intel® Boot Guard collateral. The reader is expected to be familiar with Intel® Boot Guard and to use this document, as a validation supplement to develop his own validation plan.

## 19.3 Prerequisite

This Intel® Boot Guard evaluation plan documented in this chapter requires the following components and tools for execution.

**Table 19-1. Intel® Boot Guard Tools for Testing (Sheet 1 of 2)**

Tool/Component	Revision	Comments
FIT	ME firmware kit with Intel® Boot Guard support	<b>FIT</b> is required to define the Intel® Boot Guard Boot Policies (persistent policies). Available on VIP
MEInfo	ME firmware kit with Intel® Boot Guard support	<b>MEInfo</b> is required to confirm Intel® Boot Guard Policies. Available on VIP  <b>Note: Non-Windows OS:</b> Use the EFI version of the CSME tools (MEInfo.efi) to confirm Intel® Boot Guard Policies





Table 19-1. Intel® Boot Guard Tools for Testing (Sheet 2 of 2)

Tool/Component	Revision	Comments
TXtBtgInfo.efi	0.7.10 or higher	<p>TXtBtgInfo.efi can be used to confirm Intel® Boot Guard status in the test cases below. Available on IBL. Training videos for TXtBtgInfo are available on PCDC under Ingredients-&gt;Technologies-&gt;Intel® Boot Guard-&gt;Latest Videos</p> <p>Intel® Boot Guard status can also be determined using various platform status registers:</p> <ol style="list-style-type: none"> <li>1. Refer to BIOS Writers Guide for status registers (Example: ERRORCODE, BOOTSTATUS, ANC_SACM_INFO) usage</li> <li>2. Refer to ME BIOS Writer's Guide for Intel® Boot Guard related FWSTS registers verification.</li> </ol>

## 19.4 Intel® Boot Guard Test Coverage Summary

**Note:** Profile 1 and profile 2 support are deprecated. Only Profile 0: NO\_FVME, Profile 3: VM, Profile 4: FVE and Profile 5: FVME are supported.

**Note:** Successful Intel® Boot Guard on S3 Resume is removed as TXtBtgInfo.efi tool runs only from EFI shell.

How?: A = Fully Automated using Intel® PETS, I = Interactive using Intel® PETS and M = Manual.

Test ID	Test Case Title
BtG_001	Successful Verified Measured (VM) Boot to OS <sup>1</sup>
BtG_002	Unsecure Boot to OS <sup>1</sup>
BtG_003	Failed Verified Measured (VM) Boot fail to Fallback
BtG_004	Platform Public Signing Key Provisioned
BtG_005	Successful Verified Measured (VM) Boot to OS <sup>1</sup> using FPF
BtG_006	BIOS Update Procedure includes Signature Verification
BtG_007	Service Center's Recovery process for Intel® Boot Guard failed platform
BtG_008	BIOS Continues the Chain of Trust

**Notes:**

1. Refer to [Section 1.1](#) for supported Operating Systems (OS).

Test ID	BtG_001
Test Case Title	Successful Verified-Measured (VM) Boot to OS
Mandatory/Optional	Mandatory
Firmware SKU	Consumer / Corporate
Description	In this test case, Intel® Boot Guard performs a successful verification and measuring of the SUT Initial Boot Block (IBB.) Upon successful verification Intel® Boot Guard passes execution to the IBB to continue the boot process.
Objective	This test verifies that the SUT has all the required components: hardware, firmware, ACM and BIOS. Additionally, the SUT is correctly provisioned in manufacturing for the platform to boot with the Intel® Boot Guard for IBB verification and measurement



Test ID	BtG_001
Procedure	<p><b>Prepare the SUT Persistent Policy (FPF)</b></p> <ol style="list-style-type: none"> <li>Provision the SUT Persistent Policies (NVAR, if this is development system) to either the VM or FVE or FVME profile. Per the testing objective. <ul style="list-style-type: none"> <li><b>The FVME profile usage is not advised for the development or testing environment.</b> In this strictest protection mode, test failure requires BIOS flashing to restore the system.</li> <li>Refer the ME Firmware Bring Up Guide for information on the Intel® Boot Guard related FIT options and settings.</li> </ul> </li> <li>Install the Intel® ME firmware and BIOS image that are Intel® Boot Guard enabled and are authorized by the key in the Persistent Policy (FPF or NVAR).</li> <li>Install the targeted OS (OS), if not already installed on the SUT.</li> <li>Run the MEinfo tool and check for the fields under "FPF" column for FPF contents and "ME" for NVAR contents. Ensure that these matches with what was provisioned during the image creation process.</li> </ol> <p><b>Verify the Boot</b></p> <ol style="list-style-type: none"> <li>Power-off the SUT.</li> <li>Power-on the SUT.</li> <li>Boot to EFI shell and execute TXTBtgInfo.efi.</li> <li>Verify the TXTBtgInfo.efi output to confirm that Intel® Boot Guard has booted as configured to verify and measure the IBB.</li> <li>Boot to OS.</li> <li>Execute PETS package for Intel® Boot Guard from Remote Console.</li> <li>Verify PETS results should Pass.</li> </ol>
Test Pass/Fail Criteria	<p>Test passes, if the SUT:</p> <ul style="list-style-type: none"> <li>Boots fully functional to OS.</li> <li>The TPM/PTT device reports the correct measurement in PCR.</li> <li>PETS tests BootGuard_001 and BootGuard_002 should Pass.</li> <li>TXTBtgInfo.efi reports that Intel® Boot Guard was successful.</li> </ul>

Test ID	BtG_002
Test Case Title	Un-secure Boot to OS
Mandatory/Optional	Mandatory
Firmware SKU	Consumer / Corporate
Description	In this test case, Intel® Boot Guard performs a successful un secure boot of SUT Initial Boot Block (IBB.) Upon successful completion Intel® Boot Guard passes execution to the IBB to continue the boot process with IBB verification.
Objective	This test verifies that the SUT has all the required components: hardware, firmware, ACM and BIOS. Additionally, the SUT is correctly provisioned in manufacturing for the platform to boot <b>without</b> Intel® Boot Guard verification and measuring of the IBB.
Procedure	<p><b>Prepare the SUT Persistent Policy (FPF)</b></p> <ol style="list-style-type: none"> <li>Verify <i>Persistent Policies</i> on the SUT set to default (that is, all '0') or set the <i>No_FVME</i> profile. <ul style="list-style-type: none"> <li>Refer the ME Firmware Bring Up Guide for information on the Intel® Boot Guard related FIT options and setting.</li> </ul> </li> <li>Install the Intel® CSME firmware and BIOS image that are Intel® Boot Guard enabled and are authorized by the key in the Persistent Policy (FPF or NVAR).</li> <li>Install the targeted OS (OS, OS), if not already installed on the SUT.</li> <li>Run MEinfo tool and check for the fields under "FPF" column for FPF contents and "ME" for NVAR contents. Ensure that these matches with what is provisioned during the image creation process.</li> </ol> <p><b>Verify the Boot</b></p> <ol style="list-style-type: none"> <li>Power-off the SUT.</li> <li>Power-on the SUT.</li> <li>Boot to EFI shell and execute TXTBtgInfo.efi.</li> <li>Verify the TXTBtgInfo.efi output to confirm that Intel® Boot Guard has booted as configured to verify and measure the IBB.</li> <li>Boot to the targeted OS.</li> <li>Execute PETS package for Intel® Boot Guard from Remote Console.</li> <li>Verify PETS results should Pass.</li> </ol>



Test ID	BtG_002
Test Pass/Fail Criteria	<p>Test passes, if the SUT:</p> <ul style="list-style-type: none"> <li>Boots fully functional to OS.</li> <li>PETS tests BootGuard_001 and BootGuard_002 should Pass.</li> <li>TXBTgInfo.efi reports that Intel® Boot Guard boot is successful.</li> </ul>

Test ID	BtG_003
Test Case Title	Failed VM Boot fail to Fallback
Mandatory/Optional	Mandatory
Firmware SKU	Consumer / Corporate
Description	In this test case, Intel® Boot Guard performs an unsuccessful verification and measuring of the SUT Initial Boot Block (IBB.) Upon verification failure Intel® Boot Guard performs the fallback behavior per the persistent policy.
Objective	This test verifies that the SUT has all the required components: hardware, firmware, ACM, and BIOS. Additionally, the SUT is correctly provisioned in manufacturing for the platform to handle failure condition per the SUT targeted security objective
Procedure	<p><b>Prepare the SUT Persistent Policy (FPF)</b></p> <ol style="list-style-type: none"> <li>Provision the SUT <i>Persistent Policies</i> (NVAR, if this is development system) to either the <i>VM</i> or <i>FVE</i> or <i>FVME</i> profile. Per testing objective. <ul style="list-style-type: none"> <li><b>The FVME profile usage is not advised for the development or testing environment.</b> In this strictest protection mode, test failure requires BIOS flashing to restore the system.</li> <li>Refer the ME Firmware Bring Up Guide for information on the Intel® Boot Guard related FIT options and settings.</li> </ul> </li> <li>Install the Intel® ME firmware and BIOS image that are Intel® Boot Guard enabled and are authorized by the key in the Persistent Policy (FPF or NVAR).</li> <li>Install the targeted OS (OS), if not already installed on the SUT.</li> <li>Run MEinfo tool and check for the fields under "FPF" column for FPF contents and "ME" for NVAR contents. Ensure that these matches with what is provisioned during the image creation process.</li> </ol> <p><b>Prepare the SUT BIOS</b></p> <ol style="list-style-type: none"> <li>Corrupt the BIOS image by modifying either KM, BPM or IBB to create a BPM signing key mismatch, KM key mismatch or a invalid KM key index.</li> </ol> <p><b>Verify the Boot</b></p> <ol style="list-style-type: none"> <li>Power-off the SUT.</li> <li>Power-on the SUT.</li> <li>Execute PETS package for Intel® Boot Guard from Remote Console.</li> <li>Verify PETS results should Fail.</li> <li>Verify that the platform has failed per the persistent policy. <ul style="list-style-type: none"> <li>Refer to the Intel® Boot Guard for HSW-ULT to details on expected failure handling behavior for the SUT.</li> </ul> </li> </ol>
Test Pass/Fail Criteria	<p>Test passes, if the SUT exhibit the failure condition as expected per the configured profile:</p> <ul style="list-style-type: none"> <li><b>FVE</b> - The platform halts upon verification failure.</li> <li><b>FVME</b> - The platform halts upon verification failure.</li> <li><b>VM</b> - The platform will not halt upon verification failure.</li> </ul>

Test ID	BtG_004
Test Case Title	Platform Public Signing Key Provisioned
Mandatory/Optional	Mandatory
Firmware SKU	Consumer / Corporate
Description	In this test case, the platform public signing key is verified to be provisioned for the platform.



Test ID	BtG_004
Objective	This is intended to be a check of the OEM signing capability and persistent policy provisioning process.
Procedure	<p><b>Prepare the SUT Persistent Policy</b></p> <ol style="list-style-type: none"> <li>Provision the SUT <i>Persistent Policies</i> (NVAR, if this is development system) to either the VM or FVE or FVME profile. Per testing objective. <ul style="list-style-type: none"> <li><b>The FVE profile usage is not advised for the development or testing environment.</b> In this strictest protection mode, test failure requires BIOS flashing to restore the system.</li> </ul> </li> </ol> <p><b>Verify the signing key in the Persistent Policy</b></p> <ol style="list-style-type: none"> <li>Boot the SUT to OS.</li> <li>Run MEInfo.exe.</li> <li>Evaluate the Intel® Boot Guard related fields: <ul style="list-style-type: none"> <li>"FPF" for committed Persistent policies</li> <li>"ME" for NVAR stored Persistent policies</li> </ul> </li> </ol>
Test Pass/Fail Criteria	<p>Test passes, if the SUT:</p> <ul style="list-style-type: none"> <li>Hash of the OEM platform public signing key is correctly provisioned in the Persistent Policy (NVAR or FPF) that is, matches with what is provisioned during the image creation process</li> </ul>

Test ID	BtG_005
Test Case Title	Intel® Boot Guard feature testing using Field programmable Fuse (FPF) values
Mandatory/Optional	Mandatory
Firmware SKU	Consumer / Corporate
Description	<p>In this test case, Intel® Boot Guard performs Intel® Boot Guard feature testing using the values from the FPFs that is, accessing the Intel® Boot Guard profile values from the FPFs instead of the Flash variables that is, NVARs).</p> <p><b>Note:</b> This test can be skipped, if test BtG_001 or BtG_004 are completed using FPF Persistent Policies.</p>
Objective	This test performs and validates all the components used in the Intel® Boot Guard feature that is, hardware, firmware, ACM and BIOS. It also tests that the platform is properly provisioned for Intel® Boot Guard IBB verification and measurement from the Field Programmable Fuses (FPFs).
Procedure	<p><b>Pre-requisite:</b> Perform this test ONLY, when all the tests (BtG_001 to BtG_006) have passed by testing Intel® Boot Guard using the profile values from the NVARs (flash variables).</p> <p><b>Important:</b> The profile selected to be committed into FPFs becomes the final profile, which cannot be altered later. It is not possible to return the system to a pre-test configuration state, once FPF is committed. As such, care must be taken to ensure that the proper test pre-requisites are completed before proceeding.</p> <ol style="list-style-type: none"> <li>Perform the step to commit the Intel® Boot Guard profile values to the FPFs.</li> </ol> <p>This is done automatically after CSME Manufacturing mode is disabled (during the global reset from FPT -closemfn or first boot for Pre-Lock image), if firmware and MCP combination is Production.</p> <p>Or</p> <p>Done by means of a specific FPF MEI command (if combination of firmware and MCP is Pre-production).</p> <p>Below commands can be used for FPF commit on pre-production platforms. (Also refer the CSME Tools guide for the tools usage).</p> <ul style="list-style-type: none"> <li>"FPT -FPFs" - To retrieve the FPF names.</li> <li>"FPT -COMMITFPFS &lt;FPFname&gt;" - To commit values to FPFs one at a time.</li> <li>or "FPT -COMMITFPF All" - To commit values to FPFs all at once.</li> </ul> <ol style="list-style-type: none"> <li>Run MEInfo tool to view the values set in the FPFs and the NVAR-FPF mismatch field. If there is a mismatch, tool indicates it with a FPF mismatch message.</li> <li>Execute the tests (Test ID BtG_001 or BtG_004) based on the profile that is committed on the FPFs.</li> </ol>

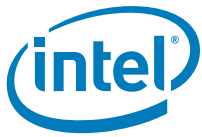


Test ID	BtG_005
Test Pass/Fail Criteria	<p>Test passes, if the SUT:</p> <ul style="list-style-type: none"> <li>The FPF commit command is successfully executed and</li> <li>MEinfo tool O/P shows the correct Intel® Boot Guard profile settings and values under the "FPF" column for each Intel® Boot Guard variable.</li> <li>Further Fail/Pass criteria is the same as criteria mentioned for each of the tests above (test id #BtG_001 or BtG_004).</li> </ul>

Test ID	BtG_006
Test Case Title	BIOS Update Procedure includes Signature Verification
Mandatory/Optional	Optional
Firmware SKU	Consumer / Corporate
Description	This is a manual assessment of the platform BIOS update process to ensure that signature verification is applied to maintain BIOS integrity.
Objective	Confirm the signature authorization structure defined by the Persistent Policy (FPF)->KM->BPM->IBB are maintained in your BIOS update process.
Procedure	1. Confirm with the BIOS Development team that BIOS update process is using proper authorization process to maintain the Intel® Boot Guard authorization structure from FPF->KM->BPM->IBB.
Test Pass/Fail Criteria	<p>Test passes, if the SUT:</p> <ul style="list-style-type: none"> <li>If the BIOS update process contains the proper checks to maintain the Intel® Boot Guard signature authorization structure.</li> </ul>

Test ID	BtG_007
Test Case Title	Service Center's Recovery process for Intel® Boot Guard failed platform
Mandatory/Optional	Optional
Firmware SKU	Consumer / Corporate
Description	This is a manual assessment of the platform service process to ensure that platforms that has failed Intel® Boot Guard verification can be recovered to fully functional state
Objective	Confirm that a service process is established to handle Intel® Boot Guard failure per the configured persistent policy
Procedure	1. Evaluate the platform service process for the failed Intel® Boot Guard scenario. <ul style="list-style-type: none"> <li>Does the service process meet the platform business objective?</li> </ul>
Test Pass/Fail Criteria	<p>Test passes, if the SUT:</p> <ul style="list-style-type: none"> <li>If the platform recovery process meets the business objective.</li> </ul>

Test ID	BtG_008
Test Case Title	BIOS Continues the Chain of Trust
Mandatory/Optional	Optional
Firmware SKU	Consumer / Corporate
Description	This is a manual test to confirm that the BIOS has taken the required steps to protect and continue the chain of trust from Intel® Boot Guard
Objective	Ensure that the SUT maintains the secure boot value proposition, when Intel® Boot Guard completes and when the UEFI Secure Boot protection are implemented in the BIOS



Test ID	BtG_008
Procedure	1. Confirm with the BIOS Development team that IBB and the next boot phase is protecting the integrity of the secure boot on the platform, as recommended in the Intel® Boot Guard BIOS Writer's Guide, when it receives platform controls from the Intel® Boot Guard ACM
Test Pass/Fail Criteria	Test passes, if the SUT: <ul style="list-style-type: none"><li>• If the BIOS team confirms that the proper protection are implemented for the SUT</li></ul>

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## 20 Manufacturing Flow Simulation Test

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### 20.1 Manufacturing Flow Simulation Test

Test ID	Test Case Title	PETS/Manual	Form Factor	Network Factor
MFG_001	Intel® CSME Manufacturing Flow Simulation Test	Manual	MB, DT and WS	LAN+WLAN; WLAN only

Test ID	MFG_001
Test Case Title	Intel® CSME Manufacturing Flow Simulation Test
Mandatory/Optional	Mandatory
Firmware SKU	Corporate
Description	For platform with Intel® ME, it is necessary to perform steps in the manufacturing line to ensure the Intel® CSME is functional and the system is secure, and ready for shipment. The minimum requirements can be met by following the Intel® CSME Manufacturing Reference Flow.
Objective	This test is to run Intel manufacturing tools in manufacturing simulation during the development phase to capture configuration, settings, and other potential issues that customers might encounter later in manufacturing, which will be costly.



Test ID	MFG_001
Procedure	<p><b>Test Environment:</b></p> <ul style="list-style-type: none"> <li>System configuration should be as close as possible to what it is during production/manufacturing phase. Example: WLAN module installed, and so forth.</li> <li>Use the same OS environment as planning to use in the manufacturing line (with all the necessary driver/software installed. Example: Intel® MEI driver for Windows* OS, and so forth.)</li> </ul> <p><b>Test Preparation:</b></p> <ul style="list-style-type: none"> <li>Configure the desired secure boot setting (OEM public key hash, policy, and so forth) for <b>Boot Guard</b> and <b>Intel® PTT Supported [FPF]</b> for PTT and all the variables in MEManuf.xml under <b>EOL VAR TEST</b> session.</li> <li>If this test is conducted on platform with <b>production configuration and ready to run EOM flow</b>, also configure the desired secure boot setting (OEM public key hash, policy, and so forth) for <b>Boot Guard</b> and <b>Intel® PTT Supported [FPF]</b> for PTT in MEManuf.xml under <b>EOL CONFIG Test</b> session.</li> </ul> <p><b>Test Procedure:</b></p> <ol style="list-style-type: none"> <li>Use the version of FPT and, MEManuf executable suitable for the chosen OS environment (located in the latest Intel® CSME kit) to simulate atleast the Intel® CSME Manufacturing reference flow (Below steps).</li> <li>If using pre-lock (the descriptor Master Access permission set to Intel recommended production value during image preparation), do only steps 5, 6, 7, 8 and 11.</li> <li>Reprogram the image currently on board (Example: Image.bin).             <ul style="list-style-type: none"> <li>Example: FPTW64.exe -f image.bin</li> </ul> </li> <li>Reset Intel® CSME and Host after program successfully.             <ul style="list-style-type: none"> <li>Example: FPTW64.exe -greset</li> </ul> </li> <li>For platform supporting AMT (if platform does not supporting AMT, skip this step), firstly ensure supported Intel WLAN module is installed. Then perform WLAN µcode update using the Intel® CSME binary (Example: ME.bin) from Firmware kit.             <ul style="list-style-type: none"> <li>Example: FWUpdLcl64.exe -f ME.bin -partid wcod</li> </ul> </li> <li>Verify Intel® CSME (for non-AMT capable only w/ Auto BIST disabled).             <ul style="list-style-type: none"> <li>Example: MEManufWin64.exe</li> <li>Example (option): MEManufWin64.exe -f MEManuf.xml (use the MEManuf.xml configuration file configured during preparation).</li> </ul> </li> <li>Verify Intel® CSME (for AMT capable w/ Auto BIST enabled)             <ul style="list-style-type: none"> <li>If <b>Automatic Build In Self Test</b> is enabled in FIT during preparation, run MEManuf once to get full verification result.                     <ul style="list-style-type: none"> <li>Example: MEManufWin64.exe.</li> <li>Example (option): MEManufWin64.exe -f MEManuf.xml (use the MEManuf.xml configuration file configured during preparation).</li> </ul> </li> <li>If <b>Automatic Build In Self Test</b> is disabled in FIT during preparation, run MEManuf twice to get full verification result. After first running 1<sup>st</sup> time MEManuf, user will observe a power cycle, which is because system entering CSME BIST under M3 mode and save the result in SPI. After running 2<sup>nd</sup> MEManuf, it will get the full validation result.                     <ul style="list-style-type: none"> <li>Example: MEManufWin64.exe.</li> <li>Example (option): MEManufWin64.exe -f MEManuf.xml (use the MEManuf.xml configuration file configured during preparation).</li> </ul> </li> </ul> </li> <li>Check Boot Guard, PTT, and all the variables match with setting configured in FIT.             <ul style="list-style-type: none"> <li>Example: MEManufWin64.exe -EOL var -f MEManuf.xml (use the MEManuf configuration file configured during preparation).</li> </ul> </li> </ol>





Test ID	MFG_001
	<p>10. Set Intel® CSME manufacturing done bit and descriptor Master Access permission to Intel recommended production value, then perform global reset to make sure Intel® CSME manufacturing mode is disabled</p> <ul style="list-style-type: none"> <li>Example: FPTW64.exe -closemnf -y</li> </ul> <p><b>Note:</b> PDR, EC BIOS or legacy addition could be used following FPTW64.exe -closemnf -y to allow various CPU/BIOS read/write access setting based on customer need. Check System Tool User Guide for more detail.</p> <p>11. Perform end of line check on Intel recommended default test item and also Boot Guard, PTT, and all the configuration check.</p> <ul style="list-style-type: none"> <li>Example: MEManufWin64.exe -EOL (It runs Intel recommended default test) or</li> <li>Example (option): MEManufWin64.exe -EOL config -f MEManuf.xml (use the MEManuf.xml configuration file configured during preparation more sub tests enabled).</li> </ul> <p><b>Note:</b> It is highly recommended you create your own script file to automatically run the above steps in order to better simulate the manufacturing flow.</p>
<b>Test Pass/Fail Criteria</b>	<p>Pass only, when all the tools run above return pass result.</p> <p><b>Note:</b> When encounter failure, check:</p> <ul style="list-style-type: none"> <li>CRB test result in Compliance kit.</li> <li>Intel® CSME firmware release notes for known issues.</li> </ul>

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## 21 Intel® ISH Firmware (FW) Compliancy

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This section provides the ISH FW test (performed using PETS) from the image creating stage to OS level, in each stage checking the ISH FW and sensors status.

Platform Enablement Suite (PETS) is a test design application and execution engine that enable users to design and run work flows on various devices. It is used for sensor Compliancy testing.

**Prerequisites:**

- The PDT Editor tool can be found in the ISH FW Kit.
- The Sensor Viewer Tool can be found in the ISH FW Kit.



## 21.1 Test Coverage Summary

Test ID	Test Case Title	Target OS	Automated/ Manual	Mandatory/ Optional
ISS_TST_01	Sensor communication test	Windows*	PETS	Mandatory
ISS_TST_02	Sensor data check	Windows*	Manual	Mandatory
ISS_TST_03	ISH FW loading and execution	Windows*	Manual	Mandatory
ISS_TST_04	Intel® SensorViewer test	Windows*	Manual	Mandatory
ISS_TST_05	Test system sensor noise and effects on sensor algorithms	Windows*	PETS	Optional
ISS_TST_06	Test worst case system interference and effect on sensor algorithms	Windows*	PETS	Optional
ISS_TST_07	Test system performance and effective calibration under a specific range of movements	Windows*	PETS	Mandatory, if motion sensors are present
ISS_TST_08	Barometer (pressure) sensor sanity test	Windows*	Semi-Automated (PETS)	Mandatory, if a barometer is present
ISS_TST_09	Light sensor (ALS) accuracy test	Windows*	Semi-Automated (PETS)	Mandatory
ISS_TST_10	Light sensor (ALS) angular response test	Windows*	Semi-Automated (PETS)	Mandatory
ISS_TST_11	360 hinge accuracy test with second accelerometer	Windows*	Semi-Automated (PETS)	Mandatory only, if the second accelerometer is present
ISS_TST_12A	PLM functionality verification in S0	Windows*	Manual	Mandatory only, if the second accelerometer is present
ISS_TST_12B	PLM functionality verification with power transitions	Windows*	Manual	Mandatory only, if the second accelerometer is present
ISS_TST_13	Heading sensor accuracy and drift test	Windows*	Semi-Automated (PETS)	Mandatory only, if a magnetometer sensor is present.
ISS_TST_14	Intel Integrated Sensor Solution power states	Windows*	PETS	Mandatory
ISS_TST_15	Sensor activity contexts	Windows*	Semi-Automated (PETS)	Optional. Perform the test if the system holds motion sensors.
ISS_TST_16	Sensor terminal contexts	Windows*	Semi-Automated (PETS)	Optional. Perform the test if the system holds motion sensors.
ISS_TST_17	Sensor gesture contexts	Windows*	Semi-Automated (PETS)	Optional. Perform the test if the system holds motion sensors.
ISS_TST_18	Wake on shake test	Windows*	Manual	Mandatory, if wake on shake is implemented
ISS_TST_19	Step counting test	Windows*	Manual	Optional



## 21.2 Sensor Communication Test

Test ID	ISS_TST_01
Test Case Title	Sensor communication test
Mandatory/Optional	Mandatory
Description	This test is checking basic communication with the ISH and ISH FW can be read.
Objective	Verify communication with the ISH sensors
Windows*/Android Procedure	<ol style="list-style-type: none"><li>1. Boot the platform to AOS/WOS/EFI shell.</li><li>2. From elevated command line run the ISSUtil Tool: "ISSUtil.exe -BIST -test 0 -verbose" "ISSUtil.exe -BIST -test 1 -verbose" "ISSUtil.exe -BIST -test 2 -verbose" "ISSUtil.exe -BIST -test 3 -verbose"</li></ol>
Test Pass/Fail Criteria	Test will pass, if each of the tests were completed successfully without any errors.

## 21.3 Sensor Data Check

Test ID	ISS_TST_02
Test Case Title	Sensor data check
Mandatory/Optional	Mandatory
Description	In the PDT Editor, user is configuring the sensors drivers, I <sup>2</sup> C data and calibration data. This test checks that those sensors information were configured correctly in PDT table.
Objective	Check the sensor data in the PDT editor to make sure it is compliant with the board.
Windows* Procedure	<p>Verify the sensors information in the PDT Editor:</p> <ol style="list-style-type: none"><li>1. Open the full SPI image in the FITC tool (Decompose it).</li><li>2. In the FITC tool folder, a folder will be created with the name of the image that was decomposed using FITC.</li><li>3. Using the PDT Editor open the PDT table from that image, it is located under: FITC\image_name\Decomp\PdtBinary.bin.</li><li>4. In the PDT Editor, verify that each of the sensors configured with the rights settings.</li></ol>
Test Pass/Fail Criteria	Test will pass, if the sensors information were configured correctly in the PDT Editor.

## 21.4 ISH FW Loading and Execution

Test ID	ISS_TST_03
Test Case Title	ISH FW version check
Mandatory/Optional	Mandatory
Description	This test is checking basic communication with the ISH and the ISH FW can be read.



Test ID	ISS_TST_03
Objective	Verify that ISH is responsive and that ISH FW can be read
Windows* Procedure	<ol style="list-style-type: none"> <li>1. Boot the platform to AOS/WOS shell.</li> <li>2. From elevated command line run the ISSUtil Tool: ISSUtil.exe -INFO</li> <li>3. In the tool output, check that: <ol style="list-style-type: none"> <li>a. ISH Status is "responding"</li> <li>b. ISH FW Version can be read and is as follow: "5.x.x.XXXX" (X- Stand for, do not care)</li> </ol> </li> </ol>
Test Pass/Fail Criteria	Test will pass, if ISH status is "responding" and ISH FW can be read.

## 21.5 Intel® Sensor Viewer Test

Test ID	ISS_TST_04
Test Case Title	Intel® SensorViewer test
Mandatory/Optional	Mandatory
Description	This test is checking that the ISH sensors are ready for use
Objective	Verify that the ISH sensors are ready for use and that data is received from the sensor
Windows* Procedure	<ol style="list-style-type: none"> <li>1. Boot the platform to Windows*</li> <li>2. Open the Intel® SensorViewer and switch to "Desktop API" in Settings.</li> <li>3. For each sensor on the platform check that the state is "Ready" and that data is received, this may require a trigger of the sensor event, for example for the orientation sensor the platform need to be moved in order to receive data in the Intel® SensorViewer.</li> </ol>
Test Pass/Fail Criteria	Test passes in the sensor viewer, all of the sensors state is "Ready" and the data is received for each of the sensors

## 21.6 Test System Sensors

### 21.6.1 Sensor Noise and Error Levels

Following is a table of sensor noise and error levels that will be monitored by some tests within the compliance guide. These numbers should be measured after calibration has been applied.



**Table of measured values from the physical sensor:**

	Maximum Offset per Axis Compared to Average	Noise per Axis
Accelerometer	30 mg	10 mg
Magnetometer	50 mGauss	10 mGauss
Gyroscope	15 dps	0.2 dps

**Table of measured values from the IISS algorithms (static—no movement):**

	Maximum Error	Average Error	STD
Inclinometer	2 degrees	2 degrees	0.75 deg
3D Compass	2 degrees	2 degrees	0.75 deg
3D Gyro	1.0 dps	1.0 dps	0.2 dps
3D Accelerometer	40 mg	40 mg	

**Note:** 3D Gyroscope and 3D Accelerometer values are “per axis.



## 21.6.2 Test System Sensor Noise and Effects on Sensor Algorithms

Test ID	ISS_TST_05
Test Case Title	Test system sensor noise and effects on sensor algorithms
Mandatory/Optional	Optional
Description	<p>The performance of the ISS sensor algorithms may degrade, if the noise levels are too high. This test measures the noise levels on each sensor at when the system is at rest to indicate the likelihood of an impact to overall system sensor performance.</p> <p>The causes for higher noise levels can include selecting a poor quality sensor or could be related to system interference from other components (i.e. CPU) or due to PCB design issues.</p> <p>The test also measures any variance seen at the output of the sensor algorithms to also indicate unexpected variance (i.e. e-compass moving or drifting) that would also indicate a performance issue with the system.</p>
Objective	Gather statistical data on both sensor data input (RAW sensor data) and data output of sensor algorithms.
Procedure	<p>Automated (PETS)</p> <p>Initial state of the SUT should be S0.</p> <p>If the system is a 2-in-1 device, the test should start with the system in the "PC" context (screen facing user with keyboard facing-up on the table).</p> <p><b>Intel® Platform Enablement Test Suite (Intel® PETS) will perform the following steps:</b></p> <ol style="list-style-type: none"> <li>1. Gather RAW and virtual sensor data over a designated period (i.e. 10s). Data will be gathered from all present physical sensors on platform and all available sensor SW drivers.</li> <li>2. If the System is a 2-in-1 device, convert it into a tablet form-factor (screen on top of keyboard or detached from it_ and repeat step #1).</li> </ol>
Test Pass/Fail Criteria	<p>Test passes, if all sequences are shown:</p> <ol style="list-style-type: none"> <li>1. RAW sensor statistical data shows noise levels within acceptable ranges.</li> <li>2. Data output from sensor algorithms do not show movement or other performance issues when the system is at rest.</li> </ol> <p>For #1 and #2 - the tool refers to the pass/fail levels placed in the section "Sensor Noise and Error Levels".</p> <p>In the case that the test results are above the pass/fail limits - the tests will raise a "warning" to the user.</p>



### 21.6.3 Test Worst Case System Interference and Effect on Sensor Algorithms

Test ID	ISS_TST_06
Test Case Title	Test worst case system interference and effect on sensor algorithms
Mandatory/Optional	Optional
Description	<p>The system may contain noise sources that cause the worst system sensor performance issues, when enabled. This can include the speakers, CPU, GPU, and others.</p> <p>The goal of this test is to measure both physical RAW sensor data and the outputs seen at the output of the sensor algorithms to understand, if increased noise levels (or movement) are seen, when typical noise sources are operated at their worst condition.</p>
Objective	Determine the worst-case system interference that can be seen on the sensors. Measures both interference seen on RAW sensor data and effect to virtual sensors.
Procedure	<p>Semi-Automated (PETS)</p> <p>Initial state of the SUT should be S0. The audio sub-system should be fully functional.</p> <p>If the system is a 2-in-1 device, the test should start with the system in the "PC" context (screen facing user with keyboard facing-up on the table).</p> <p><b>Intel® Platform Enablement Test Suite (Intel® PETS) will perform the following steps:</b></p> <ol style="list-style-type: none"><li>1. The system exercises known interference sources to refer, if they influence on the system. Data should be gathered at each step for at least 10 seconds. The interference sources include:<ul style="list-style-type: none"><li>— Outputting speaker data at maximum frequency with a tonal frequency of 100 Hz to 2000 Hz (100 Hz/step). This should be operated at maximum volume.</li><li>— CPU operated at minimum and maximum load.</li><li>— GPU operated at minimum and maximum load.</li><li>— Turn the computer screen on/off.</li></ul></li></ol> <p>For each sample data sample - the system will gather RAW and virtual sensor data. The noise levels and any movement should be recorded and compared to pass/fail levels.</p> <ol style="list-style-type: none"><li>2. The system exercises known interference sources to refer, if they have influence on the system. Data Should be gathered at each step.</li><li>3. If the system is a 2-in-1 device, convert it into a tablet form-factor (detached/screen on to of keyboard) and repeat steps #1 and #2.</li></ol>
Test Pass/Fail Criteria	<p>Test passes, if all sequences are shown:</p> <ol style="list-style-type: none"><li>1. RAW sensor statistical data shows noise levels within acceptable ranges.</li><li>2. Data output from sensor algorithms do not show movement or other performance issues when the system is at rest.</li></ol> <p><b>Note:</b> For #1 and #2 - the tool refers to the pass/fail levels placed in the section "Sensor Noise and Error Levels".</p> <p><b>Note:</b> In the case that the test results are above the pass/fail limits - the tests raises a "warning" to the user.</p>





## 21.7 Test System Performance and Effective Calibration Under a Specific Range of Movements

<b>Test ID</b>	<b>ISS_TST_07</b>
<b>Test Case Title</b>	Test system performance and effective calibration under a specific range of movements
<b>Mandatory/Optional</b>	Optional. Mandatory, if motion sensors are present
<b>Description</b>	The data quality of the sensor algorithms can be impacted by a number of factors (Example: Inaccurate sensor calibration). This test moves the sensor across a number of positions and tests that all pass-through sensors and virtual algorithms respond as expected.
<b>Objective</b>	Tests sensor configuration for correct orientation and data during both rest and movement.
<b>Procedure</b>	<p>Semi-Automated (PETS) Initial state of the SUT should be S0. The system should have run through the ISS sensor calibration procedure with the calibration data stored and used on the system. The system should be configured in a tablet context. If the device is a 2- in-1, suggest repeating in the PC form-factor with the system placed in a box that can be moved in the pattern shown below. The user is asked to run through the following movements to test the gyroscope:</p> <p><b>Test Sub-Section A: Gyroscope Z-Axis:</b></p> <ol style="list-style-type: none"> <li>1. Place the system flat on the table with the screen facing upwards.</li> <li>2. Rotate the system clockwise - the gyroscope should identify a negative angular velocity on the Z-axis.</li> <li>3. Rotate the system counter-clockwise - the gyroscope should identify a positive angular velocity on the Z-axis.</li> </ol> <p><b>Test Sub-Section B: Gyroscope X-Axis:</b></p> <ol style="list-style-type: none"> <li>1. Place the system face-up on the table with the screen facing towards you in the "portrait" position.</li> <li>2. Rotate the system clockwise - the gyroscope should identify a positive angular velocity on the Y-axis.</li> <li>3. Rotate the system counter-clockwise - the gyroscope should identify a negative angular velocity on the Y-axis.</li> </ol> <p><b>Test Sub-Section C: Gyroscope Y-Axis:</b></p> <ol style="list-style-type: none"> <li>1. Place the system face-up on the table with the screen facing towards you in the "landscape" position. The right-hand side of the screen should be pointing upwards.</li> <li>2. Rotate the system clockwise - the gyroscope should identify a negative angular velocity on the X-axis.</li> <li>3. Rotate the system counter-clockwise - the gyroscope should identify a positive angular velocity on the X-axis.</li> </ol> <p><b>Test Sub-Section D: Accelerometer:</b> Place the system in the following positions:</p> <ol style="list-style-type: none"> <li>1. Flat on the table facing up. (Z-UP) The accelerometer should read (0,0,- g0).</li> <li>2. Flat on the table facing down. (Z-down) The accelerometer should read (0,0,g0).</li> <li>3. Facing the user on the table in landscape mode. (X-DOWN) The accelerometer should read (g0,0,0).</li> <li>4. The same position as the previous step but now placed up-side-down. The accelerometer should read (-g0,0,0).</li> <li>5. Facing the user on the table in portrait mode (Y-DOWN). The accelerometer should read (0,-g0,0).</li> <li>6. The same position as the previous step but now placed up-side-down. The accelerometer should read (0,g0,0).</li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>Test passes, if all sequences are shown:</p> <p><b>For the gyroscope:</b> The correct direction was recorded from the gyroscope, when moving the system.</p> <p><b>For the accelerometer:</b> The accelerometer reading was correct within a 5 degree error.</p>



## 21.8 Barometer (Pressure) Sensor Sanity Test

Test ID	ISS_TST_08
Test Case Title	Barometer (pressure) sensor sanity test
Mandatory/Optional	Optional. Mandatory, if a barometer is present
Description	This test confirms the barometer (pressure) sensor is working correctly on the system.
Objective	Test that the barometer sensor is present and responsive to changing elevations
Procedure	Semi-Automated (PETS) Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW. 1. Lift the system to a height of 1.5-2.0 meters. Wait 10 seconds. 2. Place the system on the ground. Wait 10 seconds. For each sample data sample - the system gathers RAW and virtual sensor data.
Test Pass/Fail Criteria	Test will pass, if all sequences show: The pressure sensor recorded a change in altitude relative.



## 21.9 Light Sensor (ALS) Accuracy Test

<b>Test ID</b>	<b>ISS_TST_09</b>
<b>Test Case Title</b>	Light sensor (ALS) accuracy test
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	This test reviews the accuracy of the ambient light sensor after it is characterized.
<b>Objective</b>	<p>The ALS accuracy may be affected by a number of factors including the mechanical design of the housing, cover glass, and the calibration applied within the ISS system.</p> <p>The test is meant to test the accuracy of the ALS after it is calibrated.</p>
<b>Procedure</b>	<p>Semi-Automated (PETS)</p> <p>Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW.</p> <p>System is in a dark room or placed within a lighting tent (made out of diffused lighting material) and covered with a black cloth. The following equipment should be used:</p> <ol style="list-style-type: none"> <li>1. Tunable light source that can emit halogen light.</li> <li>2. Light meter to measure the lighting level incident on the SUT.</li> </ol> <p>The light meter is placed next to the system ALS sensor. The system should be orientated orthogonal to the light source.</p> <ol style="list-style-type: none"> <li>1. Light source is tuned to maximum amplitude. ALS reading should be displayed on the screen. Check that the received ALS value is within +/- 10% of the recorded light meter value. The screen brightness should appear not too bright or too dark.</li> <li>2. Lower the light source to mid-way. Compare again the difference between the ALS and light meter value. The screen brightness should adjust such that it is not too bright or too dark relative to the ambient light level.</li> <li>3. Tune light source to the lowest level. Compare again the difference between the ALS and light meter value. The screen brightness should adjust such that it is not too bright or too dark relative to the ambient light level.</li> <li>4. (optional) If a fluorescent light source is available, expose the system to the same "low" light level seen in the previous step. Check that the ALS light levels are correct relative to the light meter. And that the screen brightness is not too bright or too dark.</li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>Test will pass, if all sequences show:</p> <p>For all light levels tested - the ALS is correct within +/- 10%.</p>



## 21.10 Light Sensor (ALS) Angular Response Test

Test ID	ISS_TST_10
Test Case Title	Light sensor (ALS) angular response test
Mandatory/Optional	Mandatory
Description	<p>This test is used for the angular response of the ALS sensor to determine, if it falls within the requirements of the MSFT HW certification guidelines. MSFT* request that the light response does not fall by more than 50%, when changing the angle of incident light from 0 to 35 degrees.</p> <p>Issues can occur with the sensor angular response due to the light sensor cavity/hole design or other materials covering the light sensor.</p>
Objective	Confirm that the ambient light sensor angular response is greater than 50% at a 35 degree angle of incidence.
Procedure	<p>Semi-Automated (PETS)</p> <p>Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW. System is in a dark room or placed within a lighting tent (made out of diffused lighting material) and covered with a black cloth. The following equipment should be used:</p> <ol style="list-style-type: none"><li>1. Tunable light source that can emit halogen light.</li><li>2. Light meter to measure the lighting level incident on the SUT. The light meter is placed next to the system ALS sensor.</li></ol> <p>The system should be orientated orthogonal to the light source. Before starting the test:</p> <ol style="list-style-type: none"><li>1. The system should be directly facing the light source.</li><li>2. The ALS reading should be within +/- 10% of the value read by the light meter. Recommended target lighting is 100 lux with the ALS reading 90-110 lux.</li></ol> <p>When running the test:</p> <ol style="list-style-type: none"><li>1. Rotate the system so that the ALS is at a 35 degree angle to the incident light without changing the distance.</li></ol>
Test Pass/Fail Criteria	<p>Test will pass, if all sequences show:</p> <p>The recorded light level of the ALS does not fall more than 50%.</p>



## 21.11 360 Hinge Accuracy Test with Second Accelerometer

Test ID	ISS_TST_11
Test Case Title	360 hinge accuracy test with 2 <sup>nd</sup> accelerometer
Mandatory/Optional	Optional. Mandatory if the 2 <sup>nd</sup> accelerometer is present.
Description	Placing an accelerometer both in the base and lid of the system design will enable the system to determine the angle between the lid and base. This algorithm (also called a virtual protractor) communicates the system how to operate, if the system is closed, in a PC use case, or if the lid is flipped such that the system is in a tablet mode. The goal of this test is to confirm that the lid angles are reported correctly.
Objective	Confirm that the angle between the base and lid is accurately reported.
Procedure	Semi-Automated (PETS) Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW. Place the system on a flat table. Record the reported angle over a 5 second period. <ol style="list-style-type: none"> <li>0 degrees. Lid closed (screen facing keyboard).</li> <li>90 degrees. Screen open and facing the user. Screen and keyboard are orthogonal with user seeing screen and keyboard at the same time.</li> <li>180 degrees. Screen and keyboard both facing up.</li> <li>270 degrees. Screen and keyboard are orthogonal. The user cannot see the screen and keyboard at the same time.</li> <li>360 degrees. System flat on table. The screen is facing up and the keyboard is facing down.</li> </ol>
Test Pass/Fail Criteria	Test will pass, if all sequences show: The detected angle should be within a $\pm 10$ degrees of accuracy. Over the 5 seconds, the variance of the angle should have been less than $\pm 5$ degrees.

## 21.12 PLM Functionality Verification

Test ID	ISS_TST_12A
Test Case Title	PLM functionality verification without system power transitions
Mandatory/Optional	Optional. Mandatory, if PLM is implemented
Description	Test requires to go through the system modes configured in the PDT Configuration by adjusting the system position per each mode definition, while verifying and comparing the actual data reported by the PLM algorithm.
Objective	To verify proper configuration and functionality of the PLM algorithm on customer system in S0
Procedure	<ol style="list-style-type: none"> <li>Boot the system to OS.</li> <li>Set the system in a first position according to the last PLM Mode configured in the PDT Configuration file.</li> <li>User should manually acknowledge when the system is placed in the position as requested in previous step.</li> <li>User should verify if the actual system position reported by the PLM algorithm is aligned to what user confirmed.</li> <li>Continue to the next PLM Mode looping steps 2-4.</li> </ol>
Test Pass/Fail Criteria	Test will pass, only if all PLM Modes are matching the actual system position. i.e. all PLM Modes are successfully matched.



Test ID	ISS_TST_12B
Test Case Title	PLM functionality verification with system power transitions
Mandatory/Optional	Optional. Mandatory, if PLM is implemented
Description	Test requires to make system power transitions, while going through the system modes as configured in the PDT Configuration file. User is requested to adjust the system position as defined by each Platform Mode, while verifying and comparing the actual data reported by the PLM algorithm to the system position reported by the user.
Objective	To verify proper configuration and functionality of the PLM algorithm on customer system, while involving system power transition
Procedure	<ol style="list-style-type: none"><li>1. Boot the system to OS.</li><li>2. Set the system in a first position according to the last PLM Mode configured in the PDT Configuration file.</li><li>3. User should manually acknowledge, when the system is placed in the position as requested in previous step.</li><li>4. User should verify if the actual system position reported by the PLM algorithm is aligned to what user confirmed.</li><li>5. Change the system state to S3.</li><li>6. User set the system in the next position according to the last PLM Mode configured in the PDT Configuration file.</li><li>7. User should manually acknowledge, when the system is placed in the position as requested in previous step.</li><li>8. User to wake the system to OS/S0.</li><li>9. User should verify, if the actual system position reported by the PLM algorithm is aligned to what user confirmed.</li><li>10. Continue to the next PLM Mode looping steps 5-9.</li></ol>
Test Pass/Fail Criteria	Test passes, only if all PLM Modes are matching the actual system position. i.e. all PLM Modes are successfully matched.



## 21.13 Heading Sensor Accuracy and Drift Test

Test ID	ISS_TST_13
Test Case Title	Heading sensor accuracy and drift test
Mandatory/Optional	Optional. Mandatory, if a magnetometer sensor is present.
Description	The e-compass using the system accelerometer and magnetometer can experience errors for multiple reasons including incorrect sensor calibration. This test is designed to show that the heading accuracy is correct in a number of angles/directions.
Objective	Confirm that the system reports the correct heading accuracy.
Procedure	<p>Semi-Automated (PETS)</p> <p>Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW.</p> <p>If the system is a 2-in-1 device, the test should start with the system in the "PC" context (screen facing user with keyboard facing-up on the table).</p> <p>To test that the system is free of external magnetic influence:</p> <ol style="list-style-type: none"> <li>1. Gather data from the magnetometer (@ rest) - confirm that the magnetometer is not moving more than 1-2 degrees while the system remains still.</li> <li>2. Move the system 0.5 meters in each direction. Confirm that the compass reading does not change more than 1-2 degrees.</li> </ol> <p><b>Intel® Platform Enablement Test Suite (Intel® PETS) will perform the following steps:</b></p> <p>Test System Flat on Table (Z-UP)</p> <p>With a compass, place the system facing north on a flat table:</p> <ol style="list-style-type: none"> <li>1. Start with the system placed facing north and flat on the table.</li> <li>2. Rotate the system to 90 degrees from north</li> <li>3. Rotate the system to 180 degrees from north</li> <li>4. Rotate the system to 270 degrees from north</li> <li>5. Rotate the system to face north</li> </ol> <p><b>Note:</b> If system is a 2-in-1 device, convert it into a tablet form-factor (detached / screen on top of keyboard) and repeat this test sub-section.</p>
Test Pass/Fail Criteria	Test will pass, if all sequences show: System heading error should not exceed 10 degrees at any rest position.

## 21.14 Intel® Integrated Sensor Solution Power States

Test ID	ISS_TST_14
Test Case Title	Intel® Integrated Sensor Solution power states
Mandatory/Optional	Mandatory
Description	The purpose of this test is validate that the IISS is alive after system power transitions.



Test ID	ISS_TST_14
Objective	IISS is alive without errors after power transitions.
Procedure	<p>Automated (PETS)</p> <p>Initial state of the SUT should be S0 (OS up) with the IISS configured in the system FW.</p> <p>Before running this test record the output of each IISS algorithm seen at the OS level. And confirm that the full sensor functional test has passed.</p> <p>Run the following power transitions from S0:</p> <ol style="list-style-type: none"><li>1. Resume from S3 on AC + DC</li><li>2. Resume from S3 on DC</li><li>3. Resume from S4 on AC + DC</li><li>4. Resume from S4 on DC</li><li>5. Resume from S5 on AC + DC</li><li>6. Resume from S5 on DC</li><li>7. Resume from DeepS3* (Optional if FW image supports DeepSx)</li><li>8. Resume from DeepS4* (Optional if FW image supports DeepSx)</li><li>9. Resume from DeepS5* (Optional if FW image supports DeepSx)</li><li>10. Resume from G3 on AC + DC</li><li>11. Resume from G3 on DC</li><li>12. Resume from G3 with no coin battery (if coin battery exists)</li><li>13. Resume after system reset (cold reset, HW RST button)</li><li>14. Resume after system reboot (warm reset, host based)</li></ol> <p>After each system resume - check the output of each IISS algorithm seen at the OS level. And confirm that the full sensor functional test has passed.</p> <p>** To test DeepSx the user must enter the BIOS menu: 'BIOS' -&gt; 'Intel Advanced Menu' -&gt; 'PCH-IO Configuration -&gt; 'DeepSx Power Policies' -&gt; 'Enabled in S3-S4-S5'</p> <p>For manual test - the sensor diagnostic tool can be used to read the output of the sensors. The sensor functional test can be run with the ISS Utility tool ("ISSUtil.exe -BIST -test 3").</p>
Test Pass/Fail Criteria	<p>Test will pass, if all sequences show:</p> <ol style="list-style-type: none"><li>1. System functional test records a "pass" after the system resumes to S0.</li><li>2. The algorithm outputs are within a +/-10% range of their previous values prior to the system power transition.</li></ol> <p><b>Note:</b> If the sensor or sensor micro-driver does not support the "built in functional test" (test level 3), then the test will return a warning to the user.</p>





## 21.15 Sensor Activity Contexts

Test ID	ISS_TST_15
Test Case Title	Sensor activity contexts
Mandatory/Optional	Optional. Perform the test, if the system holds motion sensors.
Description	The IISS contains activity context algorithms that can determine the user activities. This includes determining if the user is (1) sitting, (2) walking, or (3) running [at a safe speed]. These tests will confirm, if the sensor activity contexts algorithms within the IISS are working properly.
Objective	Confirm that the system will detect the system user activity contexts.
Procedure	Semi-Automated (PETS) Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW. Place the system on a flat table. If the system is a 2-in-1 system, start in the tablet form factor. <ol style="list-style-type: none"> <li>1. Leave the SUT on desktop and wait for 5 minutes. The system should detect that the system is sedentary.</li> <li>2. Pick up the SUT and begin walking with it. The system should detect that user is walking with the system.</li> <li>3. Start lightly running with the SUT. The system should detect that user is running with the system.</li> </ol>
Test Pass/Fail Criteria	Test will pass, if all sequences show: The system accurately detected the user contexts.

## 21.16 Sensor Terminal Contexts

Test ID	ISS_TST_16
Test Case Title	Sensor Terminal Contexts
Mandatory/Optional	Optional. Perform the test, if the system holds motion sensors.
Description	The IISS contains terminal context algorithms that can determine, how the user is holding the system. This includes determining if the system is held <ol style="list-style-type: none"> <li>1. Face up / down,</li> <li>2. Portrait up / down, or</li> <li>3. Landscape left / right.</li> </ol> These tests will confirm, if the sensor terminal contexts algorithms within the IISS are working properly.
Objective	Confirm that the system will detect the system user terminal contexts.
Procedure	Semi-Automated (PETS) Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW. Place the system on a flat table. If the system is a 2-in-1 system, start in the tablet form factor. <ol style="list-style-type: none"> <li>1. Place the system face up and face down.</li> <li>2. Place the system portrait up and portrait down.</li> <li>3. Place the system landscape left and landscape right.</li> </ol>
Test Pass/Fail Criteria	Test will pass, if all sequences show: The system accurately detected the terminal contexts.



## 21.17 Sensor Gesture Contexts

Test ID	ISS_TST_17
Test Case Title	Sensor gesture contexts
Mandatory/Optional	Optional. Perform the test, if the system holds motion sensors.
Description	The IISS contains gesture context algorithms that can determine, how the user is holding the system. This tests will confirm, if the sensor gesture contexts algorithm within the IISS are working properly.
Objective	Confirm that the system will detect the system user gesture contexts.
Procedure	Semi-Automated (PETS) Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW. Place the system on a flat table. If the system is a 2-in-1 system start in the tablet form factor. 1. Lift the system from the table and look at the system.
Test Pass/Fail Criteria	Test will pass, if all sequences show: The system accurately detected the terminal contexts.

## 21.18 Wake on Shake Test

Test ID	ISS_TST_18
Test Case Title	Wake on shake test
Mandatory/Optional	Mandatory
Description	Wake on different events is a mandatory feature in Windows*10. As such a test that will focus on the ability to wake the system from S0i3 (CS) is a must.
Objective	Test that ISH can send a wake event to Win OS and the OS waken from S0i3 to S0
Procedure	1. Make sure that system is set in CS state (S0ix). 2. Make sure that shake event is defined in PDT and in Windows* (use SDT to check it). 3. Shake the system. 4. Windows* should wake and log on screen should appear. 5. Repeat the test 3 times. 6. There is a timeout (usually 2 minutes) until Windows* will go to SC again, unless the configuration of the specific copy of Windows* on the device set the timer to a different value.
Test Pass/Fail Criteria	Test will pass, if Windows* awakes all 3 times



## 21.19 Step Counting Test

<b>Test ID</b>	<b>ISS_TST_19</b>
<b>Test Case Title</b>	Step counting test
<b>Mandatory/Optional</b>	Optional, if the step counting is operational
<b>Description</b>	Step counting is a standard virtual sensor that is being exposed in Windows* 10. The goal is to test that step counting sensor is working correctly.
<b>Objective</b>	Test that step counting sensor is working correctly and measure user steps
<b>Procedure</b>	<p>Initial state of the SUT should be S0 (OS up). The ISS should be configured in the system FW.</p> <p>User should hold the tablet/notebook, while he/she stands.</p> <p>User should check SDT or any other sensor data report SW on the OS for the current number of step counter.</p> <p>User should start walking while counting his/her steps in a straight line.</p> <p>After counting 50 steps user should stop.</p> <p>User should compare the 50 steps that he/she made to the number of steps shown on the software (after doing the needed math of subtracting the initial number of steps).</p> <p><b>Remark:</b> The step counter starts acting of 10 seconds of stepping, so tests that will take 10 seconds or will not be able to check the counter.</p>
<b>Test Pass/Fail Criteria</b>	Amount of steps made by the user should be identical to step counter number on the SDT or any other sensor data SW.

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## 22 Platform Controller Hub (PCH) Soft Strap Configuration

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### Overview:

The Intel® PCH Soft Straps are load into the appropriate strapping registers within the PCH at boot time from the SPI flash device's Flash Descriptor. Some of the features within the PCH are configurable through the PCH Soft Straps such as the Flexible I/O, SMLINK, GbE, and Intel® ME. The PCH Soft Straps are configure using the FIT tool. Refer to the SPI Programming Guide for the details description on all the available PCH Soft Straps.

All the test case in this chapter are currently cover automatically by PETS on the target system at runtime. Static checking on the image created by FIT is not supported.

### Tools for Testing:

- **Intel® Platform Enablement Test Suite (PETS)**—Latest version of tools from this kit. Refer to the Intel® PETS user guide available in the Intel® Compliancy kit for exact instructions on how to load and setup the Intel® PETS software.
- Intel® Flash Image Tool (FIT.exe)
- **Intel® Flash Programming Tool**—Available in DOS (fpt.exe), EFI (fpt.efi), Windows\* 32-bit (fptw.exe), and Windows\* 64-bit operating systems.

### Test Environment:

The System Under Test (SUT) is to be configured in manual configuration mode a with wired LAN dynamic IP address. The DHCP server connecting the SUT and Management Console (MC) must be configured to ensure that the wired LAN and wireless LAN addresses reside on separate subnets. The MC could be a laptop or desktop system running a version of Windows\* supported by PETS. The network configuration consists of a hub or switch, network cables, and a wireless Access Point (AP).



## 22.1 Test Coverage Summary

Test ID	Test Case Title	PETS/Manual	Network Factor
PSS_001	Intel Integrated Wired LAN Test	PETS	LAN+WLAN; WLAN only
PSS_002	Wake On Wireless LAN (WoWLAN) Test	PETS	LAN+WLAN; WLAN only
PSS_003	Flexible I/O Test	PETS	LAN+WLAN; WLAN only
PSS_004	BIOS Boot-Block Size Test	PETS	LAN+WLAN; WLAN only
PSS_005	Intel® CSME SMBus ASD Address Test	PETS	LAN+WLAN; WLAN only
PSS_007	Power State Deep Sx Test	PETS	LAN+WLAN; WLAN only
PSS_008	TPM on SPI Test	PETS	LAN+WLAN; WLAN only

## 22.2 Intel Integrated Wired LAN Test

Test ID	PSS_001																													
Test Case Title	Intel Integrated Wired LAN Test																													
Mandatory/Optional	Mandatory																													
Description	The PCH Soft Straps for Intel Integrated Wired LAN has to be configure correctly to ensure proper operation. Even if not using Intel Integrated Wired LAN on your platform, these PCH Soft Straps must be configured correctly as well.																													
Objective	To verify correct configuration of PCH Soft Straps related to Intel Integrated Wired LAN.																													
Procedure	<b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b>  1. If using the Intel Integrated Wired LAN solution: <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SMLink0 Enable</td><td>Offset 0x195 [0] <b>LP A0</b> Offset x0199 [0] <b>LP A1</b></td><td>1h</td></tr><tr><td>GbE PHY SMBus Address</td><td>Offset 0x1C8 [6:0] <b>LP A0</b> Offset 0x1CC [6:0] <b>LP A1</b></td><td>64h</td></tr><tr><td>GbE MAC SMBus Address</td><td>Offset 0x1C0 [6:0] <b>LP A0</b> Offset 0x1C4 [6:0] <b>LP A1</b></td><td>70h</td></tr><tr><td>Gbe MAC SMBus Address Enable</td><td>Offset 0x1C3 [0] <b>LP A0</b> Offset 0x1C7 [0] <b>LP A1</b></td><td>1h</td></tr><tr><td>PHY Connection</td><td>Offset 0x20A [2:0] <b>LP A0</b> Offset 0x20E [2:0] <b>LP A1</b></td><td>2h</td></tr><tr><td>Intel® Integrated wired LAN Enable</td><td>Offset 0xC18 [0] <b>LP A0 &amp; A1</b></td><td>0h</td></tr></table>  a. What PCIe* port is the Intel® PHY attached? <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td rowspan="2">GBE PCIe* Port Select</td><td>Offset 0x1F3 [7:4] <b>LP A0</b> Offset 0x1F4 [3:0] Offset 0x1F4 [7:4]</td><td>Port 7 = 8h Port 8 = 8h Port 9 = 8h</td></tr><tr><td>Offset 0x1F7 [7:4] <b>LP A1</b> Offset 0x1F8 [3:0] Offset 0x1F8 [7:4]</td><td>Port 7 = 8h Port 8 = 8h Port 9 = 8h</td></tr></table>	Name	Location	Value	SMLink0 Enable	Offset 0x195 [0] <b>LP A0</b> Offset x0199 [0] <b>LP A1</b>	1h	GbE PHY SMBus Address	Offset 0x1C8 [6:0] <b>LP A0</b> Offset 0x1CC [6:0] <b>LP A1</b>	64h	GbE MAC SMBus Address	Offset 0x1C0 [6:0] <b>LP A0</b> Offset 0x1C4 [6:0] <b>LP A1</b>	70h	Gbe MAC SMBus Address Enable	Offset 0x1C3 [0] <b>LP A0</b> Offset 0x1C7 [0] <b>LP A1</b>	1h	PHY Connection	Offset 0x20A [2:0] <b>LP A0</b> Offset 0x20E [2:0] <b>LP A1</b>	2h	Intel® Integrated wired LAN Enable	Offset 0xC18 [0] <b>LP A0 &amp; A1</b>	0h	Name	Location	Value	GBE PCIe* Port Select	Offset 0x1F3 [7:4] <b>LP A0</b> Offset 0x1F4 [3:0] Offset 0x1F4 [7:4]	Port 7 = 8h Port 8 = 8h Port 9 = 8h	Offset 0x1F7 [7:4] <b>LP A1</b> Offset 0x1F8 [3:0] Offset 0x1F8 [7:4]	Port 7 = 8h Port 8 = 8h Port 9 = 8h
	Name	Location	Value																											
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	Name	Location	Value																											
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Offset 0x1F7 [7:4] <b>LP A1</b> Offset 0x1F8 [3:0] Offset 0x1F8 [7:4]		Port 7 = 8h Port 8 = 8h Port 9 = 8h																												



Test ID	PSS_001																											
	<div>b. Is GPD11 from PCH routed to LAN_DISABLE_N on the Intel wired LAN PHY? (Requires Schematic Review) — If YES:</div> <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>LAN PHY Power Control GPD11 Signal Configuration</td><td>Offset 0x118 [4] <b>LP A0 &amp; A1</b></td><td>0h</td></tr></table> <div>— If NO:</div> <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>LAN PHY Power Control GPD11 Signal Configuration</td><td>Offset 0x118 [4] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table> <div>2. If not using Intel Integrated Wired LAN solution:</div> <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>LAN PHY Power Control GPD11 Signal Configuration</td><td>Offset 0x118 [4] <b>LP A0 &amp; A1</b></td><td>1h</td></tr><tr><td>Gbe MAC SMBus Address Enable</td><td>Offset 0x1C3 [6:0] <b>LP A0</b> Offset 0x1C7 [6:0] <b>LP A1</b></td><td>0h</td></tr><tr><td>PHY Connection</td><td>Offset 0x20A [2:0] <b>LP A0</b> Offset 0x20E [2:0] <b>LP A1</b></td><td>0h</td></tr><tr><td>Intel® Integrated wired LAN Enable</td><td>Offset 0xC18 [0] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table>	Name	Location	Value	LAN PHY Power Control GPD11 Signal Configuration	Offset 0x118 [4] <b>LP A0 &amp; A1</b>	0h	Name	Location	Value	LAN PHY Power Control GPD11 Signal Configuration	Offset 0x118 [4] <b>LP A0 &amp; A1</b>	1h	Name	Location	Value	LAN PHY Power Control GPD11 Signal Configuration	Offset 0x118 [4] <b>LP A0 &amp; A1</b>	1h	Gbe MAC SMBus Address Enable	Offset 0x1C3 [6:0] <b>LP A0</b> Offset 0x1C7 [6:0] <b>LP A1</b>	0h	PHY Connection	Offset 0x20A [2:0] <b>LP A0</b> Offset 0x20E [2:0] <b>LP A1</b>	0h	Intel® Integrated wired LAN Enable	Offset 0xC18 [0] <b>LP A0 &amp; A1</b>	1h
Name	Location	Value																										
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Intel® Integrated wired LAN Enable	Offset 0xC18 [0] <b>LP A0 &amp; A1</b>	1h																										
Test Pass/Fail Criteria	Test passes if Soft Straps / register setting in this step matches to the configuration in the target system.																											



## 22.3 Wake On Wireless LAN (WoWLAN) Test

<b>Test ID</b>	<b>PSS_002</b>													
<b>Test Case Title</b>	Wake On Wireless LAN (WoWLAN) Test													
<b>Mandatory/Optional</b>	Mandatory													
<b>Description</b>	The PCH controls the voltage rails into the external wireless LAN PHY using the SLP_WLAN# pin. The corresponding SoftStrap has to be configured correctly to ensure proper function of wake on wireless LAN feature.													
<b>Objective</b>	To verify correct configuration of the SLP_WLAN# SoftStrap setting.													
<b>Procedure</b>	<p><b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b></p> <p>1. Is Wake On Wireless LAN (WoWLAN) required?</p> <p>— If YES:</p> <table border="1"> <thead> <tr> <th>Name</th><th>Location</th><th>Value</th></tr> </thead> <tbody> <tr> <td>SLP_WLAN# / GPD9 Signal Configuration</td><td>Offset 0x118 [3] <b>LP A0 &amp; A1</b></td><td>0h</td></tr> </tbody> </table> <p>— If NO:</p> <table border="1"> <thead> <tr> <th>Name</th><th>Location</th><th>Value</th></tr> </thead> <tbody> <tr> <td>SLP_WLAN# / GPD9 Signal Configuration</td><td>Offset 0x118 [3] <b>LP A0 &amp; A1</b></td><td>1h</td></tr> </tbody> </table>		Name	Location	Value	SLP_WLAN# / GPD9 Signal Configuration	Offset 0x118 [3] <b>LP A0 &amp; A1</b>	0h	Name	Location	Value	SLP_WLAN# / GPD9 Signal Configuration	Offset 0x118 [3] <b>LP A0 &amp; A1</b>	1h
Name	Location	Value												
SLP_WLAN# / GPD9 Signal Configuration	Offset 0x118 [3] <b>LP A0 &amp; A1</b>	0h												
Name	Location	Value												
SLP_WLAN# / GPD9 Signal Configuration	Offset 0x118 [3] <b>LP A0 &amp; A1</b>	1h												
<b>Test Pass/Fail Criteria</b>	Test passes if Soft Straps/register setting in this step matches to the configuration in the target system.													



## 22.4 Flexible I/O Test

Test ID	PSS_003								
Test Case Title	Flexible I/O Test								
Mandatory/Optional	Mandatory								
Description	Flexible I/O is an architecture that allows some high speed signals to be configured as PCIe*, USB 3.x or SATA signals. Through Soft Straps, the functionality on these multiplexed signals are selected to meet I/O needs on the target platform.								
Objective	To verify correct configuration of Flexible I/O Soft Straps.								
Procedure	<b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b>								
	<b>1. How do you have PCIe Controller 1 (Port 1-4) configured?</b>								
	a. 1x4 – one 4 lane PCIe* Port								
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 1 (Port 1-4)</td><td>Offset 0x161 [4:3] <b>LP A0 &amp; A1</b></td><td>3h</td></tr></table>	Name	Location	Value	PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	3h		
	Name	Location	Value						
	PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	3h						
	v. Are the lanes reversed? — If Reversed:								
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 1 Lane Reversal</td><td>Offset 0x161 [2] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table>	Name	Location	Value	PCIe Controller 1 Lane Reversal	Offset 0x161 [2] <b>LP A0 &amp; A1</b>	1h		
	Name	Location	Value						
	PCIe Controller 1 Lane Reversal	Offset 0x161 [2] <b>LP A0 &amp; A1</b>	1h						
	— If NOT Reversed:								
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 1 Lane Reversal</td><td>Offset 0x161 [2] <b>LP A0 &amp; A1</b></td><td>0h</td></tr></table>	Name	Location	Value	PCIe Controller 1 Lane Reversal	Offset 0x161 [2] <b>LP A0 &amp; A1</b>	0h		
	Name	Location	Value						
PCIe Controller 1 Lane Reversal	Offset 0x161 [2] <b>LP A0 &amp; A1</b>	0h							
b. 2x2 – two 2 lane PCIe* Port									
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 1 (Port 1-4)</td><td>Offset 0x161 [4:3] <b>LP A0 &amp; A1</b></td><td>2h</td></tr></table>	Name	Location	Value	PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	2h			
Name	Location	Value							
PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	2h							
c. 1x2, 2x1- One 2 lane PCIe* Port, Two 1 lane PCIe* Port									
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 1 (Port 1-4)</td><td>Offset 0x161 [4:3] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table>	Name	Location	Value	PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	1h			
Name	Location	Value							
PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	1h							
d. 4x1: Ports (1-4) (x1)									
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 1 (Port 1-4)</td><td>Offset 0x161 [4:3] <b>LP A0 &amp; A1</b></td><td>0h</td></tr></table>	Name	Location	Value	PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	0h			
Name	Location	Value							
PCIe Controller 1 (Port 1-4)	Offset 0x161 [4:3] <b>LP A0 &amp; A1</b>	0h							
<b>2. How do you have PCIe Controller 2 (Port 5-8) configured?</b>									
a. 1x4 – One 4 lanes PCIe* Port.									
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 2 (Port 5-8)</td><td>Offset 0x169 [4:3] <b>LP A0 &amp; A1</b></td><td>3h</td></tr></table>	Name	Location	Value	PCIe Controller 2 (Port 5-8)	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	3h			
Name	Location	Value							
PCIe Controller 2 (Port 5-8)	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	3h							





Test ID	PSS_003																																																
	<div><div>i. Are the lanes reversed? — If reversed:</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 2 Lane Reversal</td><td>Offset 0x169 [4:3] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table><div>— If NOT reversed:</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 2 Lane Reversal</td><td>Offset 0x169 [4:3] <b>LP A0 &amp; A1</b></td><td>0h</td></tr></table><div>b. 2x2 – two 2 lanes PCIe* Port.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 2 (Port 5-8)</td><td>Offset 0x169 [4:3] <b>LP A0 &amp; A1</b></td><td>2h</td></tr></table><div>c. 1x2, 2x1 – One 2 lanes PCIe* Port, Two 1 lane PCIe* Port.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 2 (Port 5-8)</td><td>Offset 0x169 [4:3] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table><div>d. 4x1- One 1 lane PCIe* Port.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 2 (Port 5-8)</td><td>Offset 0x169 [4:3] <b>LP A0 &amp; A1</b></td><td>0h</td></tr></table><div><b>3. How do you have PCIe Controller 3 (Port 9-12) configured?</b><div>a. 1x4 – One 4 lanes PCIe* Port.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 3 (Port 9-12)</td><td>Offset 0x171 [4:3] <b>LP A0 &amp; A1</b></td><td>3h</td></tr></table><div>i. Are the lanes reversed? — If reversed:</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 3 Lane Reversal</td><td>Offset 0x171 [4:3] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table><div>— If NOT reversed:</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>PCIe Controller 3 Lane Reversal</td><td>Offset 0x171 [4:3] <b>LP A0 &amp; A1</b></td><td>0h</td></tr></table></div></div>	Name	Location	Value	PCIe Controller 2 Lane Reversal	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	1h	Name	Location	Value	PCIe Controller 2 Lane Reversal	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	0h	Name	Location	Value	PCIe Controller 2 (Port 5-8)	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	2h	Name	Location	Value	PCIe Controller 2 (Port 5-8)	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	1h	Name	Location	Value	PCIe Controller 2 (Port 5-8)	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	0h	Name	Location	Value	PCIe Controller 3 (Port 9-12)	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	3h	Name	Location	Value	PCIe Controller 3 Lane Reversal	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	1h	Name	Location	Value	PCIe Controller 3 Lane Reversal	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	0h
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PCIe Controller 2 Lane Reversal	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	1h																																															
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PCIe Controller 2 (Port 5-8)	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	1h																																															
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PCIe Controller 2 (Port 5-8)	Offset 0x169 [4:3] <b>LP A0 &amp; A1</b>	0h																																															
Name	Location	Value																																															
PCIe Controller 3 (Port 9-12)	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	3h																																															
Name	Location	Value																																															
PCIe Controller 3 Lane Reversal	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	1h																																															
Name	Location	Value																																															
PCIe Controller 3 Lane Reversal	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	0h																																															



Test ID	PSS_003		
	b. 2x2 – two 2 lanes PCIe* Port.		
	<b>Name</b>	<b>Location</b>	<b>Value</b>
	PCIe Controller 3 (Port 9-12)	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	2h
	c. 1x2, 2x1 – One 2 lanes PCIe* Port, Two 1 lane PCIe*.		
	<b>Name</b>	<b>Location</b>	<b>Value</b>
	PCIe Controller 3 (Port 9-12)	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	1h
	4x1- One 1 lane PCIe** Port.		
	<b>Name</b>	<b>Location</b>	<b>Value</b>
	PCIe Controller 3 (Port 9-12)	Offset 0x171 [4:3] <b>LP A0 &amp; A1</b>	0h



Test ID	PSS_003						
	<b>1. Does this platform use PCH PCIe port 1 as USB3 Port 1?</b> — If yes, PCH PCIe Port 1 configured as USB3						
	Name	Location	Value	USB3 / PCIe Combo Port 0	Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b>	1h	
	Name	Location	Value				
	USB3 / PCIe Combo Port 0	Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b>	1h				
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 0</td><td>Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b></td><td>5h</td></tr></table> — If no is, PCH PCIe 1 Statically disabled	Name	Location	Value	USB3 / PCIe Combo Port 0	Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b>	5h
	Name	Location	Value				
	USB3 / PCIe Combo Port 0	Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b>	5h				
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 0</td><td>Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b></td><td>0h</td></tr></table>	Name	Location	Value	USB3 / PCIe Combo Port 0	Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b>	0h
	Name	Location	Value				
	USB3 / PCIe Combo Port 0	Offset 0x1F0 [5:2] <b>LP A0</b> Offset 0x1F4 [5:2] <b>LP A1</b>	0h				
	<b>2. Does this platform use PCH PCIe Port 2 as USB3 Port 2?</b> — If yes, PCH PCIe Port 2 configured as USB3						
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 1</td><td>Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b></td><td>1h</td></tr></table> — If no is, PCH PCIe Port 2 configured as PCIe	Name	Location	Value	USB3 / PCIe Combo Port 1	Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b>	1h
	Name	Location	Value				
	USB3 / PCIe Combo Port 1	Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b>	1h				
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 1</td><td>Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b></td><td>5h</td></tr></table> — If no is, PCH PCIe 2 Statically disabled	Name	Location	Value	USB3 / PCIe Combo Port 1	Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b>	5h
	Name	Location	Value				
	USB3 / PCIe Combo Port 1	Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b>	5h				
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 1</td><td>Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b></td><td>0h</td></tr></table>	Name	Location	Value	USB3 / PCIe Combo Port 1	Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b>	0h	
Name	Location	Value					
USB3 / PCIe Combo Port 1	Offset 0x1F1 [3:0] <b>LP A0</b> Offset 0x1F5 [3:0] <b>LP A1</b>	0h					
<b>3. Does this platform use PCH PCIe Port 3 as USB3 Port 3?</b> — If yes, PCH PCIe Port 3 configured as USB3							
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 2</td><td>Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b></td><td>1h</td></tr></table> — If no is, PCH PCIe Port 3 configured as PCIe	Name	Location	Value	USB3 / PCIe Combo Port 2	Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b>	1h	
Name	Location	Value					
USB3 / PCIe Combo Port 2	Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b>	1h					
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 2</td><td>Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b></td><td>5h</td></tr></table> — If no is, PCH PCIe 3 Statically disabled	Name	Location	Value	USB3 / PCIe Combo Port 2	Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b>	5h	
Name	Location	Value					
USB3 / PCIe Combo Port 2	Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b>	5h					
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>USB3 / PCIe Combo Port 2</td><td>Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b></td><td>0h</td></tr></table>	Name	Location	Value	USB3 / PCIe Combo Port 2	Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b>	0h	
Name	Location	Value					
USB3 / PCIe Combo Port 2	Offset 0x1F1 [7:4] <b>LP A0</b> Offset 0x1F5 [7:4] <b>LP A1</b>	0h					



Test ID	PSS_003					
	<b>4. Does this platform use PCH PCIe Port 4 as USB3 Port 4?</b> — If yes, PCH PCIe Port 4 configured as USB3					
	Name	Location	Value	USB3 / PCIe Combo Port 3	Offset 0x1F2 [3:0] <b>LP A0</b> Offset 0x1F6 [3:0] <b>LP A1</b>	1h
	Name	Location	Value			
	USB3 / PCIe Combo Port 3	Offset 0x1F2 [3:0] <b>LP A0</b> Offset 0x1F6 [3:0] <b>LP A1</b>	1h			
	— If no is, PCH PCIe Port 4 configured as PCIe					
	Name	Location	Value	USB3 / PCIe Combo Port 3	Offset 0x1F2 [3:0] <b>LP A0</b> Offset 0x1F6 [3:0] <b>LP A1</b>	5h
	Name	Location	Value			
	USB3 / PCIe Combo Port 3	Offset 0x1F2 [3:0] <b>LP A0</b> Offset 0x1F6 [3:0] <b>LP A1</b>	5h			
	— If no is, PCH PCIe 4 Statically disabled					
	Name	Location	Value	USB3 / PCIe Combo Port 3	Offset 0x1F2 [3:0] <b>LP A0</b> Offset 0x1F6 [3:0] <b>LP A1</b>	0h
Name	Location	Value				
USB3 / PCIe Combo Port 3	Offset 0x1F2 [3:0] <b>LP A0</b> Offset 0x1F6 [3:0] <b>LP A1</b>	0h				



Test ID	PSS_003																																																												
	<div>1. How is SATA / PCIe* Combo Port 0 Strap configured on the platform?</div> <div><div>i. Statically assigned to SATA Port 0.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 0 Strap</td><td>Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b></td><td>7h</td></tr></table></div> <div><div>ii. Statically assigned to PCIe* Port 11.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 0 Strap</td><td>Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b></td><td>5h</td></tr></table></div> <div><div>iii. Assigned PCIe based on the native mode of GPP_E0 pin.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 0 Strap</td><td>Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b></td><td>Ch</td></tr></table></div> <div><div>iv. Assigned SATA based on the native mode of GPP_E0 pin.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 0 Strap</td><td>Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b></td><td>Dh</td></tr></table></div> <div><div>v. PCIe Port 11 Statically disabled.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 0 Strap</td><td>Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b></td><td>0h</td></tr></table></div> <div>2. How is SATA / PCIe* Combo Port 1 Strap configured on the platform?</div> <div><div>i. Statically assigned to SATA Port 1.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 1 Strap</td><td>Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b></td><td>7h</td></tr></table></div> <div><div>ii. Statically assigned to PCIe* Port 12.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 1 Strap</td><td>Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b></td><td>5h</td></tr></table></div> <div><div>iii. Assigned PCIe based on the native mode of GPP_E1 pin.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 1 Strap</td><td>Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b></td><td>Ch</td></tr></table></div> <div><div>iv. Assigned SATA based on the native mode of GPP_E1 pin.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 1 Strap</td><td>Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b></td><td>Dh</td></tr></table></div> <div><div>v. PCI Port 12 Statically disabled.</div><table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SATA / PCIe* Combo Port 1 Strap</td><td>Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b></td><td>0h</td></tr></table></div>	Name	Location	Value	SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	7h	Name	Location	Value	SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	5h	Name	Location	Value	SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	Ch	Name	Location	Value	SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	Dh	Name	Location	Value	SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	0h	Name	Location	Value	SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	7h	Name	Location	Value	SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	5h	Name	Location	Value	SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	Ch	Name	Location	Value	SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	Dh	Name	Location	Value	SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	0h
Name	Location	Value																																																											
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	7h																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	5h																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	Ch																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	Dh																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	0h																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	7h																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	5h																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	Ch																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	Dh																																																											
Name	Location	Value																																																											
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	0h																																																											



## 22.5 BIOS Boot-Block Size Test

<b>Test ID</b>	<b>PSS_004</b>
<b>Test Case Title</b>	BIOS Boot-Block size Test
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	BIOS Boot-Block size deals with a BIOS recovery mechanism. If this is not set correctly, then BIOS boot-block recovery mechanism would not work.
<b>Objective</b>	To verify BIOS boot-block size of correctly setup.



Test ID	PSS_003	
<b>1. How is SATA / PCIe* Combo Port 0 Strap configured on the platform?</b>		
i. Statically assigned to SATA Port 0.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	7h
ii. Statically assigned to PCIe* Port 11.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	5h
iii. Assigned PCIe based on the native mode of GPP_E0 pin.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	Ch
iv. Assigned SATA based on the native mode of GPP_E0 pin.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 0 Strap	Offset 0x1F5 [7:4] <b>LP A0</b> Offset 0x1F9 [7:4] <b>LP A1</b>	Dh
<b>2. How is SATA / PCIe* Combo Port 1 Strap configured on the platform?</b>		
i. Statically assigned to SATA Port 1.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	7h
ii. Statically assigned to PCIe* Port 12.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	5h
iii. Assigned PCIe based on the native mode of GPP_E1 pin.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	Ch
iv. Assigned SATA based on the native mode of GPP_E1 pin.		
<b>Name</b>	<b>Location</b>	<b>Value</b>
SATA / PCIe* Combo Port 1 Strap	Offset 0x1F6 [3:0] <b>LP A0</b> Offset 0x1FA [3:0] <b>LP A1</b>	Dh



Test ID	PSS_004						
Procedure	<b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b>						
	1. What size is your SPI flash BIOS boot block?						
	a. If 64KB						
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>0h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	0h
	Name	Location	Value				
	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	0h				
	a. 128KB						
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>1h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	1h
	Name	Location	Value				
	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	1h				
	b. 256KB						
	<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>2h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	2h
	Name	Location	Value				
	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	2h				
	c. 512KB						
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>3h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	3h	
Name	Location	Value					
Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	3h					
d. 1MB							
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>4h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	4h	
Name	Location	Value					
Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	4h					
e. 2MB							
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>5h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	5h	
Name	Location	Value					
Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	5h					
f. 4MB							
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>6h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	6h	
Name	Location	Value					
Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	6h					
g. 8MB							
<table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Top Swap Block size</td><td>Offset 0x14C [6:4] LP A0 &amp; A1</td><td>7h</td></tr></table>	Name	Location	Value	Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	7h	
Name	Location	Value					
Top Swap Block size	Offset 0x14C [6:4] LP A0 & A1	7h					
Test Pass/Fail Criteria	Test passes if Soft Straps/register setting in this step matches to the configuration in the target system.						





## 22.6 Intel® CSME SMBus Alert Sending Device (ASD) Address Test

Test ID	PSS_005																								
Test Case Title	Intel® CSME SMBus Alert Sending Device (ASD) Address Test.																								
Mandatory/Optional	Mandatory for target system with Intel® AMT.																								
Description	This field is only applicable if there is an ASD attached to SMBus and using Intel® AMT.																								
Objective	To verify Intel® CSME SMBus ASD enable and address bits are correctly configure.																								
Procedure	<p><b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b></p> <p>1. Is there an Alert Sending Device (ASD) on Host SMBus?</p> <p><b>Note:</b> This is only valid for Intel® AMT enabled platforms (refer SPI Programming Guide for more information)</p> <p>— If YES,</p> <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Intel® CSME SMBus ASD Address</td><td>Offset 0x184 [6:0] <b>LP A0</b> Offset 0x188 [6:0] <b>LP A1</b></td><td>Refer details in <sup>1</sup>SPI Programming Guide</td></tr><tr><td>Intel® CSME SMBus ASD Address Enable</td><td>Offset 0x187 [0] <b>LP A0</b> Offset 0x18B [0] <b>LP A1</b></td><td>1h</td></tr><tr><td>Intel® CSME SMBus Subsystem Device ID for ASF</td><td>Offset 0x18A [31:0] <b>LP A0</b> Offset 0x18E [31:0] <b>LP A1</b></td><td>Refer details in <sup>2</sup>SPI Programming Guide</td></tr></table> <p>— If NO,</p> <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Intel® CSME SMBus ASD Address</td><td>Offset 0x184 [6:0] <b>LP A0</b> Offset 0x188 [6:0] <b>LP A1</b></td><td>0h</td></tr><tr><td>Intel® CSME SMBus ASD Address Enable</td><td>Offset 0x187 [0] <b>LP A0</b> Offset 0x18B [0] <b>LP A1</b></td><td>0h</td></tr><tr><td>Intel® CSME SMBus Subsystem Device ID for ASF</td><td>Offset 0x18A [31:0] <b>LP A0</b> Offset 0x18E [31:0] <b>LP A1</b></td><td>0h</td></tr></table> <p><b>Note:</b></p> <p><sup>1</sup>Intel® CSME SMBus Alert Sending Device (ASD) Address (MESMASDA) address must be Non-zero, unique address on the Host SMBus segment, and compatible with the master on SMBus.</p> <p><sup>2</sup>Intel® CSME SMBus Subsystem Vendor and Device ID.</p>	Name	Location	Value	Intel® CSME SMBus ASD Address	Offset 0x184 [6:0] <b>LP A0</b> Offset 0x188 [6:0] <b>LP A1</b>	Refer details in <sup>1</sup> SPI Programming Guide	Intel® CSME SMBus ASD Address Enable	Offset 0x187 [0] <b>LP A0</b> Offset 0x18B [0] <b>LP A1</b>	1h	Intel® CSME SMBus Subsystem Device ID for ASF	Offset 0x18A [31:0] <b>LP A0</b> Offset 0x18E [31:0] <b>LP A1</b>	Refer details in <sup>2</sup> SPI Programming Guide	Name	Location	Value	Intel® CSME SMBus ASD Address	Offset 0x184 [6:0] <b>LP A0</b> Offset 0x188 [6:0] <b>LP A1</b>	0h	Intel® CSME SMBus ASD Address Enable	Offset 0x187 [0] <b>LP A0</b> Offset 0x18B [0] <b>LP A1</b>	0h	Intel® CSME SMBus Subsystem Device ID for ASF	Offset 0x18A [31:0] <b>LP A0</b> Offset 0x18E [31:0] <b>LP A1</b>	0h
Name	Location	Value																							
Intel® CSME SMBus ASD Address	Offset 0x184 [6:0] <b>LP A0</b> Offset 0x188 [6:0] <b>LP A1</b>	Refer details in <sup>1</sup> SPI Programming Guide																							
Intel® CSME SMBus ASD Address Enable	Offset 0x187 [0] <b>LP A0</b> Offset 0x18B [0] <b>LP A1</b>	1h																							
Intel® CSME SMBus Subsystem Device ID for ASF	Offset 0x18A [31:0] <b>LP A0</b> Offset 0x18E [31:0] <b>LP A1</b>	Refer details in <sup>2</sup> SPI Programming Guide																							
Name	Location	Value																							
Intel® CSME SMBus ASD Address	Offset 0x184 [6:0] <b>LP A0</b> Offset 0x188 [6:0] <b>LP A1</b>	0h																							
Intel® CSME SMBus ASD Address Enable	Offset 0x187 [0] <b>LP A0</b> Offset 0x18B [0] <b>LP A1</b>	0h																							
Intel® CSME SMBus Subsystem Device ID for ASF	Offset 0x18A [31:0] <b>LP A0</b> Offset 0x18E [31:0] <b>LP A1</b>	0h																							
Test Pass/Fail Criteria	Test passes if Soft Straps/register setting in this step matches to the configuration in the target system.																								



## 22.7 Power State Deep Sx Test

Test ID	PSS_007																		
Test Case Title	Power State Deep Sx Test																		
Mandatory/Optional	Mandatory																		
Description	To minimize power consumption while in S3/S4/S5, the PCH supports a lower power, lower featured version of these power states known as Deep Sx. In the Deep Sx state, the Suspend wells are powered off, while the Deep Sx Well (DSW) remains powered. A limited set of wake events are supported by the logic located in the DSW. The Deep Sx capability and the SUSPWRDNACK pin functionality are mutually exclusive.																		
Objective	To verify correct configuration of Power State Deep Sx.																		
Procedure	<p><b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b></p> <p>1. Does the platform support power state Deep Sx? — If YES:</p> <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Deep Sx Enable</td><td>Offset 0x17C [20] <b>LP A0 and A1</b></td><td>1h</td></tr><tr><td></td><td>Offset 0xC14 [20]</td><td>1h</td></tr></table> <p>— If NO,</p> <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>Deep Sx Enable</td><td>Offset 0x17C [20] <b>LP A0 and A1</b></td><td>0h</td></tr><tr><td></td><td>Offset 0xC14 [20]</td><td>0h</td></tr></table> <p><b>Note:</b> This is not the same as Intel® CSME power state M3.</p>	Name	Location	Value	Deep Sx Enable	Offset 0x17C [20] <b>LP A0 and A1</b>	1h		Offset 0xC14 [20]	1h	Name	Location	Value	Deep Sx Enable	Offset 0x17C [20] <b>LP A0 and A1</b>	0h		Offset 0xC14 [20]	0h
Name	Location	Value																	
Deep Sx Enable	Offset 0x17C [20] <b>LP A0 and A1</b>	1h																	
	Offset 0xC14 [20]	1h																	
Name	Location	Value																	
Deep Sx Enable	Offset 0x17C [20] <b>LP A0 and A1</b>	0h																	
	Offset 0xC14 [20]	0h																	
Test Pass/Fail Criteria	Test passes if Soft Straps/register setting in this step matches to the configuration in the target system.																		



## 22.8 Trusted Platform Module (TPM) on SPI Test

Test ID	PSS_008																		
Test Case Title	Trusted Platform Module on SPI Test																		
Mandatory/Optional	Mandatory																		
Description	TPM can be configured through PCH Soft Straps to operate over LPC or SPI, but no more than 1 TPM is allowed in the target system.																		
Objective	To verify TPM on SPI is correctly configured.																		
Procedure	<b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b>  1. Does this platform have a TPM connected to SPI controller? — If YES, Skip to Boot to targeted OS testing step. <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>TPM Over SPI Bus Enable</td><td>Offset 0x1EC [0] <b>LP A0</b> Offset 0x1F0 [0] <b>LP A1</b></td><td>1h</td></tr></table> — If NO (default), <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>TPM Over SPI Bus Enable</td><td>Offset 0x1EC [0] <b>LP A0</b> Offset 0x1F0 [0] <b>LP A1</b></td><td>0h</td></tr></table>	Name	Location	Value	TPM Over SPI Bus Enable	Offset 0x1EC [0] <b>LP A0</b> Offset 0x1F0 [0] <b>LP A1</b>	1h	Name	Location	Value	TPM Over SPI Bus Enable	Offset 0x1EC [0] <b>LP A0</b> Offset 0x1F0 [0] <b>LP A1</b>	0h						
	Name	Location	Value																
	TPM Over SPI Bus Enable	Offset 0x1EC [0] <b>LP A0</b> Offset 0x1F0 [0] <b>LP A1</b>	1h																
	Name	Location	Value																
	TPM Over SPI Bus Enable	Offset 0x1EC [0] <b>LP A0</b> Offset 0x1F0 [0] <b>LP A1</b>	0h																
	<b>Boot to targeted OS. Verify correct configuration of the PCH Soft Straps below:</b>  1. What Clock Frequency is being used for TPM on SPI? a. If 48MHz <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SPI TPM Clock Frequency</td><td>Offset 0x151 [2:0] <b>LP A0 &amp; A1</b></td><td>1h</td></tr></table> b. 25MHz <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SPI TPM Clock Frequency</td><td>Offset 0x151 [2:0] <b>LP A0 &amp; A1</b></td><td>4h</td></tr></table> c. 14MHz <table><tr><th>Name</th><th>Location</th><th>Value</th></tr><tr><td>SPI TPM Clock Frequency</td><td>Offset 0x151 [2:0] <b>LP A0 &amp; A1</b></td><td>6h</td></tr></table>	Name	Location	Value	SPI TPM Clock Frequency	Offset 0x151 [2:0] <b>LP A0 &amp; A1</b>	1h	Name	Location	Value	SPI TPM Clock Frequency	Offset 0x151 [2:0] <b>LP A0 &amp; A1</b>	4h	Name	Location	Value	SPI TPM Clock Frequency	Offset 0x151 [2:0] <b>LP A0 &amp; A1</b>	6h
	Name	Location	Value																
	SPI TPM Clock Frequency	Offset 0x151 [2:0] <b>LP A0 &amp; A1</b>	1h																
	Name	Location	Value																
	SPI TPM Clock Frequency	Offset 0x151 [2:0] <b>LP A0 &amp; A1</b>	4h																
Name	Location	Value																	
SPI TPM Clock Frequency	Offset 0x151 [2:0] <b>LP A0 &amp; A1</b>	6h																	
Test Pass/Fail Criteria	Test passes if Soft Straps/register setting in this step matches to the configuration in the target system.																		





## 23 Intel® System Security Report (Nifty Rock) Compliance

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### 23.1 Introduction

The purpose of this document is to provide OEMs guidance on the steps necessary to successfully validate **Intel® System Security Report (Nifty Rock)** technology on Intel client (desktop and mobile) platforms. This document defines the purpose and value of each validation aspect in the validation process. The intent of this document is to outline the ideal validation sequence for **Intel® System Security Report (Nifty Rock)** in this platform and provide an overview of the collateral that is available to provide OEMs the framework to define their own validation strategy.

This document is not a technology. **The readers are expected to be familiar with Intel® Hardware Shield (Intel® Trusted Execution Technology, Intel® Runtime BIOS Resilience Technology, Intel® System Security Report (Nifty Rock) and Devil's Gate Rock technology) to use this document as a validation supplement to develop their own Nifty Rock validation plan.** For Nifty Rock collaterals refer to [Section 23.1.4](#).

Devil's Gate Rock (DGR) is the collection of techniques and code within the BIOS used to create and enforce HW access policy for the SMI handler. It consists of a collection of policy mechanisms that are configured by POST before the SMI handler is locked down. Once the SMI handler is locked all accesses into the system must be compliant with the policy established during POST.

Intel® Runtime BIOS Resilience is a subset of DGR covering SMM memory policy only. Intel® Runtime BIOS Resilience Protection hardens the SMI handler via hardware enforced BIOS policy regarding SMI handler access to memory using an enhanced paging policy. This paging policy covers SMI handler access to both BIOS and MLE resources. Intel® Runtime BIOS Resilience Protection is extended using a technology code named **Intel® System Security Report (Nifty Rock)**.

The Platform Properties Assessment Module (PPAM) is the primary component of **Intel® System Security Report (Nifty Rock)** and is used to **collect and report information about platform SMM implementation and configuration**, in order to provide trustworthy attestation of the resulting SMI memory policy regarding SMM secure configuration and access to MLE owned memory. **Intel® System Security Report (Nifty Rock)** is used to create a trustworthy report describing the SMM policy

#### 23.1.1 Platforms Applicable

This validation guide is applicable to the following Client vPro platforms

**Table 23-1. List of Applicable Platforms**

Platform Name
Alder Lake
Comet Lake U
Tiger Lake
Comet Lake H
Comet Lake S
Whiskey Lake U
Coffee Lake S 8+2
Coffee Lake H 8+2

## 23.1.2 Terminology

Term	Description
Intel® TXT	Intel® Trusted Execution Technology
IRBR	Intel® Runtime BIOS Resilience Technology
DGR	Devil's Gate Rock
Intel® Hardware Shield	Intel® Trusted Execution Technology, Intel® Runtime BIOS Resilience Technology, Devil's Gate Rock, Intel® System Security Report (also Nifty Rock)

## 23.1.3 Nifty Rock Prerequisites

Applicable platforms are listed above.

- Verify chipset is Intel® TXT capable
- Processor should support Intel® TXT and have it enabled in BIOS, it should be Intel® vPro® QDF as well.
- Incorporate the PPAM binaries provided as part of the PPAM kit into the BIOS as recommended in the BIOS Writer's guide. Refer to next Section.
- Install the tools provided along with the PPAM kit posted on VIP on the system. Run the tools from UEFI shell root directory

### BIOS Setting:

1. Intel Advanced Menu > CPU Configuration > Intel® TXT<Enabled>

**Note:** For enabling Intel® TXT and more details, refer to [Chapter 13, "Intel® Trusted Execution Technology \(Intel® TXT\)"](#).



## 23.1.4 Reference Documents

**Table 23-2. Intel® TXT**

Intel® TXT Software Development Guide: Measured Launch Environment Developers Guide	<a href="https://www.intel.com/content/dam/www/public/us/en/documents/guides/intel-txt-software-development-guide.pdf">https://www.intel.com/content/dam/www/public/us/en/documents/guides/intel-txt-software-development-guide.pdf</a>
Intel® TXT BIOS Specification	# 572782
Intel® Trusted Execution Technology ACM Kit	Refer to VIP portal for the latest kit
Intel® TXT TPM Provisioning Toolkit	Refer to VIP portal for the latest kit
Intel® TXT Client Debug Toolkit	Refer to VIP portal for the latest kit
Intel® Trusted Execution Technology (Intel® TXT) TBoot information	<a href="https://sourceforge.net/p/tboot/wiki/Home/">https://sourceforge.net/p/tboot/wiki/Home/</a>
Intel® Trusted Execution Technology (Intel® TXT) STM Guide	# 596559
Intel® Management Engine (Intel® ME) and Intel® Sensor Solution Consumer/Corporate Compliance Guide	Chapter 13, "Intel® Trusted Execution Technology (Intel® TXT)"

**Table 23-3. Copper Point**

Intel® Runtime BIOS Resilience Architecture Guide Overview 0.8	# 576872
Core and Uncore BIOS Specification	# 550049

**Table 23-4. Nifty Rock**

Intel® Platform Properties Assessment Module (PPAM) 1.0 Operating System User Guide	# 602426
Intel® Platform Properties Assessment Module (PPAM) 1.0 OS Diagnostic User Guide	# 609184
Intel® Platform Properties Assessment Module (PPAM) 1.1 User Guide	# 604868
Intel® Platform Properties Assessment Module (PPAM) 1.1 Diagnostic User Guide	# 609181
Nifty Rock Technology BIOS specifications	# 601824
Platform Intel® Properties Assessment Module (PPAM) Kit	Refer to VIP portal for the latest kit
Intel® CSME 15 and Intel® Sensor Solution Corporate Compliance Guide	Chapter 23

## 23.1.5 Validation Tools

Refer following commands to run from UEFI shell to collect entire report on platform capability and resources through the PPAM.

1. Load PpamService.efi
2. FrmLoaderApp.efi Frm.efi <SINIT\_ACM.bin>
3. PpamTestApp.efi
4. TxtDumpLogApp.efi
5. PpamManifestDumpApp.efi.



**Note:** SINIT\_ACM.bin needs to be passed on Intel® TXT-enabled platform

- **Load PpamService.efi**
  - Produces the PPAM launch protocol which are used by Frm.efi
- **FrmLoaderApp.efi Frm.efi <SINIT\_ACM.bin>**
  - Establishes VMX root mode
- **PpamTestApp.efi**
  - It dumps the PPAM report
- **TxtDumpLogApp.efi**
  - It dumps the ACM event log
- **PpamManifestDumpApp.efi**
  - It dumps the PPAM manifest.

## 23.2 Nifty Rock Test

This section describes the test plan used to verify Nifty Rock functionality on systems enabling the feature.

Test ID	Test Case Title	PETS/Manual	Mandatory/Optional
NR_TC01	Check PPAM binaries are successfully loaded	Manual	Mandatory
NR_TC02	Check "CapabilityPhysicalResourceBitmap" value returned indicates PPAM physical resource	Manual	Mandatory
NR_TC03	Check "PPAM_RSC_VALID_INDICATOR" value for resource list validity and every APICID should be valid	Manual	Mandatory
NR_TC04	Check "PPAM_META_PROPERTY_BITMAP" meta resources BIOS SMM properties and lock setting are asserted correctly	Manual	Mandatory
NR_TC05	Check the PPAM memory range attributes are set correctly	Manual	Mandatory
NR_TC06	Verify PPAM hash matches PpamManifest hash	Manual	Mandatory
NR_TC07	Check all PPAM resources are returned as part of PPAM_GET_RESOURCES_VMCALL	Manual	Mandatory

**Note:** Make sure to cover the prerequisites in [Section 23.1.3](#) before running any of the tests below.



## 23.3 NR\_TC01

Test ID	NR_TC01
Test Case Title	Check PPAM binaries are successfully loaded
Mandatory/Optional	Mandatory
Description	Validate no errors are reported in PPAMTestApp log
Objective	Check PPAM is successfully loaded
Procedure	<ol style="list-style-type: none"><li>1. Boot to EFI-Shell and run step 2 from root directory</li><li>2. Load PpamService.efi FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM.bin&gt; PpamTestApp.efi;</li><li>3. Obtain PpamTestApp log by running PpamTestApp.efi result in step 2</li><li>4. Make sure GetResource value for each CPU is 0x0 under PPAM_GET_RESOURCES_VMCALL and also flag bit zero, is set for all APICID's in PPAM_RSC_VALID_INDICATOR corresponding to CPU threads in GetResource.</li></ol> <p><b>Note:</b> If "FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM&gt;" does not complete correctly. Run the test again with the command "FrmLoaderApp.efi Frm.efi -notxt" to check PPAM is integrated correctly irrespective of TXT. In this case PpamTestApp log obtained, will indicate it is running outside of TXT and would not report resources under PPAM_GET_RESOURCES_VMCALL i.e ResourceSize is 0x0</p>
Test Pass/Fail Criteria	Test passes, if no error is reported in GetResource value for each CPU and there is no missing corresponding APICID in PPAM_RSC_VALID_INDICATOR

## 23.4 NR\_TC02

Test ID	NR_TC02
Test Case Title	Check "CapabilityPhysicalResourceBitmap" value returned indicates PPAM physical resource
Mandatory/Optional	Mandatory
Description	Identify PPAM implementation of physical resources reported by the platform
Objective	Validate CapabilityPhysicalResourceBitmap value returned is correct
Procedure	<ol style="list-style-type: none"><li>1. Boot to EFI-Shell and run step 2 from root directory</li><li>2. Load PpamService.efi FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM.bin&gt; PpamTestApp.efi;</li><li>3. Obtain PpamTestApp log by running PpamTestApp.efi result in step 2</li><li>4. For NR1.0 PPAM10 and lower: Verify "CapabilityPhysicalResourceBitmap" returned under PPAM_GET_CAPABILITY_VMCALL: should match 0x0000000000000001. For NR 1.1 PPAM 11: Verify "CapabilityPhysicalResourceBitmap" returned under PPAM_GET_CAPABILITY_VMCALL: should match 0x0000000000000057</li></ol>
Test Pass/Fail Criteria	Test passes if CapabilityPhysicalResourceBitmap is 0x0000000000000001 for NR1.0 PPAM10 and lower and For NR1.1 and PPAM 11: Test passes if CapabilityPhysicalResourceBitmap is 0x0000000000000057





## 23.5 NR\_TC03

Test ID	NR_TC03
Test Case Title	Check "PPAM_RSC_VALID_INDICATOR" value for resource list validity for every APICID
Mandatory/Optional	Mandatory
Description	PPAM resources are defined properly
Objective	Testing configuration of the platform
Procedure	<ol style="list-style-type: none"> <li>1. Boot to EFI-Shell and run step 2 from root directory</li> <li>2. Load PpamService.efi FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM.bin&gt; PpamTestApp.efi;</li> <li>3. Obtain PpamTestApp log by running PpamTestApp.efi result in step 2</li> <li>4. Check "RscType" value and "RscLength" under PPAM_RSC_VALID_INDICATOR. "RscType" should be 0x 00000001 and "RscLength" should be 0x0010</li> </ol>
Test Pass/Fail Criteria	Test passes, if log contains the below values under "PPAM_RSC_VALID_INDICATOR" RscType: 00000001 RscLength: 0010

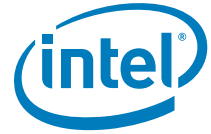
## 23.6 NR\_TC04

Test ID	NR_TC04
Test Case Title	Check "PPAM_META_PROPERTY_BITMAP" meta resources BIOS SMM properties and lock setting are asserted correctly
Mandatory/Optional	Mandatory
Description	PPAM meta properties are asserted correctly
Objective	Check meta properties; BIOS SMM properties and lock setting are asserted correctly in the platform
Procedure	<ol style="list-style-type: none"> <li>1. Boot to EFI-Shell and run step 2 from root directory</li> <li>2. Load PpamService.efi FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM.bin&gt;; PpamTestApp.efi;</li> <li>3. Obtain PpamTestApp log by running PpamTestApp.efi result in step 2</li> <li>4. Check "CapabilityMetaResourceBitmap" value from PPAM_GET_CAPABILITY_VMCALL.</li> <li>5. Check "Properties" value under PPAM_META_PROPERTY_BITMAP</li> <li>6. If "CapabilityMetaResourceBitmap" value is equal to "Properties" value under PPAM_META_PROPERTY_BITMAP, meta properties are set correctly</li> </ol>
Test Pass/Fail Criteria	PASS, if CapabilityMetaResourceBitmap value is equal to Properties value under PPAM_META_PROPERTY_BITMAP (000000000000000007)



## 23.7 NR\_TC05

Test ID	NR_TC05
Test Case Title	Check PPAM memory range attributes are not executable
Mandatory/Optional	Mandatory
Description	PPAM memory range attributes are correctly set
Objective	Check memory range attributes are not executable
Procedure	<ol style="list-style-type: none"><li>1. Boot to EFI-Shell and run step 2 from root directory</li><li>2. Load PpamService.efi FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM.bin&gt;; PpamTestApp.efi;</li><li>3. Obtain PpamTestApp log by running PpamTestApp.efi result in step 2</li><li>4. Check "RWXAttributes" value under PPAM_PHYS_MEM_RANGE returned is not 00000007</li></ol>
Test Pass/Fail Criteria	PASS, if for all memory ranges log does not have RWX Attributes equal to 00000007



## 23.8 NR\_TC06

Test ID	NR_TC06
Test Case Title	Verify PPAM hash matches PpamManifest hash
Mandatory/Optional	Mandatory
Description	PPAM Manifest contains digital signature of PPAM binary. This test is to make sure that the hash of the PPAM matches STM hash in the TXTdump log,TPM dynamic event log
Objective	Verify PPAM Manifest is correctly loaded
Procedure	<ol style="list-style-type: none"> <li>1. Boot to EFI-Shell and run step 2 from root directory</li> <li>2. Load PpamService.efi FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM.bin&gt;; PpamTestApp.efi; TXTDumpLogApp.efi; PpamManifestDumpApp.efi</li> <li>3. Obtain PPAM Manifest log generated by running PpamManifestDumpApp.efi in step 2</li> <li>4. Get PPAM Manifest SHA value that contains the hash (a non-zero value)</li> <li>5. Obtain TXT log generated by running TXTDumpLogApp.efi in step 2</li> <li>6. Get Digest(0) value from under PCRIndex - 17, EventType - 0x0000040E (STM_HASH)</li> <li>7. Compare PPAM SHA value to the digest value from txt log</li> </ol>
Test Pass/Fail Criteria	PASS, if PPAM SHA value matches the digest value

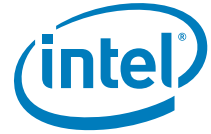
## 23.9 NR\_TC07

Test ID	NR_TC07
Test Case Title	Check all PPAM resources are returned as part of PPAM_GET_RESOURCES_VMCALL
Mandatory/Optional	Mandatory
Description	All PPAM resources should be reported



Test ID	NR_TC07
Objective	Verify HW access policy is enforced for SMM besides SMM memory policy for maximum security
Procedure	<p>1. Boot to EFI-Shell</p> <p>2. Load PpamService.efi FrmLoaderApp.efi Frm.efi &lt;SINIT_ACM&gt;; PpamTestApp.efi;</p> <p>3. Obtain PPAM Test App log generated by running PpamTestApp.efi in step2</p> <p>4. Check resources under "PPAM_GET_RESOURCES_VMCALL"</p> <p>5. For NR1.0 PPAM 10 and lower: Make sure all below resources are listed in PpamTestApp log</p> <ul style="list-style-type: none"><li>&gt; PPAM_SCRATCH_RESOURCE</li><li>&gt; PPAM_PHYS_MEM_RANGE</li><li>&gt; PPAM_META_PROPERTY_BITMAP</li><li>&gt; PPAM_RSC_VALID_INDICATOR</li><li>&gt; PPAM_META_DIAGNOSTIC (Note: This resource is displayed, if a diagnostic error occurs)</li><li>&gt; PPAM_END_OF_RESOURCES</li></ul> <p>For NR1.1 PPAM 11: Make sure all below resources are listed in PpamTestApp log</p> <ul style="list-style-type: none"><li>&gt; PPAM_SCRATCH_RESOURCE</li><li>&gt; PPAM_PHYS_MEM_RANGE</li><li>&gt; PHYS_IO_RANGE</li><li>&gt; PHYS_MSR</li><li>&gt; PHYS_CPU_STATE_SAVE_REG</li><li>&gt; PHYS_CPU_OTHER_REG</li><li>&gt; PPAM_META_PROPERTY_BITMAP</li><li>&gt; PPAM_RSC_VALID_INDICATOR</li><li>&gt; PPAM_META_DIAGNOSTIC (Note: This resource is displayed, if a diagnostic error occurs)</li></ul>
Test Pass/Fail Criteria	PASS if no resource is missing from the above listed resources under PPAM_GET_RESOURCES_VMCALLSS

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## 24 Intel® Trusted Device Setup

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### 24.1 Introduction

Intel® Trusted Device Setup (Intel® TDS) provides a tampering detection mechanism that enables IT to trust the automated device enrollment solutions.

- Devices are sealed and locked with platform measurements data on manufacturing line.
- Detection of tampering attempts after Seal applied.
- Device attestation during end user boot (3<sup>rd</sup> party solution).
- Automated provisioning based on the attestation result.

### 24.2 Solution Prerequisites

- Windows\* 10 Intel® MEI Driver with Intel® TDS support.
- Windows\* PE\* on a bootable media (Example: PXE, HDD) with configuration and tools.
- Intel® IFWI with BIOS Extension and Intel® TDS configuration enabled on CSME FW.
- Bootguard profile 5 with startup locality 3.
- HW TPM 2.0 Intel® Boot Guard or equivalent.
- OPAL v2 or Pyrite (v1 or v2) - compliant NVMe\* Self Encrypting Drive (SED), unlocked and not activated.

### 24.3 Terminology

Terms	Description
Intel® TDS	Intel® Trusted Device Setup
Intel® PMT	Intel® Platform Measurements Tool
PBA	Pre-boot application (BIOS Extension)

## 24.4 Tools for Testing

Tool Name	New For Intel® TDS	Description
Intel® Platform Measurements Tool (Intel® PMT)	Yes	Collects platform measurements and signs them, produces a signed Platform Measurement File (PMF).
Intel® MEInfo	No	Provides information about the status of the platform, and notifies the user whether Intel® TDS is enabled.
Intel® TDS Sealing Tool	Yes	Seals, unseals, and reseals a device on the manufacturing line.
Intel® TDS Seal Validation Tool	Yes	Intel® Trusted Device Setup Seal Validation Tool allows to perform a local attestation of Intel® TDS system components for functional validation purposes.  <b>Note:</b> This tool can run only on Windows* 10.
TBSLogGenerator	External Tool	Dumps PCR values and TCG log in a human-readable format for the boot session when TBSLogGenerator.exe gets run.

## 24.5 Process Prerequisites

Use the below commands to generate certificates needed for the E2E flow (Refer to [www.openssl.org](http://www.openssl.org) to get the tool):

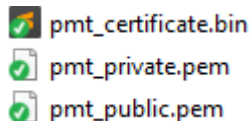
- **Generate the private key and certificate**

```
openssl.exe req -x509 -newkey rsa:2048 -keyout pmt_private.pem -out pmt_certificate.bin -days 365 -nodes -outform DER -subj "/C=US/ST=Oregon/L=Portland/O=INTEL/OU=SSG/CN=PMF pseudo-signing certificate"
```

- **Extract public key from private key**

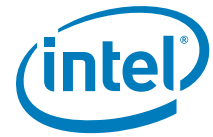
```
openssl.exe rsa -in pmt_private.pem -outform PEM -pubout -out pmt_public.pem
```

These commands will generate the following files:



pmt\_certificate.bin  
pmt\_private.pem  
pmt\_public.pem

- Copy these files to the PMT folder



## 24.6 Intel® TDS Solution Compliance Test Coverage Summary

A= Automated, M= Manual, S= Semi-automated

Test ID	Test Case Title	How	Test Type
TDS_01	FW image Intel® TDS capable	A	Compliance
TDS_02	Intel® Boot Guard enabled	A	Compliance
TDS_03	Platform prerequisites	A	Compliance
TDS_04	Seal device in collection mode	A	Compliance
TDS_05	BIOS configuration lock	S	Compliance
TDS_06	Chassis intrusion lock	S	Compliance
TDS_07	SED lock	S	Compliance
TDS_08	Opt-out	S	Compliance
TDS_09	Dropship boot unseal check	S	Compliance



## 24.7 Tests

### 24.7.1 TDS\_01

<b>Test ID</b>	<b>TDS_01</b>
<b>Test Case Title</b>	FW Image Intel® TDS Capable
<b>Mandatory/Optional</b>	Mandatory
<b>Test Type</b>	Prerequisite
<b>Description</b>	Check if the image has Intel® TDS enabled
<b>Objective</b>	Ensures the image on the platform is TDS capable.
<b>Procedure</b>	<p>Run Intel® MEInfo and verify that Intel® Trusted Device Setup shows Present/Enabled:</p> <p>FW Capabilities 0x7FF6D645</p> <p>Intel(R) Active Management Technology - PRESENT/ENABLED Protect Audio Video Path - PRESENT/ENABLED Intel(R) Dynamic Application Loader - PRESENT/ENABLED Service Advertisement &amp; Discovery - PRESENT/ENABLED Intel(R) Platform Trust Technology - PRESENT/ENABLED Persistent RTC and Memory - PRESENT/ENABLED Intel(R) Trusted Device Setup - PRESENT/ENABLED</p>
<b>Test Pass/Fail Criteria</b>	Test passes when Intel® Trusted Device Setup shows Present/Enabled.



## 24.7.2 TDS\_02

Test ID	TDS_02																																										
Test Case Title	Intel® Boot Guard enabled																																										
Mandatory/ Optional	Mandatory																																										
Test Type	Prerequisite																																										
Description	Check that Intel® Boot Guard profile 5 is enabled, and startup from locality 3.																																										
Objective	Ensures the boot flow is with secure and measured boot.																																										
Procedure	<div>1. To check Intel® Boot Guard Profile, run Intel® MEInfo with -fwstatus flag.</div> <div>2. Parse Fwstatus6, if FACB[bit=0] == 1, PBE[bit=3] == 1, VB[bit=9] ==1, MB[bit=8] == 1 and ENF[bit=6:7] == 3, then it's Boot Guard profile 5 (According to the below table)</div> <div><div>BTG PROFILES</div><table><tr><th>Profile</th><th>FACB</th><th>PBE</th><th>VB</th><th>MB</th><th>ENF</th><th>Comments</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>BTG disabled</td></tr><tr><td>3</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Debug profile</td></tr><tr><td>4</td><td>1</td><td>1</td><td>1</td><td>0</td><td>3</td><td>Strict profile</td></tr><tr><td>5</td><td>1</td><td>1</td><td>1</td><td>1</td><td>3</td><td>Strict profile + measured boot</td></tr><tr><td>6</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Available in SPS only</td></tr></table></div> <div>3. To calculate Locality 3:<div>a. Reboot and Run TBSLogGenerator &gt;log.txt</div><div>b. In log.txt, search for the event that includes a line with this format: PCR[00]= "Number" and the event does not have EV_NO_ACTION.</div></div> <div>Example:</div> <div><pre>****ID0001***0x0084-0x00d0***** Event 01: EV_S_CRTM_CONTENTS (0x00000007), 77 bytes for PCR[00] DIGEST = 812397d3441823ccc6fe375871159d47b769b5f82f1a26b66c6cb55d1e854e15 PCR[00] = 72fc9a838d68ad233649aea9f31c7568e69e2717f068ee392c6e593abca60b3d EventData (27 bytes): 00000000   42 6f 6f 74 20 47 75 61-72 64 20 4d 65 61 73 75   Boot Guard Measu 00000010   72 65 64 20 53 2d 43 52-54 4d 00   red S-CRTM ****ID0002***0x00d1-0x0104*****</pre></div> <div>4. Validate the following (DIGEST can be found in the same event of PCR[00]) :hash256((0003    DIGEST) == PCR[00]) (It is obtained from TBSLogGenerator. It is a Microsoft* tool that is released with the HLK)</div>	Profile	FACB	PBE	VB	MB	ENF	Comments	0	0	0	0	0	0	BTG disabled	3	0	1	1	1	0	Debug profile	4	1	1	1	0	3	Strict profile	5	1	1	1	1	3	Strict profile + measured boot	6	1	1	1	0	0	Available in SPS only
Profile	FACB	PBE	VB	MB	ENF	Comments																																					
0	0	0	0	0	0	BTG disabled																																					
3	0	1	1	1	0	Debug profile																																					
4	1	1	1	0	3	Strict profile																																					
5	1	1	1	1	3	Strict profile + measured boot																																					
6	1	1	1	0	0	Available in SPS only																																					
Test Pass/Fail Criteria	Test passes when BtG profile is enabled and locality is 3.																																										

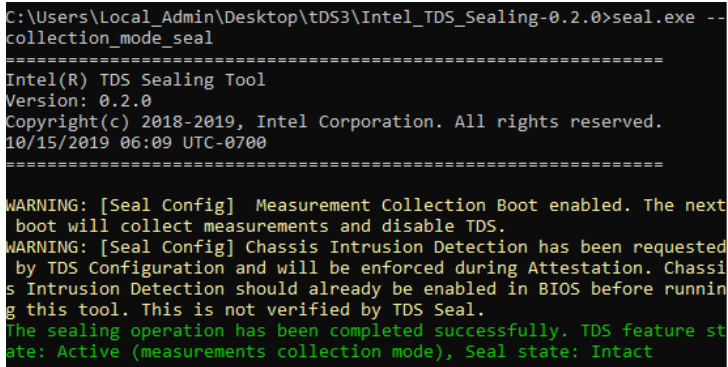
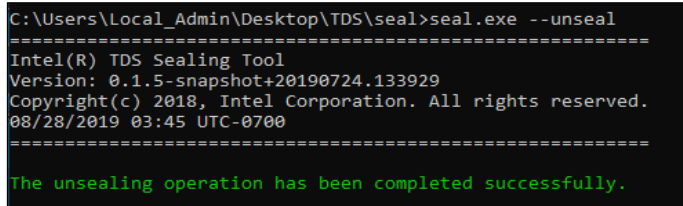


### 24.7.3 TDS\_03

<b>Test ID</b>	<b>TDS_03</b>
<b>Test Case Title</b>	Platform prerequisites
<b>Mandatory/Optional</b>	Mandatory
<b>Test Type</b>	Prerequisite
<b>Description</b>	Checks that the platform prerequisites for Intel® TDS all apply to SUT: <ul style="list-style-type: none"><li>• Platform is an Intel® vPro® machine</li><li>• Platform contains SPI TPM 2.0 module</li></ul>
<b>Objective</b>	To determine if the SUT has the prerequisites necessary for Intel® TDS.
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Check that platform is Intel® AMT capable by running Intel® MEInfo and seeing Intel® AMT is in the output (Disabled or Enabled).</li><li>2. Open TPM.msc and check that Intel® PTT's state is "Ready for use".</li></ol>
<b>Test Pass/Fail Criteria</b>	Test passes when Intel® MEInfo shows Intel® Active Management Technology – Present, and Intel® PTT state is "Ready for use".



## 24.7.4 TDS\_04

<b>Test ID</b>	<b>TDS_04</b>
<b>Test Case Title</b>	Seal device in collection mode
<b>Mandatory/Optional</b>	Mandatory
<b>Test Type</b>	Compliance
<b>Description</b>	Prepare device for measurement collection by running the Seal in collection mode command.
<b>Objective</b>	The device can be prepared for measurement collection
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Run sealing tool in collection mode: Seal.exe --collection_mode_seal -c seal.ini</li> <li>Run unseal command: Seal.exe --unseal</li> </ol>
<b>Test Pass/Fail Criteria</b>	<ol style="list-style-type: none"> <li>For step 1, the green color message indicates the test pass as "The sealing operation has been completed successfully. TDS feature state: Active (measurements collection mode), Seal state: Intact".    <pre> C:\Users\Local_Admin\Desktop\TDS3\Intel_TDS_Sealing-0.2.0&gt;seal.exe --collection_mode_seal ===== Intel(R) TDS Sealing Tool Version: 0.2.0 Copyright(c) 2018-2019, Intel Corporation. All rights reserved. 10/15/2019 06:09 UTC-0700 ===== WARNING: [Seal Config] Measurement Collection Boot enabled. The next boot will collect measurements and disable TDS. WARNING: [Seal Config] Chassis Intrusion Detection has been requested by TDS Configuration and will be enforced during Attestation. Chassis Intrusion Detection should already be enabled in BIOS before running this tool. This is not verified by TDS Seal. The sealing operation has been completed successfully. TDS feature state: Active (measurements collection mode), Seal state: Intact </pre> </li> <li>For step 2, the following message appears:    <pre> C:\Users\Local_Admin\Desktop\TDS\seal&gt;seal.exe --unseal ===== Intel(R) TDS Sealing Tool Version: 0.1.5-snapshot+20190724.133929 Copyright(c) 2018, Intel Corporation. All rights reserved. 08/28/2019 03:45 UTC-0700 ===== The unsealing operation has been completed successfully. </pre> </li> </ol>



## 24.7.5 TDS\_05

<b>Test ID</b>	<b>TDS_05</b>
<b>Test Case Title:</b>	BIOS configuration lock
<b>Mandatory/Optional</b>	Mandatory
<b>Test Type</b>	Compliance
<b>Description</b>	On a platform with Intel® TDS enabled and set, check if BIOS configuration is locked and try accessing BIOS.
<b>Objective</b>	To check if BIOS configuration lock is set on Intel® TDS enabled platforms, and that the lock works in protecting the BIOS from changes.
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. In seal.ini, PlatformMeasurements.ini and svt.ini change set the following configurations: <b>BIOSLockEnabled = 1</b> <b>ChassisIntrusionEnabled= 0</b> <b>SEDLockEnabled = 0</b></li><li>2. Run sealing flow from <a href="#">Section 24.8.1</a> (Full E2E Sealing) and validate the pass criteria is met.</li><li>3. Reboot and try to access BIOS menus through the OEM specific key before OS loads. (By using Intel® IFWI, access to BIOS menu can be done by pressing F2 key during boot.)</li><li>4. Access must be blocked.</li><li>5. Run unseal command: Seal.exe --unseal</li></ol>
<b>Test Pass/Fail Criteria</b>	<ol style="list-style-type: none"><li>1. Test fails if Step 2 fails or BIOS is not locked and hence will be able to open BIOS menus.</li><li>2. Step 5 output is as follows: <pre>C:\Users\Local_Admin\Desktop\TDS\seal&gt;seal.exe --unseal ===== Intel(R) TDS Sealing Tool Version: 0.1.5-snapshot+20190724.133929 Copyright(c) 2018, Intel Corporation. All rights reserved. 08/28/2019 03:45 UTC-0700 ===== The unsealing operation has been completed successfully.</pre></li></ol>

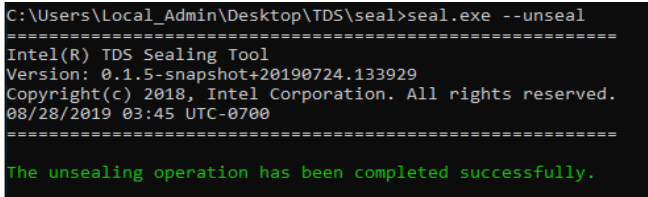


## 24.7.6 TDS\_06

<b>Test ID</b>	<b>TDS_06</b>
<b>Test Case Title</b>	Chassis intrusion lock
<b>Mandatory/Optional</b>	Mandatory
<b>Test Type</b>	Compliance (If chassis intrusion enabled in solution)
<b>Description</b>	On platform with Intel® TDS enabled and set, check if chassis intrusion detection is working
<b>Objective</b>	To check if chassis tampering detection is working when set in TDS
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. In seal.ini, PlatformMeasurements.ini and svt.ini change set the following configurations:  <b>BIOSLockEnabled = 0</b>  <b>ChassisIntrusionEnabled = 1</b>  <b>SEDLockEnabled = 0</b> </li> <li>2. Run sealing flow from <a href="#">Section 24.8.1</a> (Full E2E Sealing) and validate the pass criteria is met.</li> <li>3. Shut down.</li> <li>4. Open the chassis</li> <li>5. Power up and run get state using sealing tool:  Seal.exe --get_state  Output will include the Seal is broken, and the reason is Chassis intrusion detected.</li> <li>6. Run unseal command:  Seal.exe --unseal </li> </ol>
<b>Test Pass/Fail Criteria</b>	<ol style="list-style-type: none"> <li>1. Test pass if the output of step #5 contains the Seal state: broken and the string "Reason #2: 'Chassis Intrusion Detected'".</li> <li>2. Step 6 output is as follows: <div> <pre>C:\Users\Local_Admin\Desktop\TDS\seal&gt;seal.exe --unseal ===== Intel(R) TDS Sealing Tool Version: 0.1.5-snapshot+20190724.133929 Copyright(c) 2018, Intel Corporation. All rights reserved 08/28/2019 03:45 UTC-0700 ===== The unsealing operation has been completed successfully</pre> </div> </li> </ol>



## 24.7.7 TDS\_07

Test ID	TDS_07
Test Case Title	SED lock
Mandatory/Optional	Mandatory
Test Type	Compliance
Description	On a platform with Intel® TDS enabled and set, check if SED is locked
Objective	To check if SED is locked when applying the seal
Procedure	<ol style="list-style-type: none"><li>1. In seal.ini, PlatformMeasurements.ini and svt.ini change set the following configurations: <b>BIOSLockEnabled = 0</b> <b>ChassisIntrusionEnabled = 0</b> <b>SEDLockEnabled = 1</b></li><li>2. Run sealing flow from <a href="#">Section 24.8.1</a> (Full E2E Sealing) until step #9.</li><li>3. Shut down.</li><li>4. Replace the disk.</li><li>5. Power up and run get state using sealing tool: Seal.exe --get_state Output will include the Seal is broken due to disk tampering.</li><li>6. Run unseal command: Seal.exe --unseal</li></ol>
Test Pass/Fail Criteria	<ol style="list-style-type: none"><li>1. Test pass if the output of step #5 contains the Seal state: broken and the string "Reason #4: 'Disk Measurement Failed'".</li><li>2. Step 6 output is as follows: </li></ol>



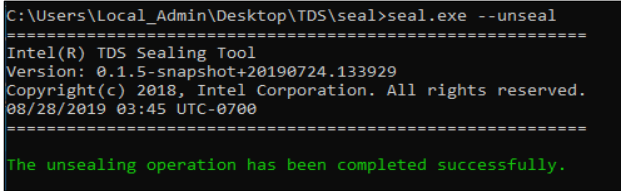
## 24.7.8 TDS\_08

<b>Test ID</b>	<b>TDS_08</b>
<b>Test Case Title</b>	Opt-Out
<b>Mandatory/Optional</b>	Mandatory
<b>Test Type</b>	Compliance
<b>Description</b>	On a platform with Intel® TDS enabled and active: 1. Use a default opt out hotkey to opt out of Intel® TDS flow 2. Use a configured opt out key to opt out of Intel® TDS flow
<b>Objective</b>	To check if opt out feature works, customizable opt out key works, and that once the opt-out is performed, the BIOS is no longer locked.
<b>Procedure</b>	<ol style="list-style-type: none"> <li>Run test TDS_05 steps 1-4 and validate it passes.</li> <li>Reboot and wait for PBA screen and enter default opt out keys {CTRL+ALT+o, CTRL+ALT+p, CTRL+ALT+t, CTRL+ALT+o}. To check opt out screen: Select "Yes"</li> </ol> <div style="background-color: black; color: white; padding: 10px; text-align: center;"> <p>Opting out of Intel® Trusted Device Setup requires you to contact your IT department to use this device.</p> <p>Do you really want to opt out?</p> <p>Yes <input type="button" value="No"/></p> </div> <ol style="list-style-type: none"> <li>On OS, Run seal.exe --get_state</li> <li>Seal state must be broken. Run unseal command: Seal.exe --unseal</li> <li>Repeat steps above and use the configured opt out keys.</li> </ol> <p><b>Note:</b> To change default, opt out keys, Open seal.ini file from Seal tool kit. Change CustomOptOutEnabled to 1 and change the OptOutHotKey to any optout keys that are not default (Allowed values are described in Section 4.8. "Opt-out hotkey" of the Intel® TDS_Sealing_Readme.txt file.</p>
<b>Test Pass/Fail Criteria</b>	<p>Test passes if default opt-out keys work, and custom opt-out keys works. Sealing tool get state will show Seal state is Broken and the reason is "Reason #1: 'Aborted by the user - BIOS lock removed'":</p> <div style="background-color: black; color: white; padding: 5px;"> <p>Seal log contains 3 events:</p> <ul style="list-style-type: none"> <li>- 10/15/2019 06:25 UTC-0700 - Seal Configured (Seal Instance ID: 3938101247)</li> <li>- 10/15/2019 06:25 UTC-0700 - Seal Enabled</li> <li>- 10/15/2019 06:40 UTC-0700 - Seal Broken (Boot Counter: 4, TDS Execution Counter: 4, Reason #1: 'Aborted by the user - BIOS Lock removed')</li> </ul> </div>

## 24.7.9 TDS\_09

<b>Test ID</b>	<b>TDS_09</b>
<b>Test Case Title</b>	Dropship boot unseal check
<b>Mandatory/Optional</b>	Mandatory



<b>Test Type</b>	Compliance
<b>Description</b>	Check if unseal works properly.
<b>Objective</b>	To check the initial step by the end user, operates as expected.
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Apply seal if not applied (Using TDS_05 until step 4)</li><li>2. Using Sealing tool to unseal the device with the following command: Seal.exe --unseal The following message appears: </li><li>3. Run seal.exe --get_state Output will include "TDS feature state: Inactive, Seal state: Disabled".</li></ol>
<b>Test Pass/Fail Criteria</b>	<p>Test passes when:</p> <ol style="list-style-type: none"><li>1. Step 2 ends with the message "The unsealing operation has been completed successfully".</li><li>2. Step 3 ends with the output "Intel® TDS feature state: Inactive, Seal state: Disabled".</li></ol>





## 24.8 Backup

### 24.8.1 Full E2E Sealing

Title	Full E2E Sealing
<p><b>Procedure</b></p>	<ol style="list-style-type: none"> <li>Run sealing tool in collection mode: Seal.exe --collection_mode_seal -c seal.ini</li> <li>Shutdown the machine using the command: shutdown /t 0 /f /s Then power on and wait for OS</li> <li>In PMT tool folder, open PlatformMeasurements.ini and do the following:             <ol style="list-style-type: none"> <li>Validate the field ExpiryDate=YYYY-MM-DD has future date</li> <li>b.Assert [Seal Configuration] in seal.ini in Seal tool folder matches the configuration in the PlatformMeasurements.ini file in PMT folder</li> <li>Save file and exit.</li> </ol> </li> <li>Open CMD with Admin privileges and run the following command to generate the measurements file PlatformMeasurements.bin: Intel_TDS_PMTx64.exe GENPLATMSRFULL .</li> <li>To Sign the PMF, Run the following command: Intel_TDS_PMTx64.exe GENSIGNEDBIN -fl signedBin.bin</li> <li>This command will generate a signed PMF binary file signedBin.bin. Copy signedBin.bin to sealing tool folder</li> <li>Seal the machine with the following command: Seal.exe --seal -g signedBin.bin</li> <li>The message "machine sealed successfully" is outputted.</li> <li>Shut down the machine.</li> <li>Boot the machine and observe the PBA screen is seen instead of BIOS:</li> </ol> <div> </div> <ol style="list-style-type: none"> <li>On OS, run sealing tool with the command: seal.exe --get_state The output will include "Intel® TDS feature state: Active, Seal State: Intact".</li> <li>Copy <b>TDS_TL3_Seal_Identity_File_***.csv</b> from seal folder to SVT folder.</li> <li>Run svt.exe --validate and make sure the tests are passed.</li> </ol>
<p><b>Test Pass/Fail Criteria</b></p>	<p>Test passes when the following applies:</p> <ol style="list-style-type: none"> <li>PBA screen seen on boot in step 10.</li> <li>Step 11 output is "Intel® TDS feature state: active, Seal State: Intact".</li> <li>Step 13 tests are passed.</li> </ol>

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## 25 Platform SKU Emulation Check

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### Overview:

The test case in this chapter was created to verify that the image being used on platforms using ES silicon is using SKU Emulation. This is done verify that the to ensure that customer are using the correct SKU configuration for the platform design(s) they are planning to ship.

### Tools for Testing:

- **Intel® Platform Enablement Test Suite (Intel® PETS):** Use latest version of this kit. Refer to the Intel® PETS user guide available in the Intel® CSME Compliance kit for details instructions on how to load and setup the Intel® PETS software.
- **ME Information tool:** EFI (MEInfo.efi), Windows\* 32-bit (MEInfoWin.exe), and Windows\* 64-bit operating systems (MEInfoWin.exe64).

### Test Environment:

The System Under Test (SUT) is to be configured in manual configuration mode a with wired LAN or wireless LAN dynamic IP address. The DHCP server connecting the SUT and Management Console (MC) must be configured to ensure that the wired LAN and wireless LAN addresses reside on separate subnets. The MC could be a laptop or desktop system running a version of Windows\* supported by PETS. The network configuration consists of a hub or switch, network cables, and a wireless Access Point (AP).

### 25.1 Test Coverage Summary

Test ID	Test Case Title	PETS/Manual	Form Factor	Network Factor
SKUEM_001	SKU Emulation check for ES Silicon	PETS	DT/MB	N/A



## 25.2 Descriptor Mode Test

Test ID	SKUEM_001																												
Test Case Title	SKU Emulation check for ES Silicon																												
Mandatory/Optional	Mandatory																												
Description	Proper emulation of the target platform SKU is needed in order to ensure that customer design and layout aligns properly with the HSIO lanes available for USB, PCIe and GbE. This test will confirm that the platform image is not set to Super SKU mode.																												
Objective	Verify that the platform image is using SKU emulation on ES silicon.																												
Procedure	1. Boot to the target OS. 2. Run MEInfo and check the PCH Device ID.																												
Test Pass/Fail Criteria	Test passes if PCH Device ID is not one of the following Super SKU values. <table><tr><th>PCH Type</th><th colspan="2">PCH Device ID</th></tr><tr><td rowspan="2">TGP-H</td><td colspan="2">4381h</td></tr><tr><td colspan="2">4382h</td></tr><tr><td>TGP-LP UP3</td><td colspan="2">A081h</td></tr><tr><td>TGP-LP UP4</td><td colspan="2">A086h</td></tr></table>			PCH Type	PCH Device ID		TGP-H	4381h		4382h		TGP-LP UP3	A081h		TGP-LP UP4	A086h													
PCH Type	PCH Device ID																												
TGP-H	4381h																												
	4382h																												
TGP-LP UP3	A081h																												
TGP-LP UP4	A086h																												
Emulated SKU IDs	The customer should verify that the correct SKU emulation setting is being used for their platform design.  Emulated SKU IDs: <table><tr><th>PCH Type</th><th>Emulated SKU</th><th>PCH Device ID</th></tr><tr><td rowspan="8">TGP-H</td><td>Q590</td><td>4384h</td></tr><tr><td>Z590</td><td>4385h</td></tr><tr><td>H570</td><td>4386h</td></tr><tr><td>B560</td><td>4387h</td></tr><tr><td>H510</td><td>4388h</td></tr><tr><td>WM590</td><td>4389h</td></tr><tr><td>QM580</td><td>438Ah</td></tr><tr><td>HM570</td><td>438Bh</td></tr><tr><td>TGP-LP UP3</td><td>Premium UP3</td><td>A082h</td></tr><tr><td>TGP-LP UP4</td><td>Premium UP4</td><td>A087h</td></tr></table>			PCH Type	Emulated SKU	PCH Device ID	TGP-H	Q590	4384h	Z590	4385h	H570	4386h	B560	4387h	H510	4388h	WM590	4389h	QM580	438Ah	HM570	438Bh	TGP-LP UP3	Premium UP3	A082h	TGP-LP UP4	Premium UP4	A087h
PCH Type	Emulated SKU	PCH Device ID																											
TGP-H	Q590	4384h																											
	Z590	4385h																											
	H570	4386h																											
	B560	4387h																											
	H510	4388h																											
	WM590	4389h																											
	QM580	438Ah																											
	HM570	438Bh																											
TGP-LP UP3	Premium UP3	A082h																											
TGP-LP UP4	Premium UP4	A087h																											

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# A Intel® Trusted Execution Technology (Intel® TXT)

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## A.1 Provisioning Trusted Platform Module (TPM) for Intel® TXT

### A.1.1 TPM 1.2 Background

Intel® TXT relies on three indices created in the TPM NVRAM area for operation:

1. AUX INDEX—This is an architectural index used by the ACMS.
2. PO (Platform Owner) INDEX—This is LCP index intended to be used by the PO (IT, System Integrator, End User) to define launch control policy appropriate for the deployed environment.

Because the AUX and PS indices are used by Intel® TXT for basic operation, these indices must be properly defined, provisioned and protected before shipment to ensure proper Intel® TXT operation. Since the PO index is intended to be used in the deployed environment, this index should not be defined by platform suppliers in shipping systems.

### A.1.2 TPM 1.2 Minimum Requirements

OEM/ODM need to make sure that following TPM provisioning steps are done prior to shipping the Intel® TXT enabled platform.

1. Define Auxiliary index

### A.1.3 TPM 1.2 Intel Provided Development Tools

To enable BIOS testing and facilitate TPM provisioning tool development, Intel has provided the following:

*ACM Packages/Bin*—The Bin directory in the ACM packages contain provisioning scripts that are appropriate for the ACM being used. Because these provisioning scripts may change with the ACM releases, BIOS evaluators are encouraged to use the scripts that come with each ACM release.

*Intel® TPM BIOS Development Kit (Intel® TPM BDK)* – This kit contains scripts and reference code that can be used by the TPM vendor or OEM tool teams to create EFI based provisioning scripts appropriate for their manufacturing process. This kit provides the IBV/OEM with EFI based sample code and executable that will provision a TPM for use with Intel® TXT. This tool kit contains documentation and build instructions that the user can use to create their own tools.

**Note:** These kits are for **reference only** and the example scripts should NOT be used to provision the TPM for BIOS testing or production provisioning.



The following sections describe the correct sequence to provision the TPM using the DOS scripts provided with ACM packages. The first section describes the required provisioning for system under test (SUT) based on Engineering Sample (ES) and debugged signed ACM (typically rev 0.5 to 0.9). The final section describes the required provisioning for SUT based on Qual Samples (QS) and production signed ACM (these are 0.9 NPW and 1.0+ releases).

## A.1.4 TPM 1.2 Provisioning for Debug Signed ACM

### A.1.4.1 Required—Provisioning for Debugged Signed ACM

With the debugged signed ACM the provisioning steps below are required for Intel® TXT operation. These steps are applicable to ACM releases from 0.5 to 0.9 that are debugged signed.

1. **AUX2\_DEF.BAT**—To define the AUX index space

### A.1.4.2 Optional—Provisioning for Debugged Signed ACM

If test plan includes test cases for platform owner (PO) policies, following scripts can be used to facilitate the PO provision process. These scripts are not provided with ACM package and are available upon request.

1. **EK.BAT**—If your TPM does not provide default EK
2. **TAKE\_OWN.BAT**—Ownership is required for PO definition
3. **POA\_DEF.BAT**—To define the PO index space
4. **Install your test PO policy**—The POA\_ANY.BAT can be modified to make the policy appropriate for your testing SW

## A.1.5 TPM 1.2 Provisioning for Production Signed ACM

### A.1.5.1 Required—Provisioning for Production Signed ACM

Production signed ACM requires that the NV indices be locked. The exception to this lock requirement are the ACM that has been tagged as non-production worthy (NPW). For NPW production signed ACM, the NV indices do not have to be locked however the PS index needs to be provisioned to allow NPW ACM execution. The appropriate PS provisioning scripts are distributed with the ACM.

For production signed ACM the provisioning steps are listed below. These ACMs typically are releases 1.0 and higher or 0.9 releases that are tagged NPW. The steps are similar to debug signed ACM with the additional locking requirement or the PS provision for NPW ACM execution

1. **AUX2\_DEF.BAT**—To define the AUX index space
2. **NV\_LOCK.BAT**—This locks the indices in the TPM NVRAM

**Note:** This locking is permanent on most TPM. Some TPM do provide a RevokeTrust mechanism that would clear the lock.



#### A.1.5.2 TPM 1.2 Optional—Provisioning for Production Signed ACM

Similar to optional provisioning for the debug signed ACM above. If the test plan includes test cases for platform owner (PO) policies, following scripts can be used to facilitate the PO provision process. These scripts are not provided with ACM package and are available upon request.

1. **EK.BAT**—If your TPM does not provide default EK
2. **TAKE\_OWN.BAT**—Ownership is required for PO definition
3. **PO\_DEF.BAT**—To define the PO index space
4. **Install test PO policy**—The PO\_ANY.BAT can be modified to make the policy appropriate for your testing SW

#### A.1.6 TPM 2.0 Background

Intel® TXT relies on TPM capability and requirements are defined by the Trusted Computer Group (TCG), an industry initiative “formed to develop, define and promote open, vendor-neutral, industry standards for trusted computing building blocks and software interfaces across multiple platforms.

##### Platform Hierarchy:

Unlike TPM 1.2 family, where the OEM had to create TPM objects (Example: AUX and PS Policy NVRAM Indexes) and then lock the TPM preventing anyone from deleting or modifying their definitions, TPM 2.0 defines 3 hierarchies that are independent of each other. These are the Platform Hierarchy, Storage Hierarchy, and Endorsement Hierarchy.

The Platform Hierarchy is dedicated for the platform vendor while the Storage Hierarchy and Endorsement Hierarchy are dedicated for the platform owner. This document only deals with the Platform Hierarchy (PH). Each hierarchy has its own authorization value (AuthValue) and authorization policy (authPolicy). More on authorization policies later, but authPolicy is an alternative way to demonstrate authorization to use the PH.

This means that there is no longer the notion of a LOCKED TPM and the OEM will now be able to add, delete, and provision its TPM objects at any time. Unlike the other hierarchies, which have persistent authorization values, the PH authValue and authPolicy are cleared each time the platform resets. It is the BIOS responsibility to establish the PH authValue (and optionally the PH authPolicy) on each platform reset.

The notion is that BIOS will set PH authValue to a random value, use that value if it needs to perform any operations that require PH authorization and then flush that value from memory (or store it in a protected location) before any executing any untrusted code (option ROMs, boot code, and so forth.).

#### A.1.7 TPM 2.0 Minimum Requirements

The OEM must provision the TPM before the platform is put into use. This may be done before the TPM is attached to the platform, during the platform manufacturing/testing process, or automatically the first time the platform boots. At a minimum this requires:

1. Creating the AUX Index



## A.1.8 TPM 2.0 Intel Provided Development Tools

To enable BIOS testing and facilitate TPM provisioning tool development, Intel has provided the following:

*ACM Packages*—The root directory in the ACM packages contain provisioning script(TPM2Prov.efi) that is appropriate for the ACM being used. Because the provisioning script may change with the ACM releases, BIOS evaluators are encouraged to use the script that come with each ACM release.

*Intel® TPM BIOS Development Kit (Intel® TPM BDK)* – This kit contains scripts and reference code that can be used by the TPM vendor or OEM tool teams to create EFI based provisioning scripts appropriate for their manufacturing process. This kit provides the IBV/OEM with EFI based sample code and executable that will provision a TPM for use with Intel® TXT. This tool kit contains documentation and build instructions that the user can use to create their own tools. **(TPM2prov.efi)**.

**Note:** These kits are for **reference only** and the example scripts should NOT be used to provision the TPM for BIOS testing or production provisioning.

## A.1.9 TPM 2.0 Provisioning for Debug Signed ACM

### A.1.9.1 Required—Provisioning for Debugged Signed ACM

With the debugged signed ACM the provisioning steps below are required for Intel® TXT operation. These steps are applicable to ACM releases from 0.5 to 0.9 that are debugged signed.

Once you download the ACM kit, user needs to complete the following two steps.

1. **Define\_AUX.nsh** —To define the AUX index space

Below is a sample output observed on execution of TPM provisioning commands:

#### 1. Define\_AUX.nsh

```
Define_AUX.nsh
2.0 FS0:\TPM2ProvTool\> echo -off
Creating Aux Index ...
Clearing AUXDeletionControl flag in PS Policy
Start Policy Session
Policy OR (Branch A, Branch B, Branch C)
Writing PS Policy to clear AUXDeletionControl flag
Flush Session 0
AUX Define
```

## A.1.10 TPM 2.0 Provisioning for Production Signed ACM

### A.1.10.1 Required—Provisioning for Production Signed ACM

Tool for TPM 2.0 Provisioning for Production Signed ACM will be released at the Production Candidate (PC) milestone of Broadwell Platform.



## A.2 Intel® TXT Trusted Boot (Tboot) Usage

Intel Corporation has submitted TXT reference code (Tboot) to sourceforge which enables Xen\* and Linux\* to use Intel® TXT for verified launch to build an Intel® TXT MLE. An Intel® TXT MLE (Tboot launched Xen\* or Linux\*) is an excellent tool for Intel® TXT checkout.

In addition to verifying that the processor, chipset, TPM and AC modules can collaborate do a measured launch, tboot has a descriptive serial output that can help root cause Intel® TXT measured launch issues.

This section describes how to use tboot-linux and tboot-xen for Intel® TXT checkout.

### A.2.1 Available Tboot Test Images

#### A.2.1.1 Pre-Built Tboot-Linux\* Live Image

To facilitate Intel® TXT evaluation, Intel has provided a Tboot evaluation kit, *Intel® Trusted Execution Technology Evaluation Kit—Trusted Boot (tboot) Usage Image*. This kit contains an .ISO image of a bootable Tboot-Linux\* environment using Fedora 19. This .ISO image can be used to create a bootable MLE on a USB Drive or DVD.

For complete instruction on how build a Tboot-Linux\* image refer to the README file located at the Mercurial Repo (<http://www.bughost.org/repos.hg/tboot.hg/file/9c733d6c3f40/README>).

### A.2.2 Invoking Tboot

With a bootable tboot image prepared either through using the Live Image or by building it from the reference code, invoking tboot is just a matter of selecting the tboot option from the grub menu. Below are the typical steps needed to launch tboot:

1. Verify that platform is ready for Intel® TXT measured launch
2. Enable all the required settings in the BIOS: TPM, Intel® VT, Intel® VT-d, Intel® TXT
3. Boot the system and select the tboot entry from grub menu.

### A.2.3 Verifying Tboot Launch

#### A.2.3.1 Using txt-stat

If the tboot launch completed into either Linux\* or Xen\*, the Linux\* executable **txt-stat** can be used to verify a successful launch. **txt-stat** is included in the tboot package. It distributed with the Tboot-Linux\* Live Image, refer the package instruction for details. **txt-stat** is also compiled by default if the tboot package was compiled at the root level.

To run **txt-stat**:

1. Login to MLE as root
2. Open a shell
3. Change to the directory that contains **txt-stat**





4. Invoke **txt-stat** from the command line using

```
shell> txt-stat
```

The **txt-stat** command will report the current status of your TXT environment. You may also access the txt-stat 'log' if uses LiveUSB for launching the Tboot LiveImage. Log file is stored on your USB flash drive under root/logs folder.

To confirm successful execution, look for the following entry in your **txt-stat** output:

```
*****
      TXT measured launch: TRUE
      secrets flag set: TRUE
*****
```

### A.2.3.2 Sample txt-stat Output

Intel(r) TXT Configuration Registers:

```
STS: 0x00018091
      sender_done: TRUE
      sexit_done: FALSE
      mem_unlock: TRUE
      mem_config_lock: FALSE
      private_open: TRUE
      mem_config_ok: FALSE
ESTS: 0x00
      txt_reset: FALSE
      txt_wake_error: FALSE
E2STS: 0x0000000000000006
      slp_entry_error: FALSE
      secrets: TRUE
      block_mem: TRUE
      reset: FALSE
ERRORCODE: 0x00000000
DIDVID: 0x00000001b0018086
      vendor_id: 0x8086
      device_id: 0xb001
      revision_id: 0x1
SINIT.BASE: 0xaaaf0000
SINIT.SIZE: 131072B (0x20000)
HEAP.BASE: 0xaaaf2000
HEAP.SIZE: 917504B (0xe0000)
DPR: 0x00000000ab000041
      lock: TRUE
      top: 0xab000000
      size: 4MB (4194304B)
*****
      TXT measured launch: TRUE
      secrets flag set: TRUE
*****
ERROR: reading TXT heap failed by read()
TBOOT log:
      max_size=7fe4
```



```
curr_pos=4d51
buf:
TBOOT: ***** TBOOT *****
TBOOT: 2013-11-21 22:24 -0400 206:9c733d6c3f40
TBOOT: *****
TBOOT: command line: boot=linux logging=vga,serial,memory
TBOOT: BSP is cpu 0
TBOOT: original e820 map:
TBOOT: 0000000000000000 - 000000000009bc00 (1)
TBOOT: 000000000009bc00 - 00000000000a0000 (2)
TBOOT: 00000000000a0000 - 0000000000010000 (2)
TBOOT: 0000000000010000 - 00000000000aa90d00 (1)
TBOOT: 00000000000aa90d00 - 00000000000aa9e700 (2)
TBOOT: 00000000000aa9e700 - 00000000000aabe700 (4)
TBOOT: 00000000000aabe700 - 00000000000aabff00 (3)
TBOOT: 00000000000aabff00 - 00000000000aac0000 (1)
TBOOT: 00000000000aac0000 - 0000000000014e0000 (1)
TBOOT: 0000000000014e0000 - 00000000000b000000 (2)
TBOOT: 00000000000b000000 - 00000000000fc00000 (2)
TBOOT: 00000000000fc00000 - 00000000000fec0100 (2)
TBOOT: 00000000000fec0100 - 00000000000fed1400 (2)
TBOOT: 00000000000fed1400 - 00000000000fed1a00 (2)
TBOOT: 00000000000fed1a00 - 00000000000fed2000 (2)
TBOOT: 00000000000fed2000 - 00000000000fee0100 (2)
TBOOT: 00000000000fee0100 - 00000000000ff98000 (2)
TBOOT: 00000000000ff98000 - 00000000000ffc0000 (2)
TBOOT: 00000000000ffc0000 - 00000000000100000000 (2)
TBOOT: TPM is ready

...

txt-stat message deleted for clarity.

...

BOOT: VMXOFF done for cpu 6
TBOOT: cpu 6 waking up, SIPI vector=10000
TBOOT: VMXOFF done for cpu 1
TBOOT: cpu 1 waking up, SIPI vector=10000
TBOOT: VMXOFF done for cpu 3
TBOOT: cpu 3 waking up, SIPI vector=10000
TBOOT: VMXOFF done for cpu 5
TBOOT: cpu 5 waking up, SIPI vector=10000
TBOOT: VMXOFF done for cpu 7
TBOOT: cpu 7 waking up, SIPI vector=10000
```



### A.2.3.3 Using Serial Port

The best method to verify a tboot launch is to view the serial output. With the serial connection connected to the SUT with baud rate at 115200, the tboot log entry can view to confirm successful measured launching.

**Note:** While ACM serial out debug message requires BIOS to explicitly use 0x3F8 port for capturing the log, Tboot LiveImage serial can be captured using any available/connect serial (COM) port on the platform.

Key entries to verify from the serial output are:

1. Confirmation from tboot that HW and SW components are ready for Intel® TXT measured launch recognized. These component confirmations are as follow:
  - i. TBOOT: TPM is ready
  - ii. TBOOT: TXT chipset and all needed capabilities present
  - iii. TBOOT: CPU is ready for SENTER
  - iv. TBOOT: SINIT matches platform
2. Confirmation that tboot is executing a measured launch using GETSEC[SENDER]. The message to verify this is:
  - i. TBOOT: executing GETSEC[SENDER]...
3. The next entries to look for are confirmations that measured launch have completed successfully. The messages to verify this are:
  - i. TBOOT: measured launch succeeded
  - ii. TBOOT: set LT.CMD.SECRETS flag
4. Last step is confirmation that tboot has successful transferred control to MLE. Below are examples of transfer messages to Linux\* and Xen\*.

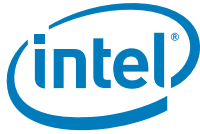
- i. TBOOT: transferring control to kernel @0x00c00000...
- ii. TBOOT: transferring control to xen @0x00100000...

### A.2.3.4 Sample Serial Output—Tboot Linux\*

Below is a sample serial port output captured from an Intel® TXT Tboot-Linux\* measured boot.

This log may be different from the log in the validation environment due to differences in system configuration, BIOS implementation and Intel® TXT patch version applied.

```
TBOOT: ***** TBOOT *****
TBOOT: 2013-11-21 22:24 -0400 206:9c733d6c3f40
TBOOT: *****
TBOOT: command line: boot=linux logging=vga,serial,memory
TBOOT: BSP is cpu 0
TBOOT: original e820 map:
TBOOT: 0000000000000000 - 000000000009bc00 (1)
TBOOT: 000000000009bc00 - 00000000000a0000 (2)
TBOOT: 00000000000a0000 - 0000000000100000 (2)
TBOOT: 0000000000100000 - 00000000aa90d000 (1)
TBOOT: 00000000aa90d000 - 00000000aa9e7000 (2)
TBOOT: 00000000aa9e7000 - 00000000aabe7000 (4)
TBOOT: 00000000aabe7000 - 00000000aabff000 (3)
```



```
TBOOT: 00000000aabff000 - 00000000aac00000 (1)
TBOOT: 0000000100000000 - 000000014e000000 (1)
TBOOT: 00000000aac00000 - 00000000b0000000 (2)
TBOOT: 00000000f8000000 - 00000000fc000000 (2)
TBOOT: 00000000fec00000 - 00000000fec01000 (2)
TBOOT: 00000000fed10000 - 00000000fed14000 (2)
TBOOT: 00000000fed18000 - 00000000fed1a000 (2)
TBOOT: 00000000fed1c000 - 00000000fed20000 (2)
TBOOT: 00000000fee00000 - 00000000fee01000 (2)
TBOOT: 00000000ff980000 - 00000000ffc00000 (2)
TBOOT: 00000000ffd80000 - 0000000100000000 (2)
TBOOT: TPM is ready
TBOOT: TPM nv_locked: FALSE
TBOOT: TPM timeout values: A: 0, B: 0, C: 10, D: 10
TBOOT: TPM: tpm_get_nvindex_size() response size incorrect
TBOOT: failed to get actual policy size in TPM NV
TBOOT: failed to read policy from TPM NV, using default
TBOOT: policy:
TBOOT: version: 2
TBOOT: policy_type: TB_POLTYPE_CONT_NON_FATAL
TBOOT: hash_alg: TB_HALG_SHA1
TBOOT: policy_control: 00000001 (EXTEND_PCR17)
TBOOT: num_entries: 2
TBOOT: policy entry[0]:
TBOOT: mod_num: 0
TBOOT: pcr: none
TBOOT: hash_type: TB_HTYPE_ANY
TBOOT: num_hashes: 0
TBOOT: policy entry[1]:
TBOOT: mod_num: any
TBOOT: pcr: 19
TBOOT: hash_type: TB_HTYPE_ANY
TBOOT: num_hashes: 0
TBOOT: TPM: write nv 20000002, offset 00000000, 00000004 bytes, return =
00000000
2
TBOOT: Error: write TPM error: 0x2.
TBOOT: no policy in TPM NV.
TBOOT: IA32_FEATURE_CONTROL_MSR: 0000ff07
TBOOT: CPU is SMX-capable
TBOOT: CPU is VMX-capable
TBOOT: SMX is enabled
TBOOT: TXT chipset and all needed capabilities present
TBOOT: TXT.ERRORCODE=0
TBOOT: LT.ESTS=0
TBOOT: IA32_FEATURE_CONTROL_MSR: 0000ff07
TBOOT: CPU is SMX-capable
TBOOT: CPU is VMX-capable
TBOOT: SMX is enabled
TBOOT: TXT chipset and all needed capabilities present
```



```

TBOOT: bios_data (@aaf20008, 2c):
TBOOT: version: 3
TBOOT: bios_sinit_size: 0x0 (0)
TBOOT: lcp_pd_base: 0x0
TBOOT: lcp_pd_size: 0x0 (0)
TBOOT: num_logical_procs: 8
TBOOT: flags: 0x00000000
TBOOT: CR0 and EFLAGS OK
TBOOT: supports preserving machine check errors
TBOOT: CPU is ready for SENTER
TBOOT: checking previous errors on the last boot.
      TPM: read nv index 20000002 offset 00000000, return value = 00000002
TBOOT: Error: read TPM error: 0x2.
TBOOT: last boot has no error.
TBOOT: chipset ids: vendor: 0x8086, device: 0xb001, revision: 0x1
TBOOT: chipset production fused: 0
TBOOT: checking if module SNB_SINIT_20100502_debug.bin is an SINIT for
this platform...
TBOOT: 2 ACM chipset id entries:
TBOOT:      vendor: 0x8086, device: 0xb001, flags: 0x1, revision: 0x1,
extended
: 0x1
TBOOT: SINIT matches platform
TBOOT: copied SINIT (size=b000) to aaf00000
TBOOT: AC mod base alignment OK
TBOOT: AC mod size OK
TBOOT: AC module header dump for SINIT:
TBOOT: type: 0x2 (ACM_TYPE_CHIPSET)
TBOOT: length: 0xa1 (161)
TBOOT: version: 0
TBOOT: chipset_id: 0xb001
TBOOT: flags: 0x8000
TBOOT: pre_production: 0
TBOOT: debug_signed: 1
TBOOT: vendor: 0x8086
TBOOT: date: 0x20100502
TBOOT: size*4: 0xb000 (45056)
TBOOT: code_control: 0x0
TBOOT: entry point: 0x00000008:00003094
TBOOT: scratch_size: 0x8f (143)
TBOOT: info_table:
TBOOT: uuid: {0x7fc03aaa, 0x46a7, 0x18db, 0xac2e,
{0x69, 0x8f, 0x8d, 0x41, 0x7f, 0x5a}}
TBOOT:      ACM_UUID_V3
TBOOT: chipset_acm_type: 0x1 (SINIT)
TBOOT: version: 3
TBOOT: length: 0x28 (40)
TBOOT: chipset_id_list: 0x4e8
TBOOT: os_sinit_data_ver: 0x5
TBOOT: min_mle_hdr_ver: 0x00020000

```



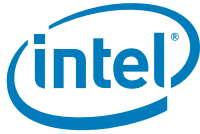
```
TBOOT: capabilities: 0x0000000e
TBOOT:     rlp_wake_getsec: 0
TBOOT:     rlp_wake_monitor: 1
TBOOT:     ecx_pgtbl: 1
TBOOT: acm_ver: 16
TBOOT: chipset list:
TBOOT: count: 2
TBOOT: entry 0:
TBOOT:     flags: 0x1
TBOOT:     vendor_id: 0x8086
TBOOT:     device_id: 0xb001
TBOOT:     revision_id: 0x1
TBOOT:     extended_id: 0x1
TBOOT: entry 1:
TBOOT:     flags: 0xb0008086
TBOOT:     vendor_id: 0x1
TBOOT:     device_id: 0x0
TBOOT:     revision_id: 0x0
TBOOT:     extended_id: 0x0
TBOOT: file addresses:
TBOOT:   &_start=00803000
TBOOT:   &_end=0087ccb4
TBOOT:   &_mle_start=00803000
TBOOT:   &_mle_end=00821000
TBOOT:   &_post_launch_entry=00803020
TBOOT:   &_txt_wakeup=008031f0
TBOOT:   &g_mle_hdr=008175c0
TBOOT: MLE header:
TBOOT:   uuid={0x9082ac5a, 0x476f, 0x74a7, 0x5c0f,
          {0x55, 0xa2, 0xcb, 0x51, 0xb6, 0x42}}
TBOOT:   length=34
TBOOT:   version=00020001
TBOOT:   entry_point=00000020
TBOOT:   first_valid_page=00000000
TBOOT:   mle_start_off=0
TBOOT:   mle_end_off=1e000
TBOOT:   capabilities: 0x00000007
TBOOT:     rlp_wake_getsec: 1
TBOOT:     rlp_wake_monitor: 1
TBOOT:     ecx_pgtbl: 1
TBOOT: MLE start=803000, end=821000, size=1e000
TBOOT: ptab_size=3000, ptab_base=00800000
TBOOT: bios_data (@aaf20008, 2c):
TBOOT:   version: 3
TBOOT:   bios_sinit_size: 0x0 (0)
TBOOT:   lcp_pd_base: 0x0
TBOOT:   lcp_pd_size: 0x0 (0)
TBOOT:   num_logical_procs: 8
TBOOT:   flags: 0x00000000
TBOOT: discarding RAM above reserved regions: 0xaabff000 - 0xaac00000
```



```

TBOOT: min_lo_ram: 0x0, max_lo_ram: 0xaa90d000
TBOOT: min_hi_ram: 0x100000000, max_hi_ram: 0x14e000000
TBOOT: no LCP module found
TBOOT: os_sinit_data (@aaf30154, 64):
TBOOT: version: 5
TBOOT: mle_ptab: 0x800000
TBOOT: mle_size: 0x1e000 (122880)
TBOOT: mle_hdr_base: 0x145c0
TBOOT: vtd_pmr_lo_base: 0x0
TBOOT: vtd_pmr_lo_size: 0xaa800000
TBOOT: vtd_pmr_hi_base: 0x100000000
TBOOT: vtd_pmr_hi_size: 0x4e000000
TBOOT: lcp_po_base: 0x0
TBOOT: lcp_po_size: 0x0 (0)
TBOOT: capabilities: 0x00000002
TBOOT:     rlp_wake_getsec: 0
TBOOT:     rlp_wake_monitor: 1
TBOOT:     ecx_pgtbl: 0
TBOOT: efi_rsdtr_ptr: 0x0
TBOOT: setting MTRRs for acmod: base=aaf00000, size=b000, num_pages=11
TBOOT: executing GETSEC[SENTER]...
TBOOT: ***** TBOOT *****
TBOOT: 2010-06-21 22:24 -0400 206:9c733d6c3f40
TBOOT: *****
TBOOT: command line: boot=linux logging=vga,serial,memory
TBOOT: BSP is cpu 0
TBOOT: original e820 map:
TBOOT: 0000000000000000 - 000000000009bc00 (1)
TBOOT: 000000000009bc00 - 00000000000a0000 (2)
TBOOT: 00000000000a0000 - 0000000000100000 (2)
TBOOT: 0000000000100000 - 00000000aa90d000 (1)
TBOOT: 00000000aa90d000 - 00000000aa9e7000 (2)
TBOOT: 00000000aa9e7000 - 00000000aabe7000 (4)
TBOOT: 00000000aabe7000 - 00000000aabff000 (3)
TBOOT: 00000000aabff000 - 00000000aac00000 (1)
TBOOT: 00000000aac00000 - 0000000014e00000 (1)
TBOOT: 00000000aac00000 - 00000000b0000000 (2)
TBOOT: 00000000b0000000 - 00000000fc000000 (2)
TBOOT: 00000000fec00000 - 00000000fec01000 (2)
TBOOT: 00000000fed10000 - 00000000fed14000 (2)
TBOOT: 00000000fed18000 - 00000000fed1a000 (2)
TBOOT: 00000000fed1c000 - 00000000fed20000 (2)
TBOOT: 00000000fee00000 - 00000000fee01000 (2)
TBOOT: 00000000ff980000 - 00000000ffc00000 (2)
TBOOT: 00000000ffd80000 - 0000000010000000 (2)
TBOOT: TPM is ready
TBOOT: TPM nv_locked: FALSE
TBOOT: TPM timeout values: A: 0, B: 0, C: 10, D: 10
TBOOT: TPM: tpm_get_nvindex_size() response size incorrect
TBOOT: failed to get actual policy size in TPM NV

```



```
TBOOT: failed to read policy from TPM NV, using default
TBOOT: policy:
TBOOT:  version: 2
TBOOT:  policy_type: TB_POLTYPE_CONT_NON_FATAL
TBOOT:  hash_alg: TB_HALG_SHA1
TBOOT:  policy_control: 00000001 (EXTEND_PCR17)
TBOOT:  num_entries: 2
TBOOT:  policy entry[0]:
TBOOT:  mod_num: 0
TBOOT:  pcr: none
TBOOT:  hash_type: TB_HTYPE_ANY
TBOOT:  num_hashes: 0
TBOOT:  policy entry[1]:
TBOOT:  mod_num: any
TBOOT:  pcr: 19
TBOOT:  hash_type: TB_HTYPE_ANY
TBOOT:  num_hashes: 0
TBOOT: TPM: write nv 20000002, offset 00000000, 00000004 bytes, return =
00000000
2
TBOOT: Error: write TPM error: 0x2.
TBOOT: no policy in TPM NV.
TBOOT: IA32_FEATURE_CONTROL_MSR: 0000ff07
TBOOT: CPU is SMX-capable
TBOOT: CPU is VMX-capable
TBOOT: SMX is enabled
TBOOT: TXT chipset and all needed capabilities present
TBOOT: TXT.ERRORCODE=c0000001
TBOOT: AC module error: acm_type=1, progress=00, error=0
TBOOT: LT.ESTS=0
TBOOT: IA32_FEATURE_CONTROL_MSR: 0000ff07
TBOOT: CPU is SMX-capable
TBOOT: CPU is VMX-capable
TBOOT: SMX is enabled
TBOOT: TXT chipset and all needed capabilities present
TBOOT: bios_data (@aaf20008, 2c):
TBOOT:  version: 3
TBOOT:  bios_sinit_size: 0x0 (0)
TBOOT:  lcp_pd_base: 0x0
TBOOT:  lcp_pd_size: 0x0 (0)
TBOOT:  num_logical_procs: 8
TBOOT:  flags: 0x00000000
TBOOT: measured launch succeeded
TBOOT: bios_data (@aaf20008, 2c):
TBOOT:  version: 3
TBOOT:  bios_sinit_size: 0x0 (0)
TBOOT:  lcp_pd_base: 0x0
TBOOT:  lcp_pd_size: 0x0 (0)
TBOOT:  num_logical_procs: 8
TBOOT:  flags: 0x00000000
```





```

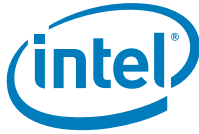
TBOOT: os_mle_data (@aaf20034, 10120):
TBOOT: version: 2
TBOOT: mbi: 0x000101b0
TBOOT: os_sinit_data (@aaf30154, 64):
TBOOT: version: 5
TBOOT: mle_ptab: 0x800000
TBOOT: mle_size: 0x1e000 (122880)
TBOOT: mle_hdr_base: 0x145c0
TBOOT: vtd_pmr_lo_base: 0x0
TBOOT: vtd_pmr_lo_size: 0xaa800000
TBOOT: vtd_pmr_hi_base: 0x100000000
TBOOT: vtd_pmr_hi_size: 0x4e000000
TBOOT: lcp_po_base: 0x0
TBOOT: lcp_po_size: 0x0 (0)
TBOOT: capabilities: 0x00000002
TBOOT:     rlp_wake_getsec: 0
TBOOT:     rlp_wake_monitor: 1
TBOOT:     ecx_pgtbl: 0
TBOOT: efi_rsdt_ptr: 0x0
TBOOT: sinit_mle_data (@aaf301b8, 22c):
TBOOT: version: 8
TBOOT: bios_acm_id:
      80 00 00 00 20 10 05 02 80 00 b0 01 ff ff ff ff ff ff ff ff
TBOOT: edx_sender_flags: 0x00000000
TBOOT: mseg_valid: 0x0
TBOOT: sinit_hash:
      d1 b1 1d 67 4e e0 9d 61 f0 67 36 08 5c 2c 1e bc ea a5 07 77
TBOOT: mle_hash:
      00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
TBOOT: stm_hash:
      00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
TBOOT: lcp_policy_hash:
      00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
TBOOT: lcp_policy_control: 0x00000002
TBOOT: rlp_wakeup_addr: 0xaaf018a0
TBOOT: num_mdrs: 7
TBOOT: mdrs_off: 0x9c
TBOOT: num_vtd_dmars: 232
TBOOT: vtd_dmars_off: 0x144
TBOOT: sinit_mdrs:
TBOOT: 0000000000000000 - 00000000000a0000 (GOOD)
TBOOT: 0000000000100000 - 0000000000f00000 (GOOD)
TBOOT: 0000000000100000 - 00000000aaf00000 (GOOD)
TBOOT: 0000000010000000 - 0000000014e00000 (GOOD)
TBOOT: 0000000400000000 - 0000000538000000 (GOOD)
TBOOT: 00000000ab000000 - 00000000ab800000 (SMRAM NON-OVERLAY)
TBOOT: 00000000000000cfc - 0000000000100cfc (PCIE EXTENDED CONFIG)
TBOOT: proc_scrtm_status: 0x00000000
TBOOT: RSDP (v002 INTEL) @ 0x000f0410
TBOOT: Seek in XSDT...
```



```
TBOOT: entry[0] sig = FACP @ 0xaab85d98
TBOOT: entry[1] sig = APIC @ 0xaabfcf18
TBOOT: acpi_table_ioapic @ aabfcfc4, .address = fec00000
TBOOT: RSDP (v002 INTEL) @ 0x000f0410
TBOOT: Seek in XSDT...
TBOOT: entry[0] sig = FACP @ 0xaab85d98
TBOOT: entry[1] sig = APIC @ 0xaabfcf18
TBOOT: entry[2] sig = TPCA @ 0xaaba4d18
TBOOT: entry[3] sig = MCFG @ 0xaaba4c98
TBOOT: acpi_table_mcfg @ aaba4c98, .base_address = f8000000
TBOOT: mtrr_def_type: e = 1, fe = 1, type = 0
TBOOT: mtrrs:
TBOOT: basemasktypev
TBOOT: 000000f800000061
TBOOT: 080000fe00000061
TBOOT: 0a0000ff80000061
TBOOT: 0a8000ffe0000061
TBOOT: 0aa000fff0000061
TBOOT: 0aac00fffc000001
TBOOT: 100000fc00000061
TBOOT: 140000ff00000061
TBOOT: 14e000ffe0000001
TBOOT: 0000000000000000
TBOOT: discarding RAM above reserved regions: 0xaabff000 - 0xaac00000
TBOOT: reserving 0xaa800000 - 0xaa90d000, which was truncated for VT-d
TBOOT: min_lo_ram: 0x0, max_lo_ram: 0xaa90d000
TBOOT: min_hi_ram: 0x100000000, max_hi_ram: 0x14e000000
TBOOT: MSR for SMM monitor control on BSP is 0x0.
TBOOT: verifying ILP is opt-out or has the same MSEG header with
TXT.MSEG.BASE
      opt-out
TBOOT: : succeeded.
TBOOT: enabling SMIs on BSP
TBOOT: mle_join.entry_point = 8031f0
TBOOT: mle_join.seg_sel = 8
TBOOT: mle_join.gdt_base = 804000
TBOOT: mle_join.gdt_limit = 3f
TBOOT: joining RLPs to MLE with MONITOR wakeup
TBOOT: rlp_wakeup_addr = 0xaaf018a0
TBOOT: cpu 7 waking up from TXT sleep
TBOOT: waiting for all APs (7) to enter wait-for-sipi...
TBOOT: MSR for SMM monitor control on cpu 7 is 0x0
TBOOT: verifying ILP's MSR_IA32_SMM_MONITOR_CTL with cpu 7
      : succeeded.
TBOOT: enabling SMIs on cpu 7
TBOOT: .VMXON done for cpu 7
TBOOT:
TBOOT: launching mini-guest for cpu 7
TBOOT: cpu 6 waking up from TXT sleep
TBOOT: MSR for SMM monitor control on cpu 6 is 0x0
```



```
TBOOT: verifying ILP's MSR_IA32_SMM_MONITOR_CTL with cpu 6
      : succeeded.
TBOOT: enabling SMIs on cpu 6
TBOOT: VMXON done for cpu 6
TBOOT: launching mini-guest for cpu 6
TBOOT: cpu 3 waking up from TXT sleep
TBOOT: MSR for SMM monitor control on cpu 3 is 0x0
TBOOT: verifying ILP's MSR_IA32_SMM_MONITOR_CTL with cpu 3
      : succeeded.
TBOOT: enabling SMIs on cpu 3
TBOOT: VMXON done for cpu 3
TBOOT: launching mini-guest for cpu 3
TBOOT: cpu 5 waking up from TXT sleep
TBOOT: MSR for SMM monitor control on cpu 5 is 0x0
TBOOT: verifying ILP's MSR_IA32_SMM_MONITOR_CTL with cpu 5
      : succeeded.
TBOOT: enabling SMIs on cpu 5
TBOOT: VMXON done for cpu 5
TBOOT: .cpu 2 waking up from TXT sleep
TBOOT: launching mini-guest for cpu 5
TBOOT: MSR for SMM monitor control on cpu 2 is 0x0
TBOOT: verifying ILP's MSR_IA32_SMM_MONITOR_CTL with cpu 2
      : succeeded.
TBOOT: enabling SMIs on cpu 2
TBOOT: VMXON done for cpu 2
TBOOT: launching mini-guest for cpu 2
TBOOT: cpu 4 waking up from TXT sleep
TBOOT: MSR for SMM monitor control on cpu 4 is 0x0
TBOOT: verifying ILP's MSR_IA32_SMM_MONITOR_CTL with cpu 4
      : succeeded.
TBOOT: enabling SMIs on cpu 4
TBOOT: VMXON done for cpu 4
TBOOT: launching mini-guest for cpu 4
TBOOT: cpu 1 waking up from TXT sleep
TBOOT: MSR for SMM monitor control on cpu 1 is 0x0
TBOOT: .verifying ILP's MSR_IA32_SMM_MONITOR_CTL with cpu 1
      . : succeeded.
TBOOT: .enabling SMIs on cpu 1
TBOOT: .VMXON done for cpu 1
TBOOT: .launching mini-guest for cpu 1
TBOOT: .
TBOOT: all APs in wait-for-sipi
TBOOT: saved IA32_MISC_ENABLE = 0x00850089
TBOOT: set LT.CMD.SECRETS flag
TBOOT: opened TPM locality 1
TBOOT: RSDP (v002 INTEL) @ 0x000f0410
TBOOT: Seek in XSDT...
TBOOT: entry[0] sig = FACP @ 0xaab85d98
TBOOT: entry[1] sig = APIC @ 0xaabfcf18
TBOOT: entry[2] sig = TCPA @ 0xaaba4d18
```



```
TBOOT: entry[3] sig = MCFG @ 0xaaba4c98
TBOOT: entry[4] sig = HPET @ 0xaaba4c18
TBOOT: entry[5] sig = SSDT @ 0xaab86018
TBOOT: entry[6] sig = SSDT @ 0xaab87c18
TBOOT: entry[7] sig = BOOT @ 0xaaba4b98
TBOOT: entry[8] sig = SSDT @ 0xaab84018
TBOOT: entry[9] sig = SSDT @ 0xaab83018
TBOOT: entry[10] sig = DMAR @ 0xaab85c18
TBOOT: DMAR table @ 0xaab85c18 saved.
TBOOT: no LCP module found
TBOOT: verifying module 0 of mbi (87e000 - bd28bf) in e820 table
      (range from 000000000087e000 to 0000000000bd28c0 is in E820_RAM)
TBOOT: : succeeded.
TBOOT: verifying module 1 of mbi (bd3000 - 2545bff) in e820 table
      (range from 0000000000bd3000 to 00000000002545c00 is in E820_RAM)
TBOOT: : succeeded.
TBOOT: protecting TXT heap (aaf20000 - aaffffff) in e820 table
TBOOT: protecting SINIT (aaf00000 - aaf1ffff) in e820 table
TBOOT: protecting TXT Private Space (fed20000 - fed2ffff) in e820 table
TBOOT: verifying e820 table against SINIT MDRs: verification succeeded.
TBOOT: verifying tboot and its page table (800000 - 87ccb3) in e820 table
      (range from 0000000000800000 to 000000000087ccb4 is in E820_RAM)
TBOOT: : succeeded.
TBOOT: Error: ELF magic number is not matched.
TBOOT: protecting tboot (800000 - 87cfff) in e820 table
TBOOT: reserving tboot memory log (60000 - 67fff) in e820 table
TBOOT: adjusted e820 map:
TBOOT: 0000000000000000 - 0000000000060000 (1)
TBOOT: 0000000000060000 - 0000000000068000 (2)
TBOOT: 0000000000068000 - 000000000009bc00 (1)
TBOOT: 000000000009bc00 - 00000000000a0000 (2)
TBOOT: 00000000000a0000 - 0000000000100000 (2)
TBOOT: 0000000000100000 - 0000000000800000 (1)
TBOOT: 0000000000800000 - 000000000087d000 (2)
TBOOT: 000000000087d000 - 0000000000f00000 (1)
TBOOT: 0000000000f00000 - 0000000001000000 (2)
TBOOT: 0000000001000000 - 00000000aa800000 (1)
TBOOT: 00000000aa800000 - 00000000aa90d000 (2)
TBOOT: 00000000aa90d000 - 00000000aa9e7000 (2)
TBOOT: 00000000aa9e7000 - 00000000aabe7000 (4)
TBOOT: 00000000aabe7000 - 00000000aabff000 (3)
TBOOT: 00000000aabff000 - 00000000aac00000 (2)
TBOOT: 00000000aac00000 - 00000000aaf00000 (2)
TBOOT: 00000000aaf00000 - 00000000aaf20000 (2)
TBOOT: 00000000aaf20000 - 00000000ab000000 (2)
TBOOT: 00000000ab000000 - 00000000b0000000 (2)
TBOOT: 00000000b0000000 - 00000000fc000000 (2)
TBOOT: 00000000fc000000 - 00000000fec01000 (2)
TBOOT: 00000000fec01000 - 00000000fed14000 (2)
TBOOT: 00000000fed14000 - 00000000fed1a000 (2)
```



```
TBOOT: 00000000fed1c000 - 00000000fed20000 (2)
TBOOT: 00000000fed20000 - 00000000fed30000 (2)
TBOOT: 00000000fee00000 - 00000000fee01000 (2)
TBOOT: 00000000ff980000 - 00000000ffc00000 (2)
TBOOT: 00000000ffd80000 - 0000000100000000 (2)
TBOOT: 0000000100000000 - 000000014e000000 (1)
TBOOT: verifying module "vmlinuz0 root=LABEL=LIVE rootfstype=auto ro
liveimg ver
bose console=tty0 console=ttyS0,115200 iommu=on vga=no OK : af 47 51 f8
48 2c
53 f8 cb 80 ea 58 94 07 62 19 60 6f 15 3b
TBOOT: verifying module "initrd0.img "...
TBOOT: OK : d1 4a 4b 3a 52 bd fb 3a 8c a5 96 51 2e 42 26 fb 09 94 ba 00
TBOOT: all modules are verified
TBOOT: pre_k_s3_state:
TBOOT: vtd_pmr_lo_base: 0x0
TBOOT: vtd_pmr_lo_size: 0xaa800000
TBOOT: vtd_pmr_hi_base: 0x100000000
TBOOT: vtd_pmr_hi_size: 0x4e000000
TBOOT: pol_hash: ab 41 62 4e 7d 71 f0 68 d4 8e 1c 2f 43 e6 16 bf 40 67 1c
39
TBOOT: VL measurements:
TBOOT: PCR 17: 97 04 35 36 30 67 4b fe 21 b8 6b 64 a7 b0 f9 9c 29 7c f9
02
TBOOT: PCR 18: af 47 51 f8 48 2c 53 f8 cb 80 ea 58 94 07 62 19 60 6f 15
3b
TBOOT: PCR 19: d1 4a 4b 3a 52 bd fb 3a 8c a5 96 51 2e 42 26 fb 09 94 ba
00
TBOOT: TPM: start OSAP, return value = 00000012
TBOOT: failed to seal data
TBOOT: PCRs before extending:
TBOOT: PCR 17: 1e 87 57 4e 91 2d f6 82 bc 88 57 db d2 58 eb 21 33 3e 96
e2
TBOOT: PCR 18: b8 0d e5 d1 38 75 85 41 c5 f0 52 65 ad 14 4a b9 fa 86 d1
db
TBOOT: PCRs after extending:
TBOOT: PCR 17: 08 76 e7 39 23 4f b4 90 28 e5 36 af 27 4f e7 8a b1 1f 2a
11
TBOOT: PCR 18: 98 6f 5b 8e bb 75 e6 e6 dc 33 b0 e6 6e 68 a8 3b 6b 9d b0
2e
TBOOT: creation or verification of S3 measurements failed.
TBOOT: tboot_shared data:
TBOOT: version: 5
TBOOT: log_addr: 0x00060000
TBOOT: shutdown_entry: 0x008031b0
TBOOT: shutdown_type: 0
TBOOT: tboot_base: 0x00803000
TBOOT: tboot_size: 0x79cb4
TBOOT: num_in_wfs: 7
TBOOT: no LCP module found
TBOOT: Error: ELF magic number is not matched.
TBOOT: assuming kernel is Linux format
```



```
TBOOT: Initrd from 0x7e68d000 to 0x7ffffc00
TBOOT: Kernel (protected mode) from 0xc00000 to 0xf512c0
TBOOT: Kernel (real mode) from 0x90000 to 0x93600
TBOOT: transferring control to kernel @0x00c00000...
Initializing cgroup subsys cpuset
Initializing cgroup subsys cpu
```

**§ §**



# B Appendix B—Intel® CSME Firmware Corporate Power Management in WoWLAN Coexistence Mode

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This chapter provides detailed tests for Intel® CSME Firmware Power Management in WoWLAN Coexistence Mode.

For details on WoWLAN Coexistence and WoWLAN Coexistence Mode, including feature availability, review the *Intel® AMT and Wake On Wireless LAN Coexistence* feature overview found in Document Number: 546827.

**Warning:** In order to fully implement Wake on Wireless LAN (WoWLAN) in Sx states, the host BIOS must set HOST\_WLAN\_PP\_EN. For more further details, refer to the PCH *External Design Specification (EDS)* and the PCH *Platform Design Guide (PDG)*. Failure to properly set the HOST\_WLAN\_PP\_EN bit may result in failures for the tests described herein.

Test Environment setup for this section:

- System Under Test (SUT) can be configured in either manual configuration mode or using enterprise provisioning mode.
- IP address can be selected as static/DHCP (IPv4 or IPv6)
- Select manageability mode as **Intel® AMT**
- Intel® Platform Enablement Test Suite should be installed on the management console.
- Install all platform drivers (Chipset, Graphics, LAN, WLAN, Intel® MEI, LMS\_SOL)
- Client platform OS can be Windows\* 10
- For wired LAN network use a hub/switch and network cables.
- Wireless setup:
  - Wireless card should be installed.
  - Setup an active wireless profile.
- LAN and WLAN interfaces IPs should be setup on different subnets.

## Tools for Testing:

Intel® Platform Enablement Test Suite—Latest version of the tool from the Intel® CSME Compliancy kit release. Refer to the Intel® Platform Enablement Test Suite user guide available in the Intel Compliancy kit for exact instructions on how to load and setup the Intel® Platform Enablement Test Suite software.

**Note:** The following tests can be run by means of Intel® Platform Enablement Test Suite or Manually by following the test procedure step by step.



## B.1 Deep SX

**Note:** CNVI does not support wake on WLAN/BT during deep system sleep states (DSx).

## B.2 Intel® CSME Power Management Test Coverage Summary

Test ID	Test Case Title	PETS/Manual	Network Factor
ME_PM_1	S0/M0 to S3/M-Off (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_2	S3/M-Off to S0/M0 (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_3	S0/M0 to S3/M3 (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_4	S3/M3 to S0/M0 (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_5	S3/M3 to S3/M-Off (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_6	S3/M3 to S3/M-Off (with Intel® CSME Wake) (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_7	S3/M-Off to S3/M3 (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_17	Host Power-Cycle Reset also known as cold reset (mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_19	Straight-to-S5, CSME Power Policy is S0-Only (Power Button Override) (BIOS: S5 after exit G3. Host WOL: Off) (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_20	Straight-to-S5, CSME Power Policy Calls for Sx Operation (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN; WLAN only
ME_PM_21	S0/M0 to S3/M-Off (without Intel® CSME Wake) to S3/M-Off (with Intel® CSME Wake) (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN
ME_PM_22	S3/M-Off (with Intel® CSME Wake) to S3/M-Off (without Intel® CSME Wake) (Mandatory)	PETS - Package Names: Compliance_Power_G3-S5_WoWLAN.xml	LAN+WLAN

**Note:** All the tests which use wake on LAN (WOL) as a trigger require SUSPEND well (SUS well) to be powered-up. Hence platforms which implement and support DeepSx cannot run WOL tests.





## B.1 AME\_PM\_1 - S0/M0 to S3/M-Off

<b>Test ID</b>	<b>ME_PM_1.1a</b>
<b>Test Case Title</b>	S0/M0 to S3/M-Off in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S0/M0; Target power state - S3/M-Off; LAN Power Policy - Power Policy #1, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - DC; Trigger: Host go S3
<b>Objective</b>	This test checks for the system power flow S0/M0 to S3/M-Off
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #1: ON in S0</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to DC.</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Put host into standby.</li> <li>9. Verify test pass/fail criteria</li> <li>10. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host goes to S3 state. Intel® CSME becomes M-Off. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.

<b>Test ID</b>	<b>ME_PM_1.2a</b>
<b>Test Case Title</b>	S0/M0 to S3/M-Off in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S0/M0; Target power state - S3/M-Off; LAN Power Policy - Power Policy #1, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: Host goes to S3
<b>Objective</b>	This test checks for the system power flow S0/M0 to S3/M-Off
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #1: ON in S0</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC.</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Put host into standby.</li> <li>9. Verify test pass/fail criteria.</li> <li>10. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host goes to S3 state. Intel® CSME become M-Off. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.



<b>Test ID</b>	<b>ME_PM_1.3a</b>
<b>Test Case Title</b>	S0/M0 to S3/M-Off in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S0/M0; Target power state - S3/M-Off; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - DC; Trigger: Host goes to S3
<b>Objective</b>	This test checks for the system power flow S0/M0 to S3/M-Off
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set the wireless management link policy to '#3: Enabled in S0, Sx/AC'</li> <li>5. Set the power source to DC.</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Put host into standby</li> <li>9. Verify test pass/fail criteria.</li> <li>10. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host goes to S3 state. Intel® CSME become M-Off. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.

## B.2 ME\_PM\_2 - S3/M-Off to S0/M0

<b>Test ID</b>	<b>ME_PM_2.2a</b>
<b>Test Case Title</b>	S3/M-Off to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S0/M0; LAN Power Policy - Power Policy #1, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - DC; Trigger: PWR button
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #1: ON in S0</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to DC.</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Check Windows last boot time</li> <li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li> <li>10. Put host into standby</li> <li>11. Verify that Intel® CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li> <li>12. Put the system back to S0 by pressing the power button shortly (make sure OS is up)</li> <li>13. Ping Intel® AMT IP address with both wired and WLAN interface and Verify Test Pass/Fail Criteria</li> <li>14. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value 0x60002306</li> <li>15. Ensure that yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Test Pass/Fail Criteria</b>	Intel® AMT answers ping by means of the LAN/WLAN interface. Host goes to S0 state. Intel® CSME becomes M0. Verify Windows last boot time has not changed.



<b>Test ID</b>	<b>ME_PM_2.3a</b>
<b>Test Case Title</b>	S3/M-Off to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S0/M0; LAN Power Policy - Power Policy #1, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: PWR button
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #1: ON in S0</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC.</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Check Windows last boot time</li> <li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li> <li>10. Put host into standby</li> <li>11. Verify that Intel® CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li> <li>12. Put the system back to S0 by pressing the power button. Make sure OS is up</li> <li>13. Ping Intel® AMT IP address with both wired and WLAN interface</li> <li>14. Verify Test Pass/Fail Criteria</li> <li>15. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x60002306</b></li> <li>16. Ensure that yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host goes to S0 state. Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.

<b>Test ID</b>	<b>ME_PM_2.4a</b>
<b>Test Case Title</b>	S3/M-Off to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S0/M0; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: host wake on magic packet
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S0/M0



Test ID	ME_PM_2.4a
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. Enable host WOL</li><li>3. If the SUT has WLAN support and the magic packet is to be sent by means of the LAN interface, enable the host WoWLAN driver setting.</li><li>4. Enable Host LAN device to wake from off states by Magic Packet only.</li><li>5. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4–S5/AC</li><li>6. Set Wireless Link Policy `#3: Enabled in S0, Sx/AC`. This is required only when wireless is used.</li><li>7. Set the power source to AC+DC</li><li>8. Configure idle timeout value in Intel® MEBX to 1</li><li>9. Boot the system to S0/M0 that is, make sure OS is up</li><li>10. Check Windows last boot time</li><li>11. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>12. Ensure that yellow bang is not seen on Drivers in Device Manager</li><li>13. Put host into standby</li><li>14. Wait for idle timeout expiry for Intel® CSME to enter M-Off (To make sure Intel® CSME enters M-Off, check SLP_A# status)</li><li>15. Wake the host by sending magic packets by means of the LAN/WLAN device. Make sure OS is up</li><li>16. Ping Intel® AMT IP address with both wired and WLAN interface.</li><li>17. Verify Test Pass/Fail Criteria</li><li>18. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x60</b>002306</li><li>19. Ensure that yellow bang is not seen on Drivers in Device Manager</li></ol>
Test Pass/Fail Criteria	Host wakes to S0 state, Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.

Test ID	ME_PM_2.5a
Test Case Title	S3/M-Off to S0/M0 in WoWLAN Coexistence Mode
Mandatory/Optional	Mandatory
Description	Original Power State: S3/M-Off; Target power state - S0/M0; LAN Power Policy - Power Policy #2, WLAN Link Policy - `#3: Enabled in S0, Sx/AC`; power source - DC; Trigger: PWR button
Objective	This test checks for the system power flow S3/M-Off to S0/M0
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3.</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4–S5/AC</li><li>4. Set Wireless Link Policy `#3: Enabled in S0, Sx/AC`. This is required only when wireless is used.</li><li>5. Set the power source to DC.</li><li>6. Boot the system to S0/M0 that is, make sure OS is up</li><li>7. Check Windows last boot time</li><li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li><li>10. Put host into standby</li><li>11. Verify that Intel® CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li><li>12. Put the system back to S0 by pressing the power button. Make sure OS is up</li><li>13. Ping Intel® AMT IP address with both wired and WLAN interface</li><li>14. Verify Test Pass/Fail Criteria</li><li>15. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x60</b>002306</li><li>16. Ensure that yellow bang is not seen on Drivers in Device Manager</li></ol>



<b>Test ID</b>	<b>ME_PM_2.5a</b>
<b>Test Pass/Fail Criteria</b>	Host wakes to S0 state, Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.

<b>Test ID</b>	<b>ME_PM_2.6a</b>
<b>Test Case Title</b>	S3/M-Off to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S0/M0; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: PWR button
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3.</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC.</li> <li>6. Configure idle timeout value in Intel® MEBX to 1</li> <li>7. Boot the system to S0/M0 that is, make sure OS is up</li> <li>8. Check Windows last boot time</li> <li>9. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>10. Ensure that yellow bang is not seen on Drivers in Device Manager</li> <li>11. Put host into standby</li> <li>12. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>13. Wait for idle timeout expiry for Intel® CSME to enter M-Off (To make sure Intel® CSME enters M-Off, check SLP_A# status)</li> <li>14. Put the system back to S0 by pressing the power button shortly. Make sure OS is up</li> <li>15. Ping Intel® AMT IP address with both wired and WLAN interface</li> <li>16. Verify Test Pass/Fail Criteria</li> <li>17. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x60</b>002306</li> <li>18. Ensure that yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host wakes to S0 state, Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.



## B.3 ME\_PM\_3 - S0/M0 to S3/M3 to S0/M0

<b>Test ID</b>	<b>ME_PM_3.1a</b>
<b>Test Case Title</b>	S0/M0 to S3/M3 to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S0/M0; Target power state - S3/M3; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: WS-MAN frame sent to the WLAN interface
<b>Objective</b>	This test checks for the system power flow S0/M0 to S3/M3 to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li><li>5. Set the power source to AC+DC</li><li>6. Boot the system to S0/M0 that is, make sure OS is up</li><li>7. Check Windows last boot time.</li><li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface).</li><li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li><li>10. Put host into standby.</li><li>11. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>12. Ping Intel® AMT IP address by means of WS-MAN protocol by means of the LAN and WLAN interfaces.</li><li>13. Verify Test Pass/Fail Criteria</li><li>14. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x68</b>002306</li><li>15. Ensure that yellow bang is not seen on Drivers in Device Manager</li></ol>
<b>Test Pass/Fail Criteria</b>	Host wakes to S0 state, Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.

<b>Test ID</b>	<b>ME_PM_3.21a</b>
<b>Test Case Title</b>	S0/M0 to S3/M3 to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S0/M0; Target power state - S3/M3; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#2: Enabled in S0 only'; power source - ACDC; Trigger: WS-MAN frame sent to the WLAN interface



<b>Test ID</b>	<b>ME_PM_3.21a</b>
<b>Objective</b>	This test checks for the system power flow S0/M0 to S3/M3 to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#2: Enabled in S0 only'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC.</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up.</li> <li>7. Check Windows last boot time.</li> <li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface).</li> <li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li> <li>10. Put host into standby</li> <li>11. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>12. Ping Intel® AMT IP address by means of WS-MAN protocol by means of the LAN and WLAN interfaces.</li> <li>13. Verify Test Pass/Fail Criteria</li> <li>14. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x68</b>002306</li> <li>15. Ensure that yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host wakes to S0 state, Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.

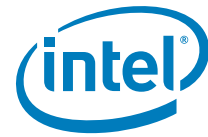


## B.4 ME\_PM\_4 - S3/M3 to S0/M0

<b>Test ID</b>	<b>ME_PM_4.1a</b>
<b>Test Case Title</b>	S3/M3 to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M3; Target power state - S0/M0; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: Host wake on magic packet
<b>Objective</b>	This test checks for the system power flow S3/M3 to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. Enable host WOL</li><li>3. If the SUT has WLAN support and the magic packet is to be sent by means of the LAN interface, enable the host WoWLAN driver setting.</li><li>4. Enable Host LAN/WLAN device to wake from off states by Magic Packet only.</li><li>5. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>6. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li><li>7. Set the power source to AC+DC</li><li>8. Boot the system to S0/M0 that is, make sure OS is up</li><li>9. Check Windows last boot time</li><li>10. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>11. Ensure that yellow bang is not seen on Drivers in Device Manager</li><li>12. Put host into standby</li><li>13. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>14. Wake up the host by sending magic packets by means of the LAN/WLAN device.</li><li>15. Ping Intel® AMT IP address by means of the LAN and WLAN interface and Verify Test Pass/Fail Criteria</li><li>16. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x68</b>002306</li><li>17. Ensure that yellow bang is not seen on Drivers in Device Manager</li></ol>
<b>Test Pass/Fail Criteria</b>	Host goes to S0 state. Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.

<b>Test ID</b>	<b>ME_PM_4.2a</b>
<b>Test Case Title</b>	S3/M3 to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M3; Target power state - S0/M0; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: Power button
<b>Objective</b>	This test checks for the system power flow S3/M3 to S0/M0





<b>Test ID</b>	<b>ME_PM_4.2a</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC + DC</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Check Windows last boot time</li> <li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li> <li>10. Put host into standby</li> <li>11. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>12. Wake the host by pressing power button</li> <li>13. Ping Intel® AMT IP address by means of the LAN/WLAN interface and Verify Test Pass/Fail Criteria</li> <li>14. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x68</b>002306</li> <li>15. Ensure that yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host returns to S0. Intel® CSME becomes M0. Intel® AMT is reachable by means of the LAN and WLAN interface. Verify Windows last boot time has not changed.

<b>Test ID</b>	<b>ME_PM_4.21a</b>
<b>Test Case Title</b>	S3/M3 to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M3; Target power state - S0/M0; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#2: Enabled in S0 only'; power source - ACDC; Trigger: Host wake on magic packet
<b>Objective</b>	This test checks for the system power flow S3/M3 to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. Enable host WOL</li> <li>3. If the SUT has WLAN support and the magic packet is to be sent by means of the LAN interface, enable the host WoWLAN driver setting.</li> <li>4. Enable Host LAN/WLAN device to wake from off states by Magic Packet only.</li> <li>5. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>6. Set Wireless Link Policy '#2: Enabled in S0 only'. This is required only when wireless is used.</li> <li>7. Set the power source to AC+DC</li> <li>8. Boot the system to S0/M0 that is, make sure OS is up</li> <li>9. Check Windows last boot time</li> <li>10. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>11. Ensure that yellow bang is not seen on Drivers in Device Manager</li> <li>12. Put host into standby</li> <li>13. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>14. Wake up the host by sending magic packets by means of the LAN/WLAN device.</li> <li>15. Ping Intel® AMT IP address by means of the LAN and WLAN interface and Verify Test Pass/Fail Criteria</li> <li>16. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x68</b>002306</li> <li>17. Ensure that yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host goes to S0 state. Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN and WLAN interface. Verify Windows last boot time has not changed.



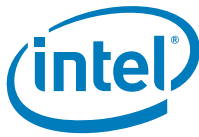
Test ID	ME_PM_4.22a
Test Case Title	S3/M3 to S0/M0 in WoWLAN Coexistence Mode
Mandatory/Optional	Mandatory
Description	Original Power State: S3/M3; Target power state - S0/M0; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#2: Enabled in S0 only'; power source - ACDC; Trigger: Power button
Objective	This test checks for the system power flow S3/M3 to S0/M0
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>4. Set Wireless Link Policy '#2: Enabled in S0 only'. This is required only when wireless is used.</li><li>5. Set the power source to AC + DC</li><li>6. Boot the system to S0/M0 that is, make sure OS is up</li><li>7. Check Windows last boot time</li><li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li><li>10. Put host into standby</li><li>11. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>12. Wake the host by pressing power button</li><li>13. Ping Intel® AMT IP address by means of the LAN/WLAN interface only and Verify Test Pass/Fail Criteria</li><li>14. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x68</b>002306</li><li>15. Ensure that yellow bang is not seen on Drivers in Device Manager</li></ol>
Test Pass/Fail Criteria	Host returns to S0. Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface only. Verify Windows last boot time has not changed.



## B.5 ME\_PM\_5 - S3/M3 to S3/M-Off (Without Intel® CSME Wake)

<b>Test ID</b>	<b>ME_PM_5.1a</b>
<b>Test Case Title</b>	S3/M3 to S3/M-Off (without Intel® CSME Wake) in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M3; Target power state - S3/M-Off; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: ACDC->DC
<b>Objective</b>	This test checks for the system power flow S3/M3 to S3/M-Off (without Intel® CSME Wake)
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Put host into standby</li> <li>9. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>10. Disconnect AC power cord</li> <li>11. Verify Test Pass/Fail Criteria</li> <li>12. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host stays in S3 state. Intel® CSME stays off. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.

<b>Test ID</b>	<b>ME_PM_5.21a</b>
<b>Test Case Title</b>	S3/M3 to S3/M-Off (without Intel® CSME Wake) in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M3; Target power state - S3/M-Off; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#2: Enabled in S0 only'; power source - ACDC; Trigger: ACDC->DC
<b>Objective</b>	This test checks for the system power flow S3/M3 to S3/M-Off (without Intel® CSME Wake)
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#2: Enabled in S0 only'. This is required only when wireless is used.</li> <li>5. Set the power source to AC + DC</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Put host into standby</li> <li>9. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>10. Disconnect AC power cord</li> <li>11. Verify Test Pass/Fail Criteria</li> <li>12. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host stays in S3 state. Intel® CSME becomes M-Off. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.



## B.6 ME\_PM\_6 - S3/M3 to S3/M-Off (With Intel® CSME Wake)

<b>Test ID</b>	<b>ME_PM_6.1a</b>
<b>Test Case Title</b>	S3/M3 to S3/M-Off (with Intel® CSME Wake) in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M3; Target power state - S3/M-Off; LAN Power Policy - Power Policy #2, WLAN Link Policy `#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: Wait idle time.
<b>Objective</b>	This test checks for the system power flow S3/M3 to S3/M-Off (with Intel® CSME Wake)
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>4. Set Wireless Link Policy `#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li><li>5. Set the power source to AC + DC</li><li>6. Configure idle timeout value in Intel® MEBX to 1</li><li>7. Boot the system to S0/M0 that is, make sure OS is up</li><li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>9. Put host into standby</li><li>10. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>11. Wait for idle timeout expiry for CSME to enter M-Off (To make sure Intel® CSME enters M-Off by checking that SLP_A# should be asserted)</li><li>12. Verify Test Pass/Fail Criteria</li><li>13. FWSTS: N/A</li></ol>
<b>Test Pass/Fail Criteria</b>	Host stays in S3 state. Verify that Intel® CSME became M-Off by checking that SLP_A# signal is asserted,

<b>Test ID</b>	<b>ME_PM_6.21a</b>
<b>Test Case Title</b>	S3/M3 to S3/M-Off (with Intel® CSME Wake) in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M3; Target power state - S3/M-Off; LAN Power Policy - Power Policy #2, WLAN Link Policy `#2: Enabled in S0 only'; power source - ACDC; Trigger: Wait idle time.
<b>Objective</b>	This test checks for the system power flow S3/M3 to S3/M-Off (with Intel® CSME Wake)



<b>Test ID</b>	<b>ME_PM_6.21a</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#2: Enabled in S0 only'. This is required only when wireless is used.</li> <li>5. Set the power source to AC + DC</li> <li>6. Configure idle timeout value in Intel® MEBX to 1</li> <li>7. Boot the system to S0/M0 that is, make sure OS is up</li> <li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>9. Put host into standby</li> <li>10. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>11. Wait for idle timeout expiry for CSME to enter M-Off (To make sure Intel® CSME enters M-Off check SLP_A# status)</li> <li>12. Verify Test Pass/Fail Criteria</li> <li>13. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Host stays in S3 state. Verify that Intel® CSME became M-Off by checking that SLP_A# signal is asserted,

## B.7 ME\_PM\_7 - S3/M-Off to S3/M3 (to S0/M0)

<b>Test ID</b>	<b>ME_PM_7.1a</b>
<b>Test Case Title</b>	S3/M-Off to S3/M3 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Wireless Only</b>	No
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S3/M3; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: Wake CSME by means of the LAN ping.
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S3/M3
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC + DC</li> <li>6. Configure idle timeout value in Intel® MEBX to 1</li> <li>7. Boot the system to S0/M0 that is, make sure OS is up</li> <li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>9. Put the system into standby</li> <li>10. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>11. Wait for idle timeout expiry for Intel® CSME to enter M-Off (To make sure Intel® CSME enters M-Off check SLP_A# status)</li> <li>12. Wake up Intel® CSME by means of the Intel® CSME version query over the LAN interface.</li> <li>13. Verify Test Pass/Fail Criteria</li> <li>14. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Intel® AMT answers ping by means of the LAN interface. Host stays in S3 state. Intel® CSME becomes M3.



<b>Test ID</b>	<b>ME_PM_7.2a</b>
<b>Test Case Title</b>	S3/M-Off to S3/M3 to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S3/M3; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - DC; Trigger: WS-MAN frame sent to the WLAN interface
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S3/M3 to S0/M0
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li><li>5. Set the power source to DC</li><li>6. Boot the system to S0/M0 that is, make sure OS is up</li><li>7. Check Windows last boot time.</li><li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>9. Ensure that yellow bang is not seen on Drivers in Device Manager</li><li>10. Put host into standby</li><li>11. Verify that CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li><li>12. Reconnect AC power cord. (ME wakes to CM3 but goes back to CM3-PG soon)</li><li>13. Ping Intel® AMT IP address by means of WS-MAN protocol by means of the LAN and WLAN interfaces.</li><li>14. Verify Test Pass/Fail Criteria</li><li>15. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x68</b>002306</li><li>16. Ensure that yellow bang is not seen on Drivers in Device Manager</li></ol>
<b>Test Pass/Fail Criteria</b>	Host wakes to S0 state, Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.

<b>Test ID</b>	<b>ME_PM_7.3a</b>
<b>Test Case Title</b>	S3/M-Off to S3/M3 to S0/M0 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S3/M3; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#3: Enabled in S0, Sx/AC'; power source - ACDC; Trigger: WS-MAN frame sent to the WLAN interface
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S3/M3 to S0/M0



<b>Test ID</b>	<b>ME_PM_7.3a</b>
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC + DC</li> <li>6. Configure idle timeout value in Intel® MEBX to 1</li> <li>7. Boot the system to S0/M0 that is, make sure OS is up</li> <li>8. Check Windows last boot time.</li> <li>9. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>10. Ensure that yellow bang is not seen on Drivers in Device Manager</li> <li>11. Put the system into standby</li> <li>12. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>13. Wait for idle timeout expiry for Intel® CSME to enter M-Off (To make sure Intel® CSME enters M-Off check SLP_A# status)</li> <li>14. Wake up Intel® CSME and the system by means of the Intel® CSME version query over the WLAN interface.</li> <li>15. Verify Test Pass/Fail Criteria</li> <li>16. Confirm that the system is in S0/M0 state and the second bit of the FWSTS 2 register should have a value <b>0x60</b>002306</li> <li>17. Ensure that yellow bang is not seen on Drivers in Device Manager</li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>Host wakes to S0 state, Intel® CSME becomes M0. Intel® AMT answers ping by means of the LAN/WLAN interface. Verify Windows last boot time has not changed.</p> <p><b>Note:</b> It could take about ~30-40 seconds for the firmware to start responding to pings by means of the WLAN interface.</p>

<b>Test ID</b>	<b>ME_PM_7.21a</b>
<b>Test Case Title</b>	S3/M-Off to S3/M3 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Wireless Only</b>	No
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S3/M3; LAN Power Policy - Power Policy #2, WLAN Link Policy - '#2: Enabled in S0 only'; power source - ACDC; Trigger: Wake CSME by means of the LAN ping.
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S3/M3
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy '#2: Enabled in S0 only'.</li> <li>5. This is required only when wireless is used.</li> <li>6. Set the power source to AC+DC.</li> <li>7. Configure idle timeout value in Intel® MEBX to 1.</li> <li>8. Boot the system to S0/M0 that is, make sure OS is up.</li> <li>9. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>10. Put the system into standby</li> <li>11. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>12. Wait for idle timeout expiry for Intel® CSME to enter M-Off (To make sure Intel® CSME enters M-Off check SLP_A# status)</li> <li>13. Wake up Intel® CSME by means of the Intel® CSME version query over the LAN interface.</li> <li>14. Verify Test Pass/Fail Criteria</li> <li>15. FWSTS: N/A</li> </ol>



<b>Test ID</b>	<b>ME_PM_7.21a</b>
<b>Test Pass/Fail Criteria</b>	Intel® AMT answers ping by means of the LAN interface. Host stays in S3 state. Intel® CSME becomes M3.

<b>Test ID</b>	<b>ME_PM_7.22a</b>
<b>Test Case Title</b>	S3/M-Off to S3/M3 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Wireless Only</b>	No
<b>Description</b>	Original Power State: S3/M-Off; Target power state - S3/M3; LAN Power Policy - Power Policy #2, WLAN Link Policy - #2: Enabled in S0 only; power source - DC; Trigger: DC->ACDC.
<b>Objective</b>	This test checks for the system power flow S3/M-Off to S3/M3
<b>Procedure</b>	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>4. Set Wireless Link Policy `#2: Enabled in S0 only'. This is required only when wireless is used.</li><li>5. Set the power source to DC</li><li>6. Boot the system to S0/M0 that is, make sure OS is up</li><li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>8. Put host into standby</li><li>9. Verify that CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li><li>10. Reconnect AC power cord</li><li>11. Ping Intel® AMT IP address by means of the LAN interface only</li><li>12. Verify Test Pass/Fail Criteria</li><li>13. FWSTS: N/A</li></ol>
<b>Test Pass/Fail Criteria</b>	Intel® AMT is reachable by means of the LAN interface only. Host stays in S3 state. Intel® CSME becomes M3.





## B.8 Straight-to-S5, Intel® CSME Power Policy is S0 Only

Test ID	ME_PM_19.3a
Test Case Title	S3/M-Off to S5/M-Off in WoWLAN Coexistence Mode
Mandatory/Optional	Mandatory
Description	<p>This test checks for S3/M-Off to S5/M-Off flow; LAN Power Policy - Power Policy #1, WLAN Link Policy `#3: Enabled in S0, Sx/AC'; power source - DC; trigger: PWR button override.</p> <p><b>Notes:</b> If Deep S4/S5 state is enabled on the platform under test, make sure Deep S4/S5 global parameters are configured in PETS:</p> <ol style="list-style-type: none"> <li>1. "Deep S4/S5 enabled" should be set to TRUE</li> <li>2. "Deep S4/S5 Policy" should be configured to the policy chosen in BIOS.</li> </ol>
Objective	This test checks for S3/M-Off to S5/M-Off flow
Procedure	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #1: ON in S0</li> <li>4. Set Wireless Link Policy `#3: Enabled in S0, Sx/AC'. <b>Note:</b> This is required only when wireless is used.</li> <li>5. Set the power source to DC.</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface).</li> <li>8. Move host into Standby (S3).</li> <li>9. Verify that Intel® CSME is off (Intel® AMT does not answer ping by means of the LAN/WLAN interface)</li> <li>10. Press PWR button for more than 5 seconds (power button override).</li> <li>11. If Deep S4/S5 is enabled and configuration policy matches the target power state, check for Deep S4/S5 signal. (For details on Deep S4/S5 policies, refer to the table in the beginning of this chapter)</li> <li>12. Verify that CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li> <li>13. Verify Test Pass/Fail Criteria</li> <li>14. FWSTS: N/A</li> </ol>
Test Pass/Fail Criteria	<p>System goes to S0/M0 and then to S5/M-Off.</p> <p><b>Note:</b> Depending on OEM implementation system may directly go to G3 after power button override event.</p> <p>If Deep S4/S5 is enabled and configuration policy matches the target power state, platform should be in Deep S4/S5 state.</p>



<b>Test ID</b>	<b>ME_PM_19.4a</b>
<b>Test Case Title</b>	S3/M-Off to S5/M-Off in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	<p>This test checks for S3/M-Off to S5/M-Off flow; LAN Power Policy - Power Policy #1, WLAN Link Policy `#3: Enabled in S0, Sx/AC'; power source - ACDC; trigger: PWR button override</p> <p><b>Note:</b> If Deep S4/S5 state is enabled on the platform under test, make sure Deep S4/S5 global parameters are configured in PETS: 1. "Deep S4/S5 enabled" should be set to TRUE 2. "Deep S4/S5 Policy" should be configured to the policy chosen in BIOS.</p>
<b>Objective</b>	This test checks for S3/M-Off to S5/M-Off flow
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #1: ON in S0</li> <li>4. Set Wireless Link Policy `#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Move host to standby (S3)</li> <li>9. Verify that Intel® CSME is off (Intel® AMT does not answer ping by means of the LAN/WLAN interface)</li> <li>10. Press PWR button for more than 5 seconds (power button override)</li> <li>11. If Deep S4/S5 is enabled and configuration policy matches the target power state, check for Deep S4/S5 signal. (For details on Deep S4/S5 policies, refer to the table in the beginning of this chapter)</li> <li>12. Verify that CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li> <li>13. Verify Test Pass/Fail Criteria</li> <li>14. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	<p>System goes to S0/M0 and then to S5/M-Off.</p> <p><b>Note:</b> Depending on OEM implementation system may directly go to G3 after power button override event.</p> <p>If Deep S4/S5 is enabled and configuration policy matches the target power state, platform should be in Deep S4/S5 state.</p>



## B.9 Straight-to-S5, Intel® CSME Power Policy Calls for Sx Operation

<b>Test ID</b>	<b>ME_PM_20.3a</b>
<b>Test Case Title</b>	S3/M3 to S5/M3 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	This test checks for S3/M3 to S5/M3 flow; LAN Power Policy - Power Policy #2, WLAN Link Policy `#3: Enabled in S0, Sx/AC'; power source - ACDC; trigger: Power Button Override
<b>Objective</b>	This test checks for S3/M3 to S5/M3 flow
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy `#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Move host to Standby (S3)</li> <li>9. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>10. Press PWR button for more than 5 seconds (power button override)</li> <li>11. Verify Test Pass/Fail Criteria</li> <li>12. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	System goes to S0/M0 to S5/M-Off and then to S5/M3 after ~ 4-5 seconds.

<b>Test ID</b>	<b>ME_PM_20.4a</b>
<b>Test Case Title</b>	S3/M-Off to S5/M3 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	This test checks for S3/M-Off to S5/M3 flow; LAN Power Policy - Power Policy #2, WLAN Link Policy `#3: Enabled in S0, Sx/AC'; power source - ACDC; trigger: Power Button Override



Test ID	ME_PM_20.4a
Objective	This test checks for S3/M-Off to S5/M3 flow
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Configure idle timeout value in Intel® MEBX to 1</li><li>4. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>5. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li><li>6. Set the power source to AC+DC</li><li>7. Boot the system to S0/M0 that is, make sure OS is up</li><li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>9. Move host into Standby (S3)</li><li>10. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>11. Wait for idle timeout expiry for CSME to enter M-Off (To make sure CSME enters M-Off check SLP_A# status)</li><li>12. Press PWR button for more than 5 seconds (power button override)</li><li>13. Verify Test Pass/Fail Criteria</li><li>14. FWSTS: N/A</li></ol>
Test Pass/Fail Criteria	System goes to S0/M0 to S5/M-Off and then to S5/M3 after ~ 4-5 seconds.

Test ID	ME_PM_20.9a
Test Case Title	S3/M-Off to S5/M-Off in WoWLAN Coexistence Mode
Mandatory/Optional	Mandatory
Description	<p>This test checks for S3/M-Off to S5/M3 flow; LAN Power Policy - Power Policy #2, WLAN Link Policy '#3: Enabled in S0, Sx/AC'; power source - DC; trigger: Power Button Override</p> <p><b>Note:</b> If Deep S4/S5 state is enabled on the platform under test, make sure Deep S4/S5 global parameters are configured in PETS:</p> <ol style="list-style-type: none"><li>1. "Deep S4/S5 enabled" should be set to TRUE</li><li>2. "Deep S4/S5 Policy" should be configured to the policy chosen in BIOS.</li></ol>
Objective	This test checks for S3/M-Off to S5/M-Off flow
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li><li>4. Set Wireless Link Policy '#3: Enabled in S0, Sx/AC'. This is required only when wireless is used.</li><li>5. Set the power source to DC</li><li>6. Boot the system to S0/M0 that is, make sure OS is up</li><li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>8. Move host to Standby (S3)</li><li>9. Verify that Intel® CSME is off (Intel® AMT does not answer ping by means of the LAN/WLAN interface)</li><li>10. Press PWR button for more than 5 seconds (power button override)</li><li>11. If Deep S4/S5 is enabled and configuration policy matches the original power state of this test, check for Deep S4/S5 signal. (For details on Deep S4/S5 policies, refer to the table in the beginning of this chapter)</li><li>12. Verify Test Pass/Fail Criteria.</li><li>13. FWSTS: N/A</li></ol>



<b>Test ID</b>	<b>ME_PM_20.9a</b>
<b>Test Pass/Fail Criteria</b>	Host goes to S5 by means of the S0 and stays in S5. Intel® CSME goes to M-Off. Intel® AMT is not reachable by means of the LAN/WLAN interface. <b>Note:</b> Depending on OEM implementation system may directly go to G3 after power button override event instead of going to S5. If Deep S4/S5 is enabled and configuration policy matches the target power state, platform should be in Deep S4/S5 state.

<b>Test ID</b>	<b>ME_PM_20.22a</b>
<b>Test Case Title</b>	S3/M3 to S5/M3 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	This test checks for S3/M3 to S5/M3 flow; LAN Power Policy - Power Policy #2, WLAN Link Policy `#2: Enabled in S0 only'; power source - ACDC; trigger: Power Button Override
<b>Objective</b>	This test checks for S3/M3 to S5/M3 flow.
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>4. Set Wireless Link Policy `#2: Enabled in S0 only'. This is required only when wireless is used.</li> <li>5. Set the power source to AC+DC</li> <li>6. Boot the system to S0/M0 that is, make sure OS is up</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li> <li>8. Move host to Standby (S3)</li> <li>9. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>10. Press PWR button for more than 5 seconds (power button override)</li> <li>11. After 4-5 seconds Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>12. Verify Test Pass/Fail Criteria</li> <li>13. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	System goes to S0/M0 to S5/M-Off and then to S5/M3 after ~ 4-5 seconds. Intel® AMT answers ping by means of the LAN interface only.

<b>Test ID</b>	<b>ME_PM_20.23a</b>
<b>Test Case Title</b>	S3/M-Off to S5/M3 in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Description</b>	This test checks for S3/M-Off to S5/M3 flow; LAN Power Policy - Power Policy #2, WLAN Link Policy `#2: Enabled in S0 only'; power source - ACDC; trigger: Power Button Override
<b>Objective</b>	This test checks for S3/M-Off to S5/M3 flow



Test ID	ME_PM_20.23a
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li><li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li><li>3. Configure idle timeout value in Intel® MEBX to 1</li><li>4. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4–S5/AC</li><li>5. Set Wireless Link Policy '#2: Enabled in S0 only'. This is required only when wireless is used.</li><li>6. Set the power source to AC+DC</li><li>7. Boot the system to S0/M0 that is, make sure OS is up</li><li>8. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN/WLAN interface)</li><li>9. Move host into Standby (S3)</li><li>10. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>11. Wait for idle timeout expiry for CSME to enter M-Off (To make sure CSME enters M-Off check SLP_A# status)</li><li>12. Press PWR button for more than 5 seconds (power button override)</li><li>13. After 4-5 seconds Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>14. Verify Test Pass/Fail Criteria</li><li>15. FWSTS: N/A</li></ol>
Test Pass/Fail Criteria	System goes to S0/M0 to S5/M-Off and then to S5/M3 after ~ 4-5 seconds. Intel® AMT answers ping by means of the LAN interface only



## B.10 S0/M0 to S3/M-Off (Without Intel® CSME Wake) to S3/M-Off (with Intel® CSME Wake)

<b>Test ID</b>	<b>ME_PM_21.1a</b>
<b>Test Case Title</b>	S0/M0 to S3/M-Off (without Intel® CSME Wake) to S3/M-Off (with Intel® CSME Wake) in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Wireless Only</b>	No
<b>Description</b>	This test checks for S0/M0 to S3/M-Off (without Intel® CSME Wake) to S3/M-Off (with Intel® CSME Wake) flow; This test checks for S3/M-Off to S3/M-Off flow; LAN Power Policy - Power Policy #2;; power source - DC; trigger: DC->ACDC + Wait Idle Time
<b>Objective</b>	This test checks for S0/M0 to S3/M-Off (without Intel® CSME Wake) to S3/M-Off (with Intel® CSME Wake) flow
<b>Procedure</b>	<ol style="list-style-type: none"> <li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li> <li>2. If the SUT has WLAN support, enable the host WoWLAN driver setting.</li> <li>3. Set the idle timeout value in Intel® MEBX to 1</li> <li>4. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4-S5/AC</li> <li>5. Set the power source to DC</li> <li>6. Boot the system to S0/M0 (that is, make sure OS is up)</li> <li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN interface)</li> <li>8. Move host to standby (S3)</li> <li>9. Verify that CSME is in M-Off state. This can be done by checking SLP_A# signal, that should be asserted, indicating Intel® CSME is in M-Off.</li> <li>10. Reconnect AC power cord.</li> <li>11. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li> <li>12. Wait for IdleTimeout expiration to enter M-Off State (To confirm Intel® CSME enters M-Off status check SLP_A# status)</li> <li>13. Verify Test Pass/Fail Criteria</li> <li>14. FWSTS: N/A</li> </ol>
<b>Test Pass/Fail Criteria</b>	Intel® AMT answers ping by means of the LAN interface. Host stays in S3 state. Intel® CSME becomes M3. After Idle timeout expires Intel® CSME turns off.

## B.11 S0/M0 to S3/M-Off (with Intel® CSME Wake) to S3/M-Off (Without Intel® CSME Wake)

<b>Test ID</b>	<b>ME_PM_22.1a</b>
<b>Test Case Title</b>	S3/M-Off (with Intel® CSME Wake) to S3/M-Off (without Intel® CSME Wake) in WoWLAN Coexistence Mode
<b>Mandatory/Optional</b>	Mandatory
<b>Wireless Only</b>	No
<b>Description</b>	This test checks for S3/M-Off to S3/M-Off flow; LAN Power Policy - Power Policy #2;; power source - ACDC; trigger: ACDC->DC



Test ID	ME_PM_22.1a
Objective	This test checks for S0/M0 to S3/M-Off (with Intel® CSME Wake) to S3/M-Off (without Intel® CSME Wake) flow
Procedure	<ol style="list-style-type: none"><li>1. Configure BIOS to keep the system in S5 after exiting G3 (Intel® CSME available)</li><li>2. If the SUT has WLAN support, disable the WoWLAN driver setting.</li><li>3. Set the idle timeout value in Intel® MEBX to 1</li><li>4. Set the Original Power Policy to #2: ON in S0, Intel® CSME Wake in S3/AC, S4–S5/AC</li><li>5. Set the power source to AC+DC</li><li>6. Boot the system to S0/M0 that is, make sure OS is up</li><li>7. Verify that Intel® CSME is on (Intel® AMT answers ping by means of the LAN interface)</li><li>8. Move host to standby (S3)</li><li>9. Verify that Intel® CSME is on (This can be done by checking SLP_A# signal, that should be de-asserted, indicating Intel® CSME is in M3.)</li><li>10. Wait for IdleTimeout expiration to enter M-Off State (To confirm Intel® CSME enters M-Off status check SLP_A# status)</li><li>11. Disconnect AC power cord.</li><li>12. Verify Test Pass/Fail Criteria</li><li>13. FWSTS: N/A</li></ol>
Test Pass/Fail Criteria	Intel® AMT does not answer ping by means of the LAN interface. Host stays in S3 state. Intel® CSME stays M-Off.

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# C Appendix C—Power Management (PM) Stress Test Corporate in WoWLAN Coexistence Mode

For details on WoWLAN Coexistence and WoWLAN Coexistence Mode, including feature availability, review the *Intel® AMT and Wake On Wireless LAN Coexistence* feature overview found in # [546827](#).

**Warning:** In order to fully implement Wake on Wireless LAN (WoWLAN) in Sx states, the host BIOS must set HOST\_WLAN\_PP\_EN. For more further details, refer to the *PCH External Design Specification (EDS)* and the *Platform Design Guide (PDG)*. Failure to properly set the HOST\_WLAN\_PP\_EN bit may result in failures for the tests described herein.

## Tools for Testing:

- Intel® Platform Enablement Test Suite—Latest version of the tool from the Intel® CSME Compliancy kit release. Refer to the Intel® Platform Enablement Test Suite user guide available in the Intel Compliancy kit for exact instructions on how to load and setup the Intel® Platform Enablement Test Suite software.
- System Under Test (SUT)—Should be connected to Intel® Automated Power Switch 3 (Intel® APS 3).

## C.1 PM Test Coverage Summary

Test ID	Test Case Title	PETS/Manual	Form Factor
PM_ST_5	S0/M0 to S3/M-Off to S0/M0	Intel® PETS	DT, MB, WS/Server, LAN, WLAN
PM_ST_6	S0/M0 to S3/M3 to S0/M0	Intel® PETS	DT, MB, WS/Server, LAN, WLAN

**Note:** DT = Desktop, MB = Mobile, WS-Server = Workstation-Server, LAN = systems with LAN interface and test is performed using LAN interface, WLAN = systems with WLAN interface and test is performed using the WLAN interface, WLAN = systems with WLAN interface and test is performed using the WLAN interface, only if the WLAN card supports Host Wake on WLAN.

The tests in this section are designed to be run, individually, a large number of iterations. Some of them require changing the system configuration before being run. When performing very large numbers of iterations, the tests may each take many hours, and in some cases several days.

Intel validation runs each of these tests and the number of iterations indicated. Each OEM should decide the tolerance level required for their boards, and choose an appropriate number of iterations.



The tests in this section are not designed to be run automatically one after the other—the user needs to get the SUT into the starting state, and then run the test multiple times. However each test individually ends with the SUT in the same state as when it started, allowing for easy iteration.

Apart from where explicitly mentioned, the CSME Idle Timeout value should be set larger than 1, to ensure the system does not pass the timeout before the required state is noted.

If the platform is configured with Deep Sx or SUS Well Down enabled (on mobile platforms), according to the enabled Deep Sx S-state (DeepS4/DeepS5), expect the CSME to transition to M-Off when reaching that specific Sx state.

Tests that require the CSME Idle Timeout will fail if there is noise on the network preventing CSME going to an idle state. Ensure that routers with spanning tree, for example, are not present on the network.

When running long iterations, ensure that the management console is set not to go to sleep, as this will pause the test.

Ensure that the SUT can boot to OS without prompting the user for any actions (such as scanning drivers and so forth.), since this will affect the stress tests that boot the SUT to the OS.

## C.2 PM\_ST\_5 - S0/M0 to S3/M-Off to S0/M0

Test ID	PM_ST_5a
Test Case Title	S0/M0 to S3/M-Off to S0/M0 in WoWLAN Coexistence Mode
Mandatory/Optional	Mandatory
Form Factor	Desktop, Mobile, and Workstation/Server
Description/Objective	This test checks for the system power flow from S0/M0 to S3/M-Off to S0/M0
Procedure	<p>If the SUT has WLAN support, enable the host WoWLAN driver setting.</p> <p><b>Initial State:</b> S0/M0</p> <p><b>Power:</b> PP1, ACDC</p> <p>Ensure that yellow bang is not seen on Drivers in Device Manager</p> <p><b>Trigger 1:</b> Host go to S3</p> <p><b>Middle State:</b> S3/M-Off</p> <p><b>Trigger 2:</b> Ping Intel® AMT IP address by means of WS-MAN protocol by means of the WLAN interface to wake system.</p> <p><b>Final State:</b> S0/M0</p> <p>Verify the system is in S0/M0 and verify the second bit of the FWSTS 2 register value should be <b>0x60002306</b></p> <p>Ensure that yellow bang is not seen on Drivers in Device Manager</p> <p>Ensure that no SPI flash log was found in system (For example, use MEinfo to check)</p>
Iterations	Mobile: >= 2000 Desktop: >= 750
Test Pass/Fail Criteria	Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design.



### C.3 PM\_ST\_6 - S0/M0 to S3/M3 to S0/M0

Test ID	PM_ST_6a
Test Case Title	S0/M0 to S3/M3 to S0/M0 in WoWLAN Coexistence Mode
Mandatory/Optional	Mandatory
Form Factor	Desktop, Mobile, and Workstation/Server
Description/Objective	This test checks for the system power flow from S0/M0 to S3/M3 to S0/M0
Procedure	<p>If the SUT has WLAN support, enable the host WoWLAN driver setting.</p> <p><b>Initial State:</b> S0/M0</p> <p><b>Power:</b> PP2, ACDC</p> <p>Ensure that yellow bang is not seen on Drivers in Device Manager</p> <p>Trigger 1: Host go to S3</p> <p><b>Middle State:</b> S3/M3</p> <p><b>Trigger 2:</b> Ping Intel® AMT IP address by means of WS-MAN protocol by means of the WLAN interface to wake system.</p> <p><b>Final State:</b> S0/M0</p> <p>Verify the system is in S0/M0 and verify the second bit of the FWSTS 2 register value should be <b>0x68</b>002106</p> <p>Ensure that yellow bang is not seen on Drivers in Device Manager</p> <p>Ensure that no SPI flash log was found in system (For example, use MEinfo to check)</p>
Iterations	<p>Mobile: &gt;= 2000</p> <p>Desktop: &gt;= 750</p>
Test Pass/Fail Criteria	Test passes, if all steps are completed successfully, for at least the recommended number of iterations as set by the OEM per the tolerance level of the system design.

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